MX•COM, INC. MiXed Signal ICs

DATA BULLETIN

MX375

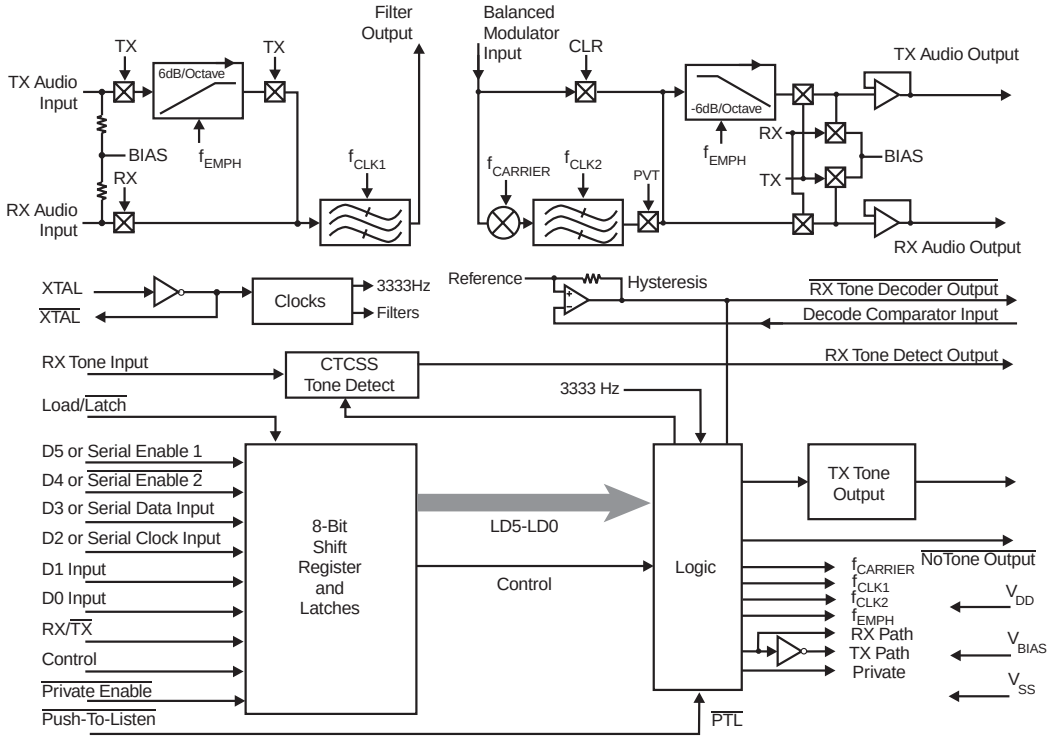
Pvt SQUELCH™ CTCSS Encoder/Decoder

Features

- **PRIVATE/CLEAR CAPABILITY**
- **ON-CHIP TX AUDIO PRE/DEEMPHASIS**
- **ALTERNATIVE TO STANDARD CTCSS "PARTY LINE"**
- **POWERSAVE OPTION**

Applications

- **MOBILE RADIOS**
- **COMMUNITY REPEATERS**
- **TELEPHONE/RADIO INTERCONNECT SYSTEMS**



The MX375 is a CMOS LSI microcircuit which combines CTCSS Encode/Decode operation with voice band frequency inversion. Frequency inversion is achieved by modulating the input audio with a 3333 Hz carrier frequency. Higher voice band frequencies are translated downward, and lower frequencies upward, resulting in a "mirror image" voice transmission. *Pvt*SQUELCH™ combines CTCSS with inverted speech to prevent users from understanding each other's communications unless the transmissions are accompanied by the group's assigned tone. Its net effect is to eliminate casual eavesdropping and give mobile radio users a certain degree of privacy at a minimal price. Up to 38 *Pvt*SQUELCH user groups (one per CTCSS tone) can share a single radio channel. With *Pvt*SQUELCH, competing businesses can share a radio channel without compromising communications security.

Device features: 1) serial or parallel tone programming capability (serial or parallel offered on MX375J, P & LH8), 2) the ability to operate under NOTONE conditions, 3) on-chip Tx and Rx audio filtering, 4) pin-selectable Private/Clear operation, and 5) pre/deemphasis filters in the Tx path, for optimal recovered audio quality.

A low-cost 4 MHz crystal/clock and a single 5V supply are required for operation. The MX375 is available in the following package styles: 28-pin PDIP (MX375P), 28-pin CDIP (MX375J) 28-pin PLCC (MX375LH8), and 24-pin PLCC (MX375LH).

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MX•COM, Inc. reserves the right to change specifications at any time and without notice.

1. Block Diagram

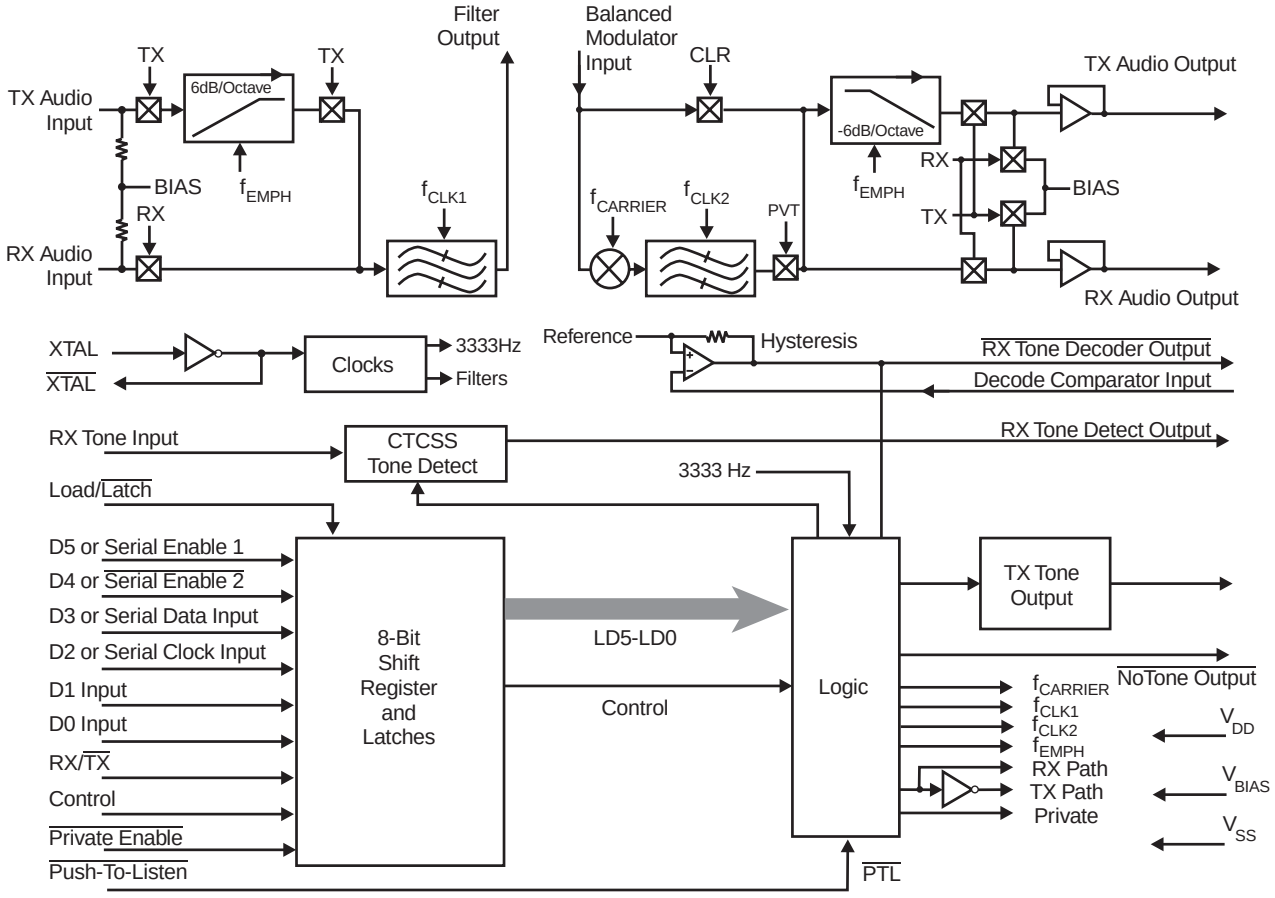


Figure 1: Device Block Diagram

2. Signal List

Pin No.		Name	Type	Description
LH	J,P,LH8			
1	28	V_{DD}	power	5V supply pin.
2	1	XTAL/CLOCK	input	This is the input to the clock oscillator inverter. An external 4 MHz Xtal or clock input should be applied to this pin.
3	2	$\overline{\text{XTAL}}$	output	This is the 4 MHz output of the clock oscillator inverter.
4	3	LOAD/$\overline{\text{LATCH}}$	input	This input controls the eight input latches: RX/$\overline{\text{TX}}$, $\overline{\text{PrivateEnable}}$, and D0-D5, as detailed in Table 5. Alternatively, the RX/$\overline{\text{TX}}$ and $\overline{\text{PrivateEnable}}$ inputs can be addressed separately by setting the Load/$\overline{\text{Latch}}$ and Control inputs as shown in Table 5. 1 MΩ pullup.
5-7		D4-D2	input	Programming Inputs (Serial Mode Only): These are the $\overline{\text{RX}}$/TX tone programming and function inputs which enable the serial programming mode. With Load/$\overline{\text{Latch}}$ at logic "0" serial data is loaded in the following sequence: D5, D4, D3, D2, D1, D0, RX/$\overline{\text{TX}}$, $\overline{\text{PrivateEnable}}$. When these 8 bits have been clocked in on the rising clock edge, data is latched by strobing the Load/$\overline{\text{Latch}}$ input "0 - 1 - 0" (See Figure 5). Pin 5 (D4) = $\overline{\text{Serial Enable2}}$ Pin 6 (D3) = Serial Data Input Pin 7 (D2) = Serial Clock Input
	4-9	D5-D0	input	Parallel Programming Inputs: These are the RX/$\overline{\text{TX}}$ tone programming and function inputs which select the CTCSS tone (See Table 4). *For both Serial and Parallel Modes:* In RX, a NOTONE program enables RX Audio Output and forces the RX Tone Decode Output to a logic "0". In TX, a NOTONE program generates a constant V_{BIAS}-0.7V condition at the TX Tone Output pin. Each input has a 1 MΩ pullup resistor.
8	10	$\overline{\text{RX TONE DECODE}}$	output	The gated output of the decode comparator. In RX, a logic "0" indicates a valid CTCSS tone decode condition, or the presence of NOTONE programming. A logic "0" enables the RX audio path. In TX, this output is held at logic "1".
9	11	DECODE COMPARATOR	input	The voltage level at this pin is compared internally with a fixed reference level. A greater input level compared to the reference will result in a logic "0" at the RX Tone Decode output. This input should be externally connected to the RX Tone Detect output via external integration components C10, R2, R3, and D1 (see Figure 2).
10	12	RX TONE DETECT	output	In RX, this pin outputs a logical "1" when a valid programmed CTCSS tone is received at the RX TONE INPUT. This input should be externally connected to the Decode Comparator input via external integration components C10, R2, R3, and D1 (see Figure 2).
N/A	13	NOTONE	output	This pin outputs a logic "0" when a Notone CTCSS code has been programmed in RX. It is typically used to enable carrier squelch circuits under Notone RX conditions.
11	14	V_{SS}	power	The negative supply pin (ground).
12	15	TX TONE OUTPUT	output	The buffered CTCSS sinewave tone output appears on this pin. In TX mode, the tone frequency is selected by program code (see Table 4); if NOTONE is programmed, the output is at Vbias-0.7V. In RX mode, the output goes open circuit. This is an emitter follower output with an internal 10 kΩ load.

Pin No.		Name	Type	Description
LH	J,P,LH8			
13	16	V_{BIAS}		This pin is set internally to $V_{DD}/2$. It must be externally decoupled using a capacitor (C7) to V_{SS}. See Figure 2.
14	17	FILTER OUTPUT	output	This is the output of the Input Audio Bandpass Filter. It must be A.C. coupled to the Balanced Modulator Input via capacitor C4. See Figure 2.
15	18	BALANCED MODULATOR INPUT	input	This is the input to the balanced modulator. Must be A.C. coupled to the Filter Output via capacitor C4. See Figure 2.
16	19	RX AUDIO OUTPUT	output	Outputs the received audio from a buffered output stage and is held at V_{BIAS} when in TX.
17	20	TX AUDIO OUTPUT	output	Outputs the transmitted audio in TX. In RX, this pin is held at V_{BIAS}.
18	21	RX AUDIO INPUT	input	The audio input for the RX mode. Input signals should be AC coupled via external capacitor C6. See Figure 2
19	22	TX AUDIO INPUT	input	This is the TX Audio voice input. Signals should be AC coupled via external capacitor C11. See Figure 2
20	23	$\overline{\text{PTL}}$	input	The "press to listen" function input. In RX mode, a logic "0" enables the RX Audio Output directly, overriding tone squelch but not intercepting a private conversation; in TX mode, a logic "0" reverses the phase of the TX Tone Output for "squelch tail" reduction (see Table 5).
21	24	CONTROL		This input, together with Load/$\overline{\text{Latch}}$, selects the operational mode of the RX/$\overline{\text{TX}}$ and $\overline{\text{PrivateEnable}}$ functions. See Table 5
22	25	RX/$\overline{\text{TX}}$	input	This input selects the RX or TX mode (RX = 1, TX = 0). This can be loaded in Serial or Parallel modes as described in Table 5
23	26	$\overline{\text{PRIVATE}}$ $\overline{\text{ENABLE}}$		This input selects either Private or Clear mode (Clear = 1, Private = 0), and can be loaded by Serial or Parallel modes as described in Table 5. This input has an internal 1 MΩ pullup resistor.
24	27	RX TONE INPUT	input	This is the received audio input to the on-chip CTCSS tone decoder. It should be A.C. coupled via capacitor C5.

Note: The MX375LH package is available in serial mode only.

Table 1: Signal List

3. External Components

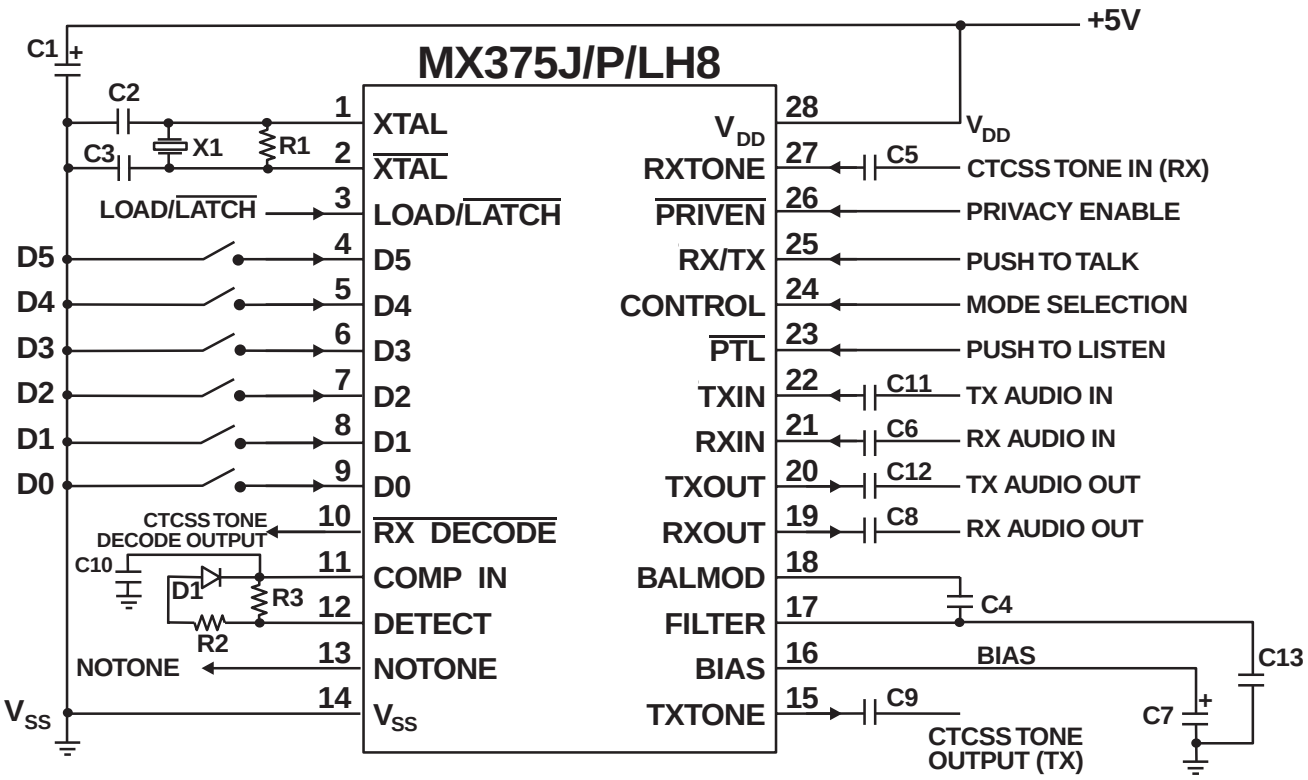


Figure 2: Recommended External Components

R1		1MΩ	±10%
R2		560kΩ	±10%
R3		820kΩ	±10%
X1	Note 1, 2	4MHz	
C1		1.0µF	±20%
C2		33pF	±20%
C3		33pF	±20%
C4		0.1µF	±20%
C5		0.1µF	±20%

C6		0.1µF	±20%
C7		1.0µF	±20%
C8		0.1µF	±20%
C9		0.1µF	±20%
C10		0.1µF	±20%
C11		0.1µF	±20%
C12		0.1µF	±20%
C13		0.001µF	±20%
D1		small signal	

Table 2: Recommended External Components

Recommended External Components Note:

1. For best results, a crystal oscillator design should drive the clock inverter input with signal levels of at least 40% of V_{DD}, peak to peak. Tuning fork crystals generally cannot meet this requirement. To obtain crystal oscillator design assistance, consult your crystal manufacturer.
2. XTAL - At cut, fundamental, parallel resonant 20pF load capacitance, 0.05% tolerance

4. General Description

4.1.1 Pre- and De-emphasis

Pre- and De-emphasis (6dB/octave) filters are included on-chip in the transmit path, so that the use of this device will produce natural sounding audio (clear or private modes) when installed in modern radio communication transceivers, with or without existing audio processing circuitry. The recommended layout is shown in block form below.

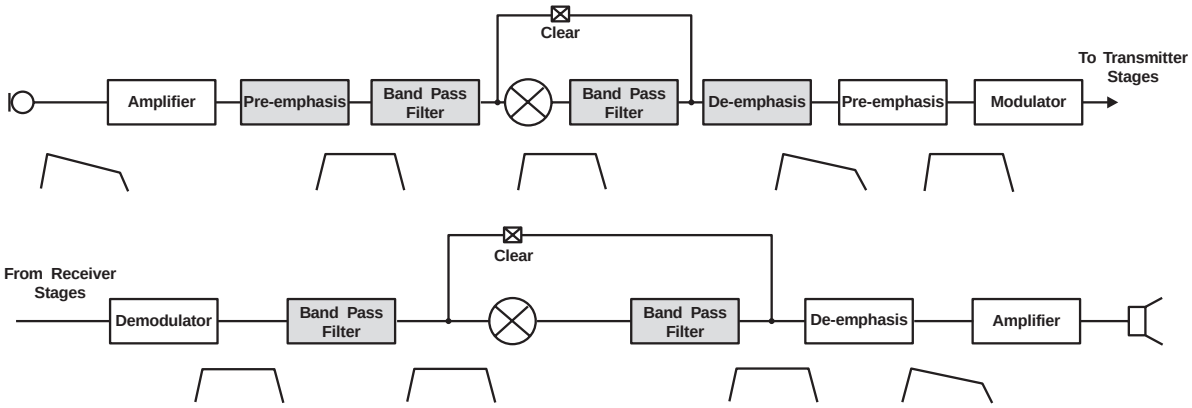


Figure 3: Transmit and Receive Paths

4.1.2 Functions and Outputs

D0-D5	Notone	RX/TX	PRIVATE ENABLE	PTL	RX TONE DETECT	RX TONE DECODER	TONE OUTPUT	TONE PHASE	TX PATH	RX PATH	PATH STATE	TONE
Tone	1	0	0	1	0	1	YES	0°	OPEN	BIAS	INV	TX, TONE
Tone	1	0	0	0	0	1	YES	180°	OPEN	BIAS	INV	TX, TONE REV
Notone	0	0	0	X	0	1	BIAS	X	OPEN	BIAS	CLR	TX, NOTONE
Tone	1	1	0	1	0	1	BIAS	X	BIAS	BIAS	X	INCOMPATIBLE
Tone	1	1	0	0	0	1	BIAS	X	BIAS	OPEN	CLR	INCOMPATIBLE
Tone	1	1	0	X	1	0	BIAS	X	BIAS	OPEN	INV	COMPATIBLE
Notone	0	1	0	X	X	0	BIAS	X	BIAS	OPEN	CLR	RX, NOTONE
Tone	1	0	1	1	0	1	YES	0°	OPEN	BIAS	CLR	TX, TONE
Tone	1	0	1	0	0	1	YES	180°	OPEN	BIAS	CLR	TX, TONE REV
Notone	0	0	1	X	0	1	BIAS	X	OPEN	BIAS	CLR	TX, NOTONE
Tone	1	1	1	1	0	1	BIAS	X	BIAS	BIAS	X	INCOMPATIBLE
Tone	1	1	1	0	0	1	BIAS	X	BIAS	OPEN	CLR	INCOMPATIBLE
Tone	1	1	1	X	1	0	BIAS	X	BIAS	OPEN	CLR	COMPATIBLE
Notone	0	1	1	X	X	0	BIAS	X	BIAS	OPEN	CLR	RX, NOTONE

Table 3: Functions and Outputs

Note:

1. Algebraic functions:
   RX Path On = RX × (PTL + RX Tone Decoder)
   Clear Path = Notone + Private Enable + (PTL × RX × RX Tone Decoder)
   Notone (D0 - D5) = 000011
   Carrier Frequency = 3333Hz During inverted Path (TX or RX)
2. The Pre- and De-emphasis circuits remain in the transmit path in both the Clear and Invert Modes.
3. Power remains applied to the CTCSS tone decoder at all times.
4. During clear operation the carrier frequency is turned off to reduce spurious emissions.

5. Application

5.1.1 CTCSS Programming

Nominal Frequency(Hz)	Frequency(Hz)	Δ F_0 (%)	Program Inputs					
			D5	D4	D3	D2	D1	D0
67.0	67.05	+0.07	1	1	1	1	1	1
71.9	71.9	0	0	1	1	1	1	1
74.4	74.35	-0.07	1	1	1	1	1	0
77.0	76.96	-0.5	0	0	1	1	1	1
79.7	79.77	+0.09	1	1	1	1	0	1
82.5	82.59	+0.1	0	1	1	1	1	0
85.4	85.38	-0.2	1	1	1	1	0	0
88.5	88.61	+0.13	0	0	1	1	1	0
91.5	91.58	+0.09	1	1	1	0	1	1
94.8	94.76	-0.04	0	1	1	1	0	1
97.4	97.29	-0.11	1	1	1	0	1	0
100.0	99.96	-0.04	0	0	1	1	0	1
103.5	103.43	-0.07	0	1	1	1	0	0
107.2	107.15	-0.05	0	0	1	1	0	0
110.9	110.77	-0.12	0	1	1	0	1	1
114.8	114.64	-0.14	0	0	1	0	1	1
118.8	118.8	0	0	1	1	0	1	0
123.0	122.8	-0.17	0	0	1	0	1	0
127.3	127.08	-0.17	0	1	1	0	0	1
131.8	131.67	-0.10	0	0	1	0	0	1
136.5	136.61	+0.08	0	1	1	0	0	0
141.3	141.32	+0.02	0	0	1	0	0	0
146.2	146.37	+0.12	0	1	0	1	1	1
151.4	151.09	-0.2	0	0	0	1	1	1
156.7	156.88	+0.11	0	1	0	1	1	0
162.2	162.31	+0.07	0	0	0	1	1	0
167.9	168.14	+0.14	0	1	0	1	0	1
173.8	173.48	-0.19	0	0	0	1	0	1
179.9	180.15	+0.14	0	1	0	1	0	0
186.2	186.29	+0.05	0	0	0	1	0	0
192.8	192.86	+0.03	0	1	0	0	1	1
203.5	203.65	+0.07	0	0	0	0	1	1
210.7	210.17	-0.25	0	1	0	0	1	0
218.1	218.58	+0.22	0	0	0	0	1	0
225.7	226.12	+0.18	0	1	0	0	0	1
233.6	234.19	+0.25	0	0	0	0	0	1
241.8	241.08	-0.30	0	1	0	0	0	0
250.3	250.28	-0.01	0	0	0	0	0	0
Notone			1	1	0	0	0	0

Table 4: CTCSS Programming

(A) Explanation of Load/Latch function in Serial and Parallel Modes		
Load Configuration	**Load/$\overline{\text{Latch}}$**	**Result**
Parallel	1	Transparent, the data acts directly
Parallel	1 - 0	Latches present data in
Parallel	0	No further changes except to allow serial mode selection
Serial (data loading)	0	No change while serial data train is loaded
Serial (data loaded)	0 - 1 - 0	Loaded serial data is latched

(B) Explanation of Control Input			
Load Configuration	**Load/$\overline{\text{Latch}}$**	**Control**	**RX/$\overline{\text{TX}}$, $\overline{\text{Private Enable}}$**
Parallel	0	0	Latched
Parallel	1	0	Transparent
Parallel	X	1	Transparent
Serial	0 - 1 - 0	0	Serial Load
Serial	X	1	Transparent

Table 5: Load/$\overline{\text{Latch}}$ and Control Input Function

Notes:

1. "0 - 1 - 0" is a strobe pulse as shown in Figure 4 and Figure 5.
2. "X" denotes any logical state.

6. Performance Specification

6.1 Electrical Performance

Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

General	**Min.**	**Typ.**	**Max.**	**Units**
Supply Voltage	-0.3		7.0	V
Input Voltage at any pin	-0.3		(V_{DD} + 0.3)	V
Current				
V_{DD}	-30		30	mA
V_{SS}	-30		30	mA
Any other pin	-20		20	mA
J / P / LH / LH8 Packages				
Total Device Dissipation at T_{AMB} 25°C			800	mW
Derating above 25°C			10	mW/°C above 25°C
Operating Temperature	-40°		85°	C
Storage Temperature	-55°		125°	C

Table 6: Absolute Maximum Ratings

Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Typ.	Max.	Units
Supply (V_{DD}-V_{SS})		4.5	5.0	5.5	V
Operating Temperature		-40		85	°C
Xtal/Clock Frequency			4.0		MHz

Table 7: Operating Limits

Operating Characteristics

For the following conditions unless otherwise specified:

V_{DD} = 5.0V, T_{AMB} = 25°C, XTAL = 4.0MHz, Audio level)dB ref. = 300mV_{RMS}, Composite input signal = 0dB, 1 kHz tone in, -12dB (6kHz band limited) Gaussian white noise with a -20dB CTCSS tone.

	Notes	Min.	Typ.	Max	Units
Static Values					
Supply Voltage		4.5	5.0	5.5	V
Supply Current					
TX (Private)				15.0	mA
TX (Operating)				12.0	mA
RX (Operating)				7.0	mA
Analog Input Impedance			0.5		MΩ
Analog Output Impedance			0.5		kΩ
Tone Input Impedance			0.5		MΩ
Input Logic “1”		3.5			V
Input Logic “0”				1.5	V
Output Logic “1” (I=-0.1mA)		4.0			V
Output Logic “0” (I=-0.1mA)				1.0	V
Dynamic Values					
Decoder					
Input Signal Level	1,4	-20			dB
Response Time	1,4,6			250	ms
Deresponse Time	1,4,6			250	ms
Selectivity	4	±0.5		±3.0	%f_0
Encoder					
Tone Output Level (775mV_{RMS} ref.)		-3.0	0	3.0	dB
Tone Frequency Accuracy		-0.3		0.3	%f_0
Tone Harmonic Distortion			2.0	5.0	%
Tone Output Load Current	2			5.0	mA
Output Level Variation between Tones	9	-1.0		1.0	dB
Risetime (to 90% nominal level)					
(f_0>100 Hz)	5		15		ms
(f_0<100 Hz)	5		45		ms

	Notes	Min.	Typ.	Max	Units
RX Clear					
Total Harmonic Distortion	3		2	5	%
Output Noise Level	7		-43		dB
Passband Gain (300-3033Hz)	3	-1	0	1	dB
Passband Ripple (300-3033Hz)	3			3	dB
Audio Stopband Attenuation					
(f_{IN}>3333Hz)	8		-20		dB
(f_{IN}>3633Hz)	8		-45		dB
(f_{IN}<250Hz)			-42		dB
RX Invert					
Total Harmonic Distortion	3,8		4	10	%
Baseband Breakthrough	3		-40		dB
Carrier Breakthrough			-40		dB
Output Noise Level	7,8		-37		dB
Passband Ripple (300-3000Hz)	3		-	4	dB
Audio Stopband Attenuation					
(f_{IN}>3333Hz)	8		-50		dB
(f_{IN}>3633Hz)	8		-60		dB
(f_{IN}<250Hz)			-60		dB
TX Clear					
Total Harmonic Distortion	3		3	5	%
Output Noise Level	7		-43		dB
Passband Gain (300-3033Hz)	3		0		dB
Passband Ripple (300-3033Hz)	3			3	dB
Audio Stopband Attenuation					
(f_{IN}>3333Hz)	8		-20		dB
(f_{IN}>3633Hz)	8		-45		dB
(f_{IN}<250Hz)			-42		dB
TX Invert					
Total Harmonic Distortion	3,8		4	10	%
Baseband Breakthrough			-40		dB
Carrier Breakthrough			-40		dB
Output Noise Level	7,8		-37		dB
Passband Ripple (300-3033Hz)	3,8			4	dB
Audio Stopband Attenuation					
(f_{IN}>3333Hz)	8		-50		dB
(f_{IN}>3633Hz)	8		-60		dB
(f_{IN}<250Hz)	8		-60		dB

Table 8: Operating Characteristics

Operating Characteristics Notes:

1. These values are obtained using the external integrating components given in Figure 2.
2. An emitter follower output
3. With an input signal of 1 kHz @ 0dB.
4. Under Composite Signal test conditions.
5. Any programmed tone with R_L=600 Ω, C_L=15pF, including any response to a phase reversal instruction.
6. f_0 > 100 Hz, (for 100Hz > f_0 > 67Hz: t = [100/f_0(Hz)] x 250ms).
7. Input ac short-circuit, audio path enabled.
8. Due to frequency inversion, these figures reflect the difference from the ideal response.
9. Reference 156.7 Hz (MX175 and MX275).

6.2 Timing Information

6.2.1 Serial Loading

	Min.	Typ.	Max.	Unit
Serial Mode Enable Set Up Time (t_{SMS})	250	-	-	ns
Clock "High" Pulse Width (t_{PWH})	250	-	-	ns
Clock "Low" Pulse Width (t_{PWL})	250	-	-	ns
Data Set Up Time (t_{DS})	150	-	-	ns
Data Hold Time (t_{DH})	50	-	-	ns
Load/Latch Set Up Time (t_{LL})	250	-	-	ns
Load/Latch Pulse Width (t_{LLW})	150	-	-	ns

Table 9: Serial Loading Timing Information

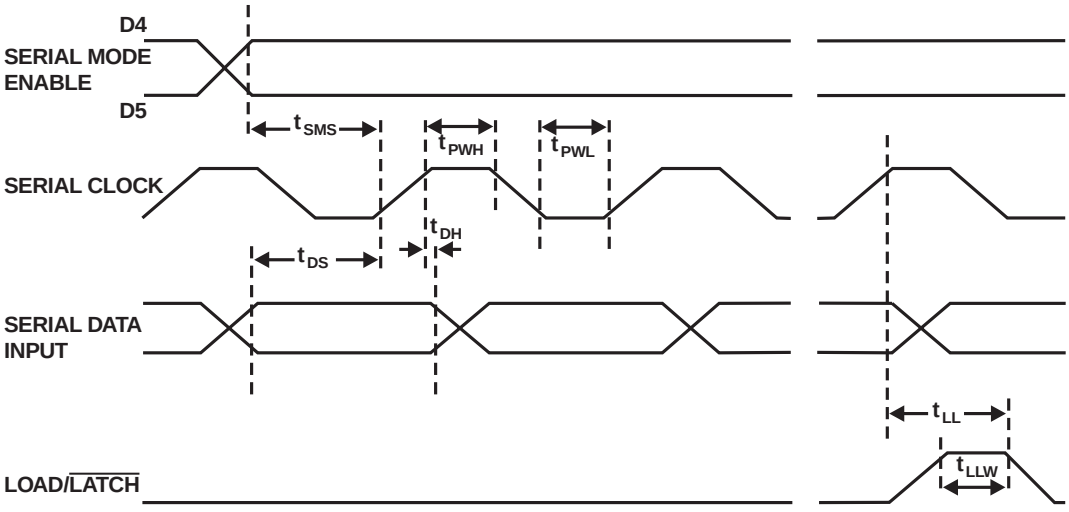


Figure 4: Serial Loading Timing

6.2.2 Parallel Loading

	Min.	Typ.	Max.	Unit
Data Valid Time (t_{VP})	200			ns
Load Time (t_L)	150			ns
Fall Time (t_F)			50	ns
Data Hold Time (t_H)	50			ns

Table 10: Parallel Loading Timing Information

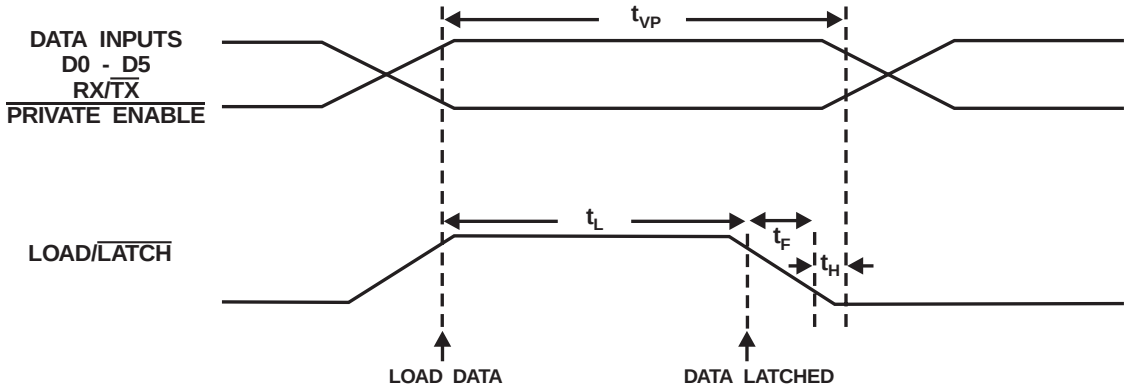
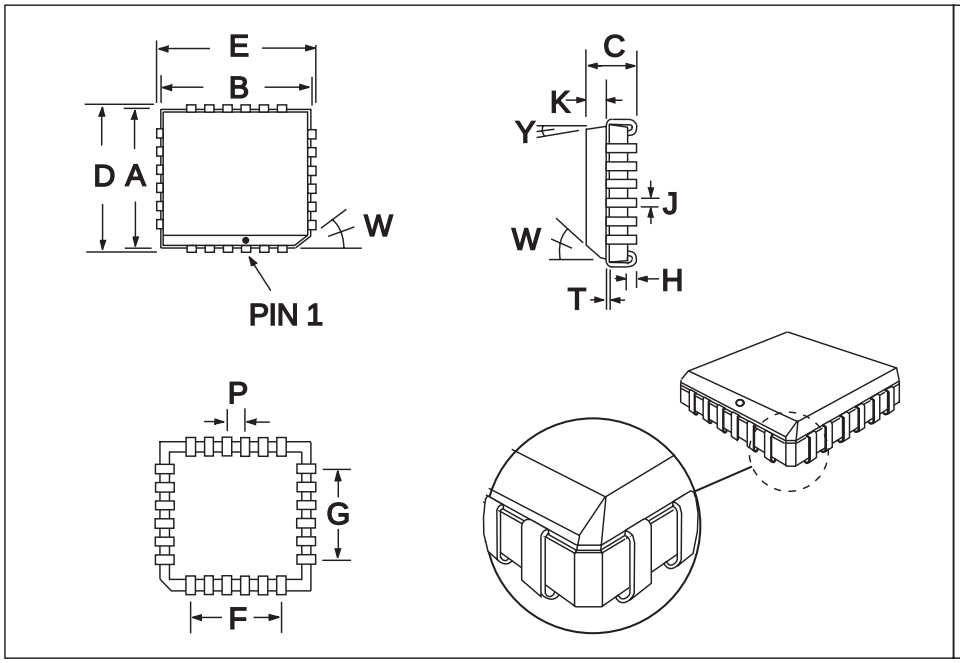


Figure 5: Parallel Load Timing

6.3 Packaging

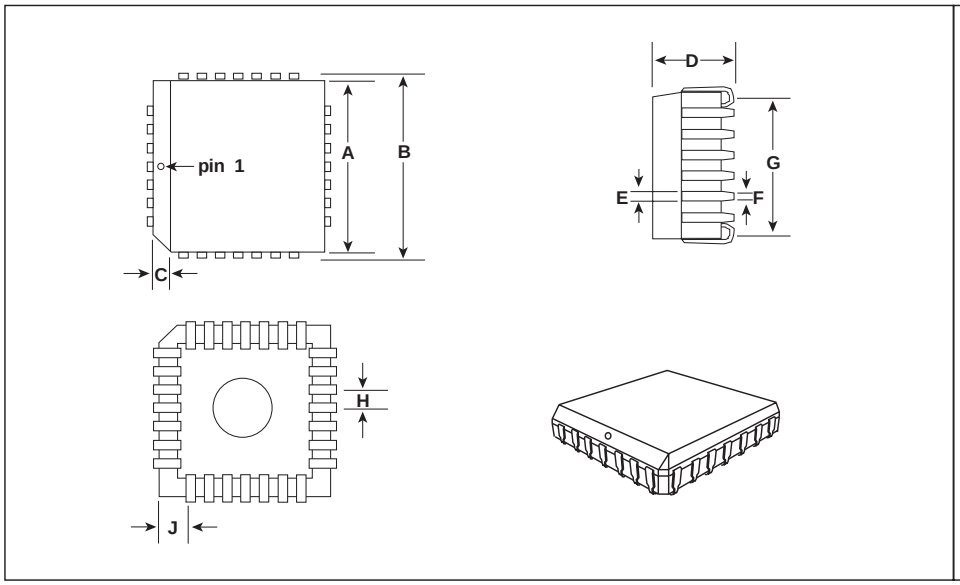


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	0.380 (9.61)		0.409 (10.40)
B	0.380 (9.61)		0.409 (10.40)
C	0.128 (3.25)		0.146 (3.70)
D	0.417 (10.60)		0.435 (11.05)
E	0.417 (10.60)		0.435 (11.05)
F		0.250 (6.35)	
G		0.250 (6.35)	
H		0.023 (0.58)	
J	0.018 (0.45)		0.022 (0.55)
K	0.047 (1.19)		0.048 (1.22)
P	0.049 (1.24)		0.051 (1.30)
T	0.006 (0.152)		0.009 (0.22)
W	30°	45°	
Y		6°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 6: 24-pin PLCC Mechanical Outline: *Order as part no. MX375LH*

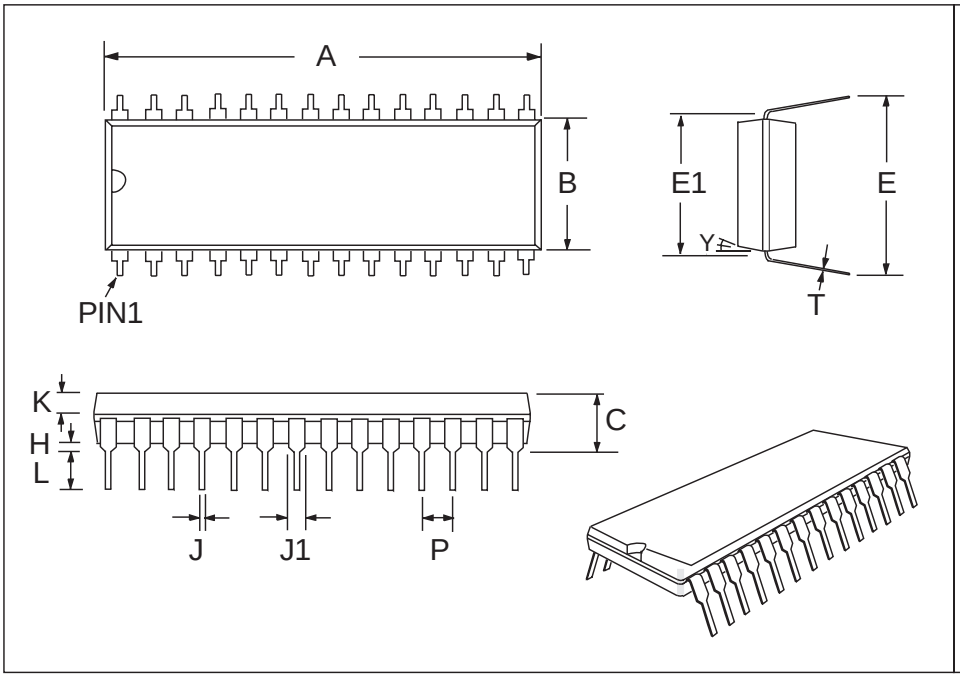


Package Tolerances

DIM.	MIN.	MAX.
A	.450 (11.43)	.453 (11.51)
B	.485 (12.32)	.495 (12.57)
C	.045x45	typical
D	.165 (4.20)	.180 (4.57)
E	.026 (0.66)	.030 (0.76)
F	.017 (0.43)	.021 (0.53)
G	.410 (10.41)	.430 (10.92)
H	.050 (1.27)	typical
J	.070 (1.78)	.085 (2.16)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 7: 28-pin PLCC Mechanical Outline: *Order as part no. MX375LH8*

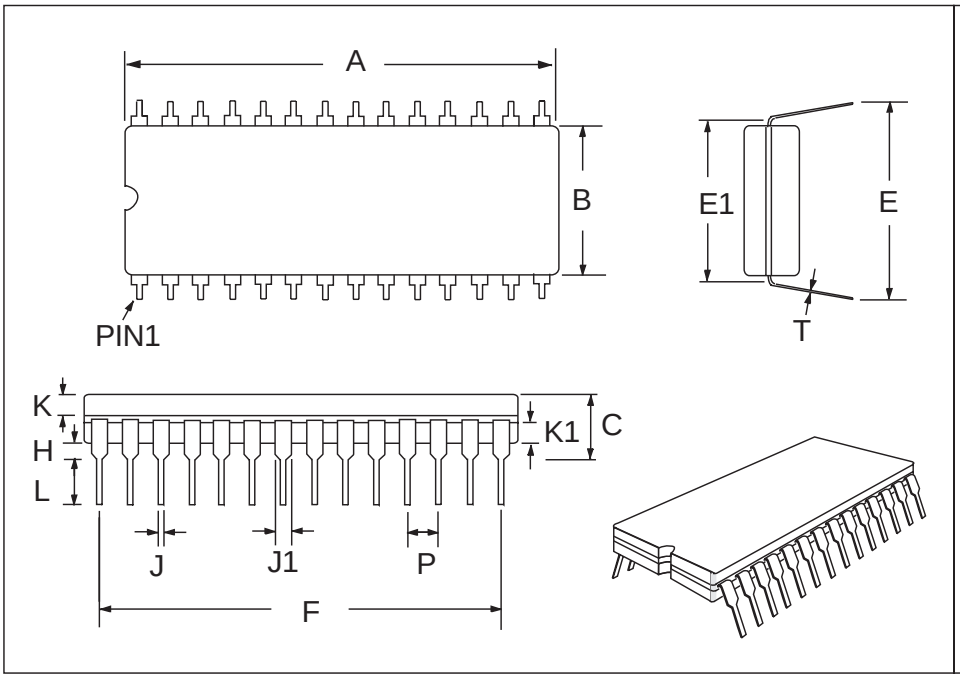


Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.440 (36.44)		1.47 (37.20)
B	0.530 (13.41)		0.555 (14.04)
C	0.160 (4.05)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
H	0.015 (0.38)		0.045 (1.14)
J	0.013 (0.33)		0.021 (0.53)
J1		0.060 (1.52)	
K	0.066 (1.67)		0.074 (1.88)
L	0.125 (3.16)		0.160 (4.05)
P		0.100 (2.54)	
T		0.010 (0.25)	
Y		7°	

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 8: 28-pin PDIP Mechanical Outline: *Order as part no. MX375P*



Package Tolerances

DIM.	MIN.	TYP.	MAX.
A	1.440 (36.58)		1.460 (37.08)
B	0.510 (12.94)		0.530 (13.45)
C	0.165 (4.19)		0.230 (5.84)
E	0.640 (16.26)		0.715 (18.14)
E1	0.608 (15.43)		0.618 (15.70)
F		1.300 (33.02)	
H	0.015 (0.38)		0.050 (1.27)
J		0.018 (0.46)	
J1		0.055 (1.39)	
K	0.050 (1.27)		0.080 (2.03)
K1	0.075 (1.91)		0.080 (2.03)
L	0.115 (2.92)		0.171 (4.34)
P		0.100 (2.54)	
T	0.0090 (0.228)		0.0102 (0.259)

NOTE : All dimensions in inches (mm.)
Angles are in degrees

Figure 9: 28-pin CDIP Mechanical Outline: *Order as part no. MX375J*

CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CML Product Data

In the process of creating a more global image, the three standard product semiconductor companies of CML Microsystems Plc *(Consumer Microcircuits Limited (UK), MX-COM, Inc (USA) and CML Microcircuits (Singapore) Pte Ltd)* have undergone name changes and, whilst maintaining their separate new names *(CML Microcircuits (UK) Ltd, CML Microcircuits (USA) Inc and CML Microcircuits (Singapore) Pte Ltd*), now operate under the single title **CML Microcircuits**.
These companies are all 100% owned operating companies of the CML Microsystems Plc Group and these changes are purely changes of name and do not change any underlying legal entities and hence will have no effect on any agreements or contacts currently in force.

CML Microcircuits Product Prefix Codes

Until the latter part of 1996, the differentiator between products manufactured and sold from MXCOM, Inc. and Consumer Microcircuits Limited were denoted by the prefixes MX and FX respectively. These products use the same silicon etc. and today still carry the same prefixes. In the latter part of 1996, both companies adopted the common prefix: CMX.

This notification is relevant product information to which it is attached.

CML Microcircuits (USA) [formerly MX-COM, Inc.] Product Textual Marking

On CML Microcircuits (USA) products, the **'MX-COM'** textual logo is being replaced by a **'CML'** textual logo.

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