MAXIM

High Speed 12 Bit A/D Converter

MX578

General Description

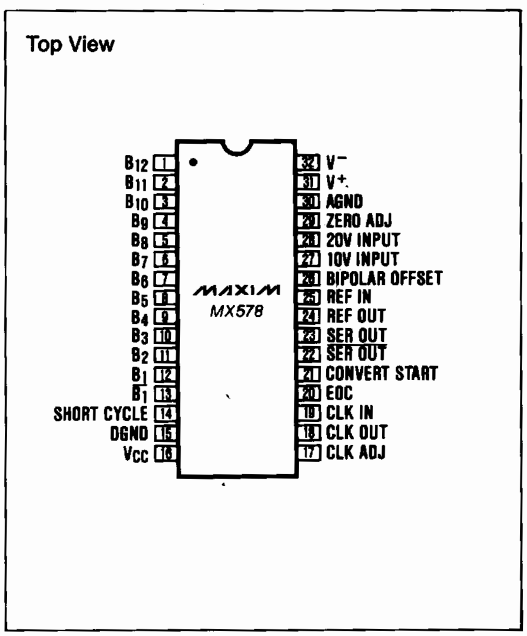
The MX578 is a 12-bit successive approximation analog-to-digital converter complete with internal clock and reference. The combination of bipolar and CMOS technology optimizes accuracy, speed, and power in a convenient 32 pin ceramic DIP. Maximum conversion time is 3μS (L version) however the device may be operated at faster speeds with reduced resolution by short cycling.

Multiple input ranges are accommodated in both unipolar and bipolar modes using internal resistors. These resistors also track those in the reference for low gain drift with temperature. All data bits are available in both parallel and serial form using either the internal or an external clock.

Applications

High Speed Data Acquisition Systems
Transient Recorders
Multichannel Data Loggers
Digital Signal Processing

Pin Configuration



Features

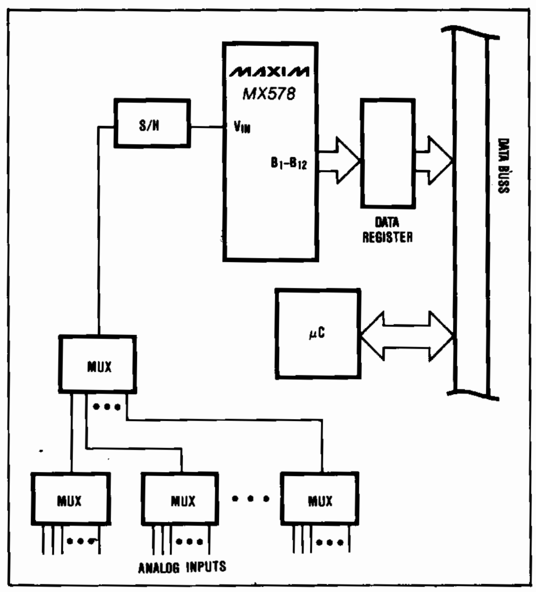
- ♦ Pin-for-Pin Second Source
- ♦ Fast Conversion: 3μs (MX578L)
- ♦ Internal +10V Reference
- ♦ Low Gain TC: 30ppm/°C Max
- ♦ Linearity Error: 0.012% Max
- ♦ No Missing Codes Over Temperature
- ♦ Parallel and Serial Outputs
- ♦ Adjustable Internal Clock
- ♦ Short Cycle Capability

Ordering Information

PART	TEMP. RANGE	PACKAGE
MX578JN	0°C to +70°C	32 Lead Ceramic DIP
MX578KN	0°C to +70°C	32 Lead Ceramic DIP
MX578LN	0°C to +70°C	32 Lead Ceramic DIP
MX578SN	-55°C to +125°C	32 Lead Ceramic DIP
MX578TN	-55°C to +125°C	32 Lead Ceramic DIP

For ±12V Supplies, Order MX578ZXX
(For Hermetic Seal (D) Please Contact Factory.)

Typical Operating Circuit



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ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage, V^+ (pin 31 to GND) .... +18V
Negative Supply Voltage, V^- (pin 32 to GND) .... -18V
Digital Supply Voltage, V_{CC} (pin 16 to GND) .... +7V
Digital Input Voltage
(pins 14, 17, 19, 21) .... GND – 0.5V ≤ V_{IN} ≤ V_{CC} + 0.5V
Analog GND to Digital GND .... ±0.5V

Analog Inputs (pins 25, 26, 27) .... ±12V
(pins 28, 29) .... ±24V
Ref Out .... Indefinite Short to AGND
Momentary Short to V^+
Power Dissipation .... 2W @ 100°C
Storage Temperature .... –65°C ≤ T_A ≤ +160°C
Lead Temperature (Soldering, 10 sec.) .... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (V^+ = +15V, V^- = –15V, V_{CC} = +5V, T_A = +25°C, unless noted—Note 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Offset (Note 1)	Unipolar, T_A = 25°C $T_{MIN} \le T_A \le T_{MAX}$; MX578L,K,J,T MX578S Bipolar (Note 1, 2), T_A = 25°C $T_{MIN} \le T_A \le T_{MAX}$; MX578L,K,J,T MX578S		±0.1 ±3 ±3 ±0.1 ±8 ±8	±0.25 ±10 ±15 ±0.25 ±20 ±25	%FSR ppm/°C ppm/°C %FSR ppm/°C ppm/°C
Gain Error (Note 1, 3)	T_A = 25°C $T_{MIN} \le T_A \le T_{MAX}$; MX578L,K,J,T MX578S		±0.1 ±15 ±15	±0.25 ±30 ±50	%FSR ppm/°C ppm/°C
Linearity	T_A = 25°C $T_{MIN} \le T_A \le T_{MAX}$; MX578L,K,J MX578S,T		 ¾ 	½ ¾	LSB
Differential Linearity Error	$T_{MIN} \le T_A \le T_{MAX}$		no missing codes		
Differential Linearity Drift	$T_{MIN} \le T_A \le T_{MAX}$		±2		ppm/°C
Reference Voltage Accuracy	$V_{nominal}$ = 10.000V		±10	±100	mV
Reference Voltage Drift	$T_{MIN} \le T_A \le T_{MAX}$		±10	±30	ppm/°C
Reference Output Current		±1			mA
Power Supply Rejection Ratio (Note 5)	V^+ = +13.5 to +16.5V V^- = –13.5 to –16.5V V_{CC} = +4.5 to +5.5V			0.005 0.005 0.005	%/%ΔV
Conversion Speed	MX578L MX578K,T MX578J,S	3.0 4.5 6.0			µs
Input Impedance	0V to +10V range 0V to +20V range -5V to +5V range –10V to +10V range		5 10 5 10		kΩ
Power Supply Range (Note 5)	V^+ V^- V_{CC}	13.5 –13.5 4.75		16.5 –16.5 5.25	V
Power Supply Current	V^+ V^- V_{CC}		11 21 45	15 35 80	mA
Power Dissipation			0.7	1.15	W
Operating Temperature Range	MX578L,K,J MX578S,T	0 –55		+70 +125	°C
Logic Output Drive Logic Input Load	B_1–B_{12}, $\overline{B_1}$, $\overline{\text{CLOCK OUT}}$ SER OUT, $\overline{\text{SER OUT}}$ EOC CLOCK IN, CONVERT START		2 2 8 1		LS TTL Loads
Parallel Output Code	Unipolar Bipolar	Binary Offset Binary/Two's Complement			
Serial Output Code	Unipolar Bipolar	Binary/Complementary Binary Offset Binary/Complementary Offset Binary			

Note 1: Adjustable to zero.
Note 2: 50Ω, 1% resistor between pins 24 and 26.
Note 3: 50Ω, 1% resistor between pins 24 and 25.
Note 4: MX578ZXX models, V^+ = +12V, V^- + -12V
Note 5: 'Z' models, V+ = 11.6V to 12.6V, V^- = -11.6V to -12.6V

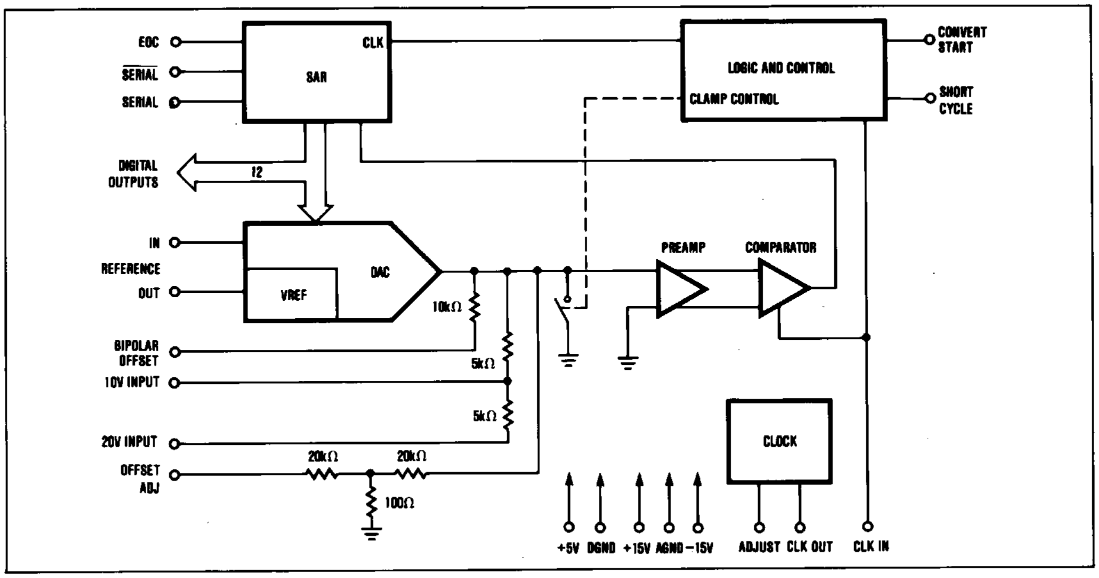


Figure 1. Maxim MX578 Block Diagram.

Detailed Description

The MX578 is a 12-bit successive approximation A/D converter in which the analog input is compared to the output of a high speed D/A converter (Figure 1). The D/A is binarily stepped until its output matches the analog input. The digital code from the successive approximation register (SAR) appears on the outputs as the binary value of the input voltage. The conversion processs consists of twelve successive tests, starting with the D/A set to half Full Scale (FS). The comparator determines whether the D/A output is higher or lower than the analog input and either sets or resets Bit 1 (MSB). On the next test, the D/A is incremented up or down ¼ FS, based on the last decision, and is again compared to the input. The result is stored as BIT 2. Each comparator decision is clocked into the SAR for the remaining bits until all twelve have been tested.

A positive going pulse on Convert Start resets the D/A Converter to ½ FS and sets the End-Of-Convert (EOC) high indicating that a conversion is in progress (Figure 7). The internal clock is enabled and the conversion begins on the trailing edge of the Start Convert (S) pulse. After the last bit has been tested, EOC goes LOW indicating that the output data is valid.

Calibration Procedure

For a large number of MX578 applications no user calibration is needed. The performance limits for an uncalibrated device are given in the Electrical Characteristics section. If more precision is required then offset and gain adjustments can be made as follows.

Table 1. Calibration Chart

	ANALOG INPUT VOLTAGE				OUTPUT CODE(1) MSB LSB
	0 TO +10V	0 TO +20V	-5 TO +5V	-10 TO +10V	MSB LSB
+FS -1LSB	+9.9976	+19.9951	+4.9976	+9.9951	1111 1111 1111
+FS -1½LSB	+9.9964	+19.9927	+4.9964	+9.9927	1111 1111 111@
Mid Scale +½LSB	+5.0012	+10.0024	+0.0012	+0.0024	1000 0000 000@
Mid Scale	+5.0000	+10.0000	+0.0000	+0.0000	1000 0000 0000
-FS +½LSB	+0.0012	+0.0024	-4.9988	-9.9976	0000 0000 000@
-FS	+0.0000	+0.0000	-5.0000	-10.0000	0000 0000 0000

Note 1: The symbol "@" indicates a 0 or 1 with equal probability.

High Speed 12 Bit A/D Converter

Keeping in mind that the offset must always be adjusted before the gain, set the system into a mode of continuous conversions with a high repetition rate (>1kHz) while monitoring the output data lines using an oscilloscope, logic analyzer triggered on EOC, or LED's driven by latched data outputs clocked by EOC. Using a DVM, set the input voltage ½ LSB above −Full Scale (−FS) for the appropriate range (Table 1). Adjust the offset potentiometer (Figure 2) so that the LSB (B_{12}) alternates between a "0" and "1" with a 50% duty cycle with all the other bits OFF. Using LED's, the LSB will appear at half intensity. The gain is similarly set by applying a voltage of +FS −1½LSB (Table 1) and adjusting the LSB for the same 50% ON condition with the exception that all the other bits are ON.

In bipolar mode, it is often desired to calibrate the bipolar zero condition at mid scale rather than the −FS offset. In this case set the input to MID SCALE +½LSB and adjust the LSB for 50% duty cycle with all bits off except B_1 (MSB).

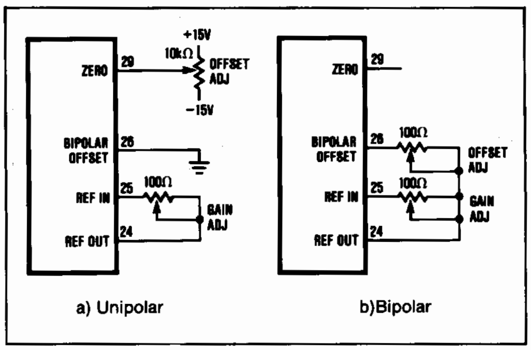


Figure 2. Unipolar and Bipolar Calibration Circuit.

Clock Adjust

The internal clock on all grades is set for a nominal 5.8µs with tolerance of about +0.2µs with no external components connected to pin 17. To obtain 3.0µs for the L grade, connect an 825Ω resistor as shown in Figure 5(a). For K and T grades, use a 3.3kΩ resistor for 4.5µs. For J and S grades, it is recommended that no adjustment be made unless exactly 6.0µs is required.

For faster conversion speeds, connect a resistor chosen from Figure 3 between pins 17 and 18. For slower conversions, connect a capacitor, Figure 4, from pin 17 to GND. A combination of both resistor and capacitor maybe used particularly for fine adjustment of slow clock settings (Figure 5).

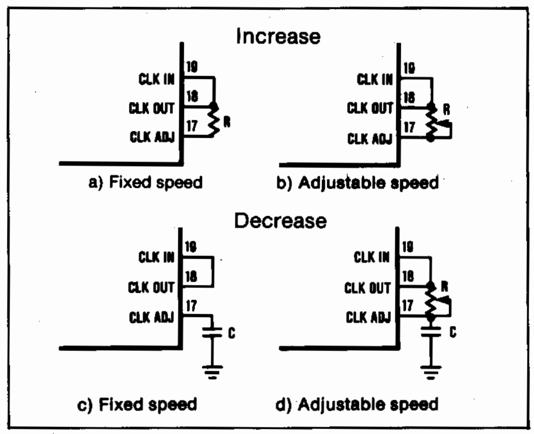


Figure 5. Adjusting the Internal Clock.

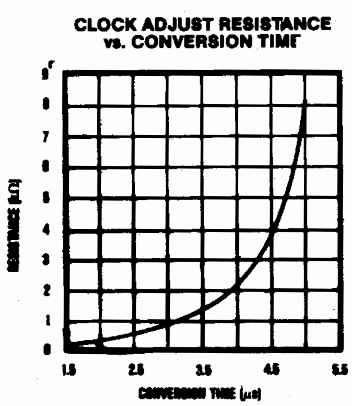


Figure 3. Speed vs. Resistance.

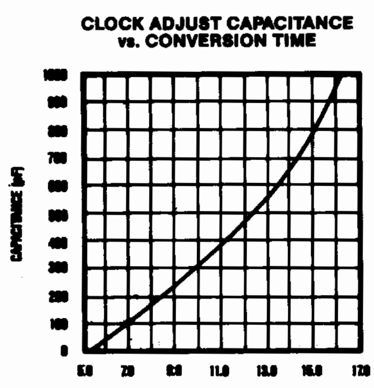


Figure 4. Speed vs. Capacitance.

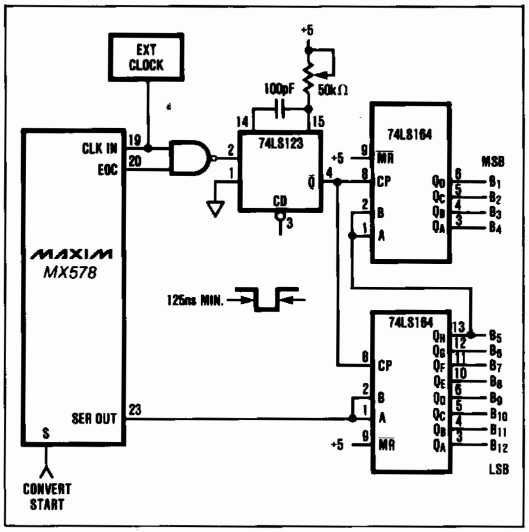
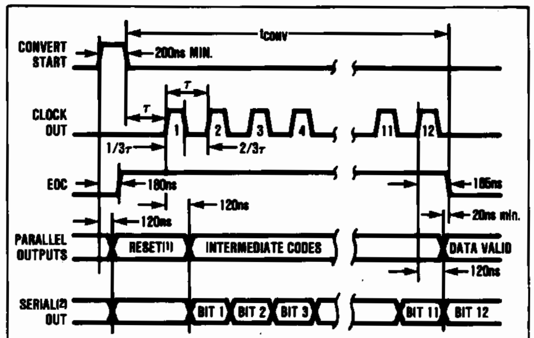


Figure 6. Serial Output with External Clock.



t_{conv}(μs)	τ(ns)
3	240
4.5	360
6	480

Note 1. 1. Reset = 0111 1111 1111 (MSB...LSB)
Note 2. Additional 20ns delay for SER OUT

Figure 7. Timing Diagram.

Short Cycle

For conversions of less than 12 bits, SHORT CYCLE, pin 14, must be connected to the next higher bit than the desired resolution. For example, connecting pin 14 to pin 2 will result in 10 bit conversions. When using an external clock, EOC must also be used to inhibit the CLK IN.

External Clock

The external clock can be used for synchronous applications, such as clocking the serial output data into a serial-to-parallel shift register (Figure 6). The clock should have a duty cycle between 30% and 70%. The main advantage of serial transmission is the reduction in the number of output lines from 12 to 1, which is particularly useful when using optical couplers or sending data over long distances.

Application Hints

Layout

The Analog and Digital Grounds should be directly connected together as close as possible to the package and then tied to a quiet analog ground with no switching transients taking place during the conversion. A ground plane works best, but is not necessary if large traces are used. It is advisable to filter the supplies with 10μF electrolytic capacitors on the PC board along with 0.1μF bypassing capacitors as close to the supply pins on the MX578 as possible. Above all, separate the analog circuit connections, pins 24 through 32, away from the digital section. If a digital signal must cross an analog connection, make sure it crosses at a ninety degree angle on different sides of the board if at all possible.

If using only the 20V input range, leave the 10V input (pin 27) completely unconnected since capacitance on this high impedance point can degrade dynamic performance. When relays or switches are used, mount them as close to the input pins as possible.

Although not necessary to achieve rated specifications, it is recommended that a 10μF electrolytic capacitor be connected on REF OUT to GND for improved noise on the code transitions.

Interfacing

The digital outputs of the MX578 should be latched since they are constantly changing during the conversion. Edge triggered, rather than transparent latches are preferred, such as the 74LS574 (Figure 8), to prevent changing data lines feeding back into the analog portions of the A/D converter. Capacitive loading above 30pF as well as connections more than a few inches long should be avoided on the digital outputs of the A/D.

Input Signal Conditioning

The analog input should be driven by a wide bandwidth, low output impedance op amp or a fast sample-hold. Although V_{IN} may not change during the conversion, the load current of the A/D abruptly changes with each clock cycle due to successive DAC codes (Figure 1). The amplifier must recover to the original value in time for the rest of the circuit to settle before the comparator can make a decision. An op amp which can settle to 0.01% in 50 to 100ns for a 0.5mA change in load current with no thermal tail and low offset voltage drift is recommended.

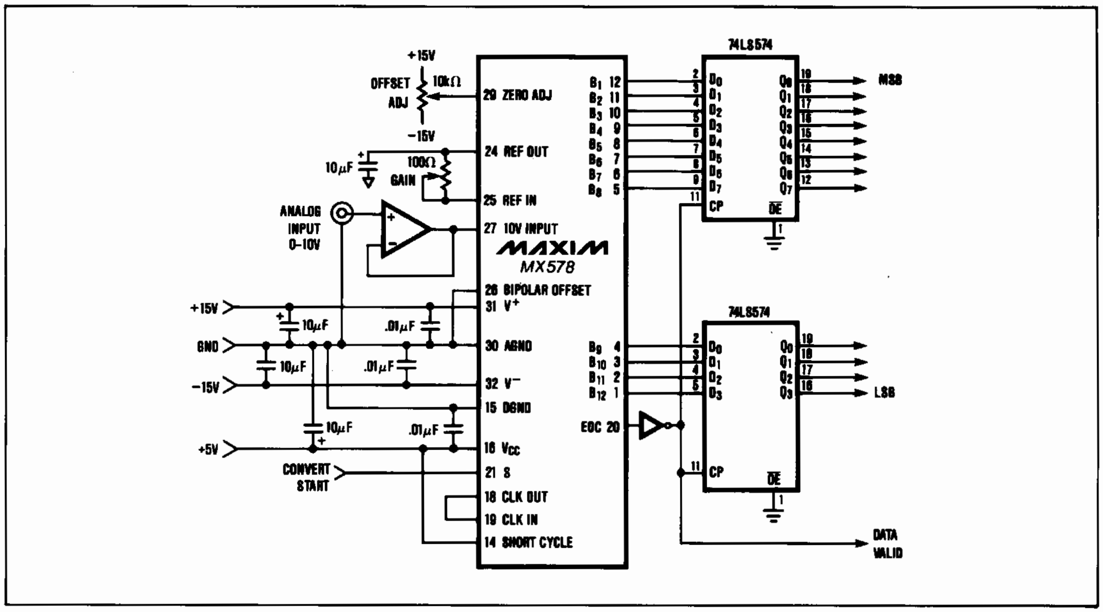


Figure 8. Typical Application for Unipolar 0-10V Range.

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