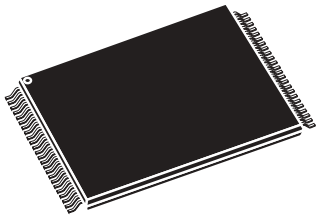
NAND01GR3B2C NAND01GW3B2C NAND01GR4B2C NAND01GW4B2C

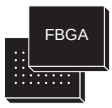
1-Gbit, 2112-byte/1056-word page, 1.8 V/3 V, single level cell NAND flash memory

Features

- NAND interface
  - x8 or x16 bus width
  - Multiplexed address/ data
  - Pinout compatibility for all densities
- Supply voltage: 1.8 V/3 V
- Page size
  - x8 device: (2048 + 64 spare) bytes
  - x16 device: (1024 + 32 spare) words
- Block size
  - x8 device: (128K + 4K spare) bytes
  - x16 device: (64K + 2K spare) words
- Page read/program
  - Random access: 25 µs (max)
  - Sequential access: 25 ns (min)
  - Page program time: 200 µs (typ)
- Copy back program mode
- Cache read mode
- Fast block erase: 2 ms (typ)
- Status register
- Electronic signature
- Chip enable ‘don’t care’
- Security features
  - OTP area
  - Serial number (unique ID)
  - Non-volatile protection option
- Data protection
  - Hardware block locking
  - Hardware program/erase locked during power transitions
- ONFI 1.0 support
  - Cache read
  - Read signature
  - Read
- Data integrity
  - 100,000 program/erase cycles per block (with ECC)
  - 10 years data retention
- RoHS compliant packages
- Development tools
  - Error correction code models
  - Bad blocks management and wear leveling algorithms
  - Hardware simulation models



TSOP48 12 x 20 mm



VFBGA63 9 x 11 x 1.05 mm

VFBGA153 8 x 9 x0.9 mm

Table 1. Device summary

Reference	Root part numbers
NAND01G-B2C	NAND01GR3B2C, NAND01GW3B2C
	NAND01GR4B2C, NAND01GW4B2C(1)

1. x16 organization only available for MCP products.

Contents

List of tables

List of figures

1 Description

The NAND01G-B2C is a 1-Gbit device belonging to the NAND SLC large page family. The device operates with a 1.8 V or 3 V voltage supply. The size of a page is either 2112 bytes (2048 + 64 spare) or 1056 words (1024 + 32 spare) depending on whether the device has a x8 or x16 bus width.

The address lines are multiplexed with the data input/output signals on a multiplexed x8 or x16 input/output bus. This interface reduces the pin count and makes it possible to migrate to other densities without changing the footprint.

Each block can be programmed and erased up to 100,000 cycles (with ECC on). To extend the lifetime of NAND flash devices, the implementation of an error correction code (ECC) is mandatory.

The devices feature a write protect pin that allows performing hardware protection against program and erase operations.

The devices feature an open-drain ready/busy output that can be used to identify if the program/erase/read (P/E/R) controller is currently active. The use of an open-drain output allows the ready/busy pins from several memories to be connected to a single pull-up resistor.

A Copy Back Program command is available to optimize the management of defective blocks. When a page program operation fails, the data can be programmed in another page without having to resend the data to be programmed.

The cache read feature is also implemented according to ONFI 1.0 specification.

All devices have the chip enable don’t care feature, which allows the bus to be shared among several memories active at the same time, as chip enable transitions during the latency time do not stop the read operation. Program and erase operations can never be interrupted by chip enable transitions.

The devices are available in the following packages:

- TSOP48 (12 x 20 mm)
- VFBGA63 (9 x 11 x 1.05 mm, 0.8 mm pitch)
- VFBGA153 (8 x 9 x 0.9 mm, 0.5 mm pitch)

and come with three security features:

- OTP (one time programmable) area, which is a restricted access area where sensitive data/code can be stored permanently.
- Serial number (unique identifier), which allows the devices to be uniquely identified.
- Non-volatile protection to lock sensible data permanently. For more details of this option contact your nearest Numonyx sales office.

These security features are subject to an NDA (non-disclosure agreement) and are, therefore, not described in the datasheet. For more details about them, refer to the nearest Numonyx sales office.

For information on how to order these options refer to *Table 28: Ordering information scheme*. Devices are shipped from the factory with block 0 always valid and the memory content bits, in valid blocks, erased to ’1’.

See *Table 2: Product description*, for all the devices available in the family.

Table 2. Product description

Reference	Part number	Density	Bus width	Page size	Block size	Memory array	Operating voltage	Timings				Package
								Random access time (max)	Sequential access time (min)	Page Program time (typ)	Block erase (typ)	
NAND01G-B2C	NAND01GR3B2C	1 Gbit	x8	2048 +64 bytes	128K +4K bytes	64 pages x 1024 blocks	1.7 to 1.95 V	25 µs	45 ns	200 µs	2 ms	VFBGA63 VFBGA153
	NAND01GW3B2C						2.7 to 3.6 V	25 µs	25 ns			TSOP48
	NAND01GR4B2C		x16	1024 +32 words	64K+ 2K words		1.7 to 1.95 V	25 µs	45 ns			(1)
	NAND01GW4B2C						2.7 to 3.6 V	25 µs	25 ns			(1)

1. x16 organization only available for MCP.

Figure 1. Logic block diagram

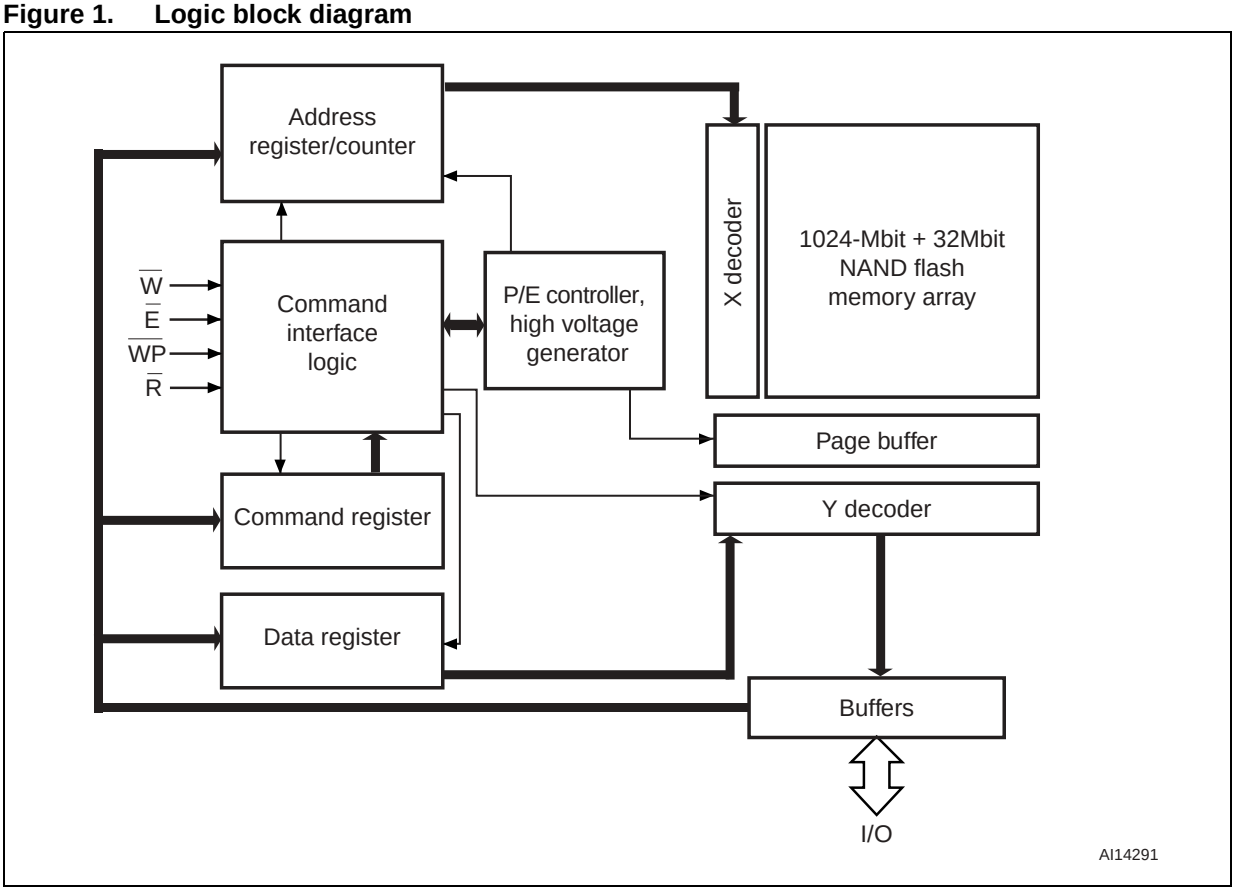
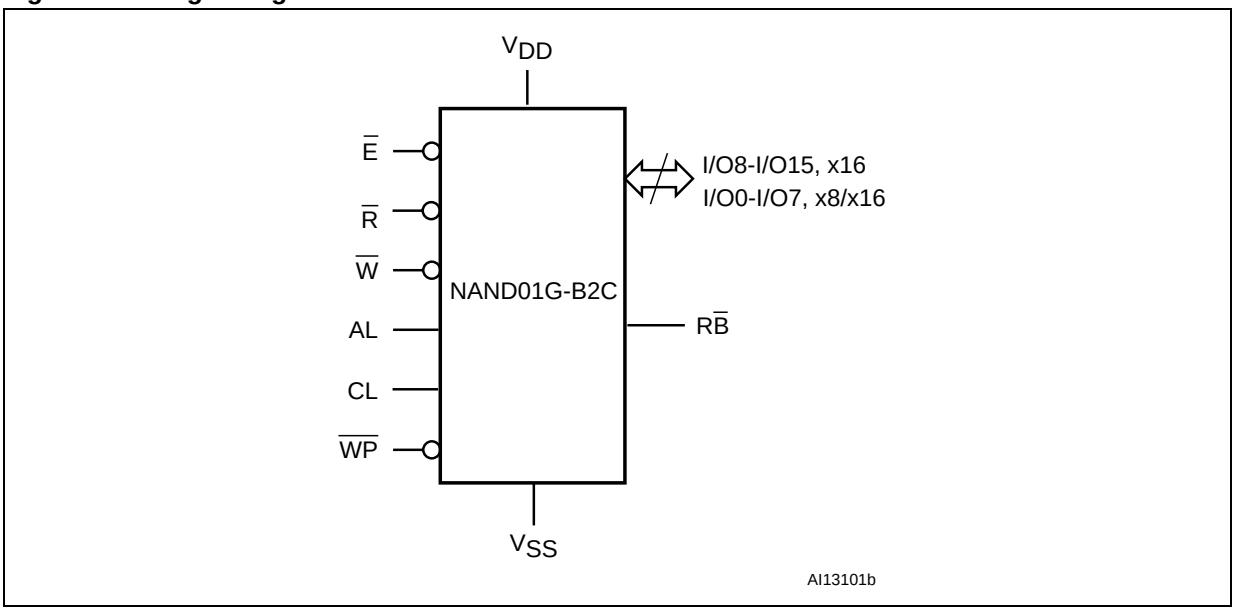


Figure 2. Logic diagram

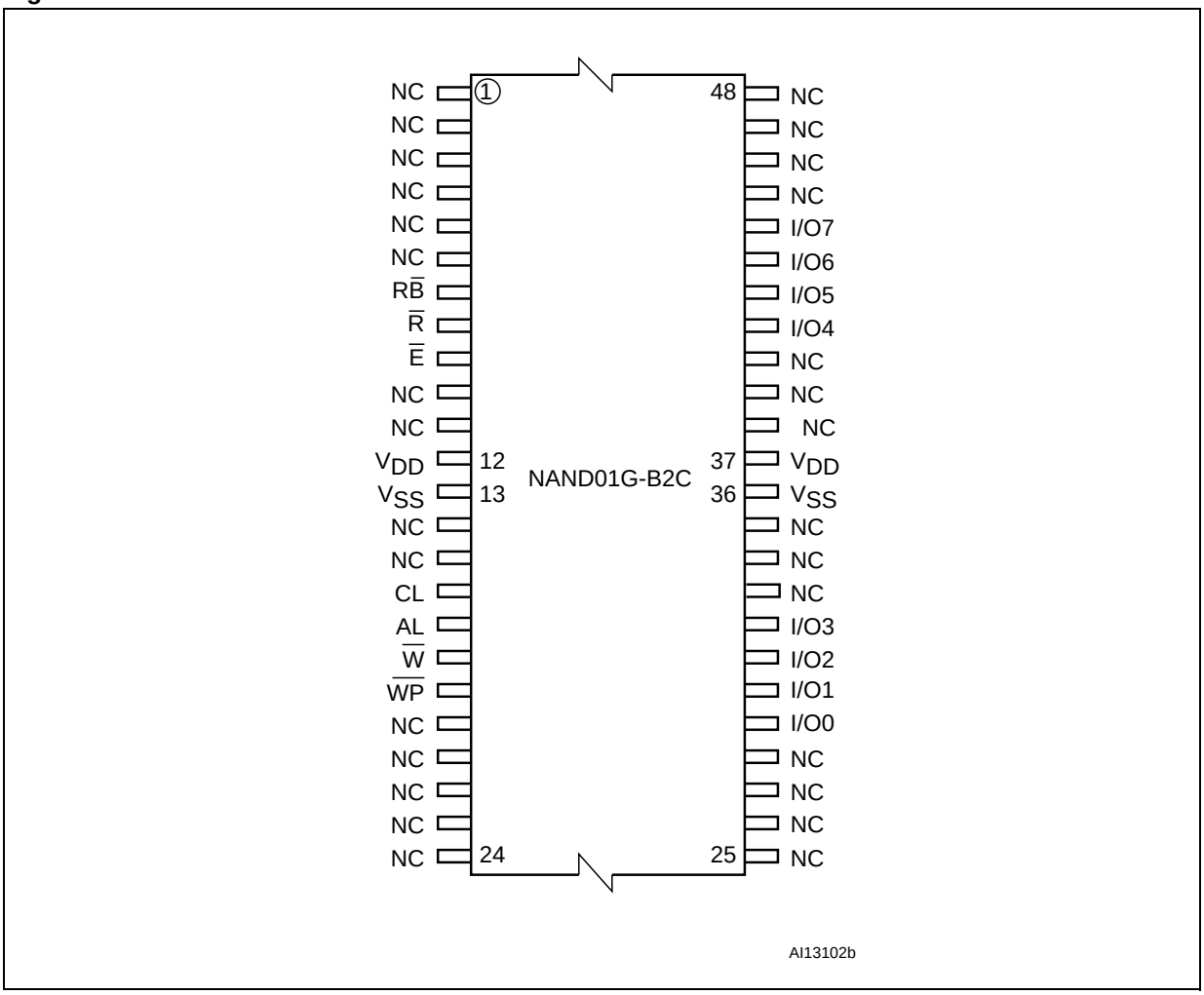


1. x16 organization only available for MCP.

Table 3. Signal names

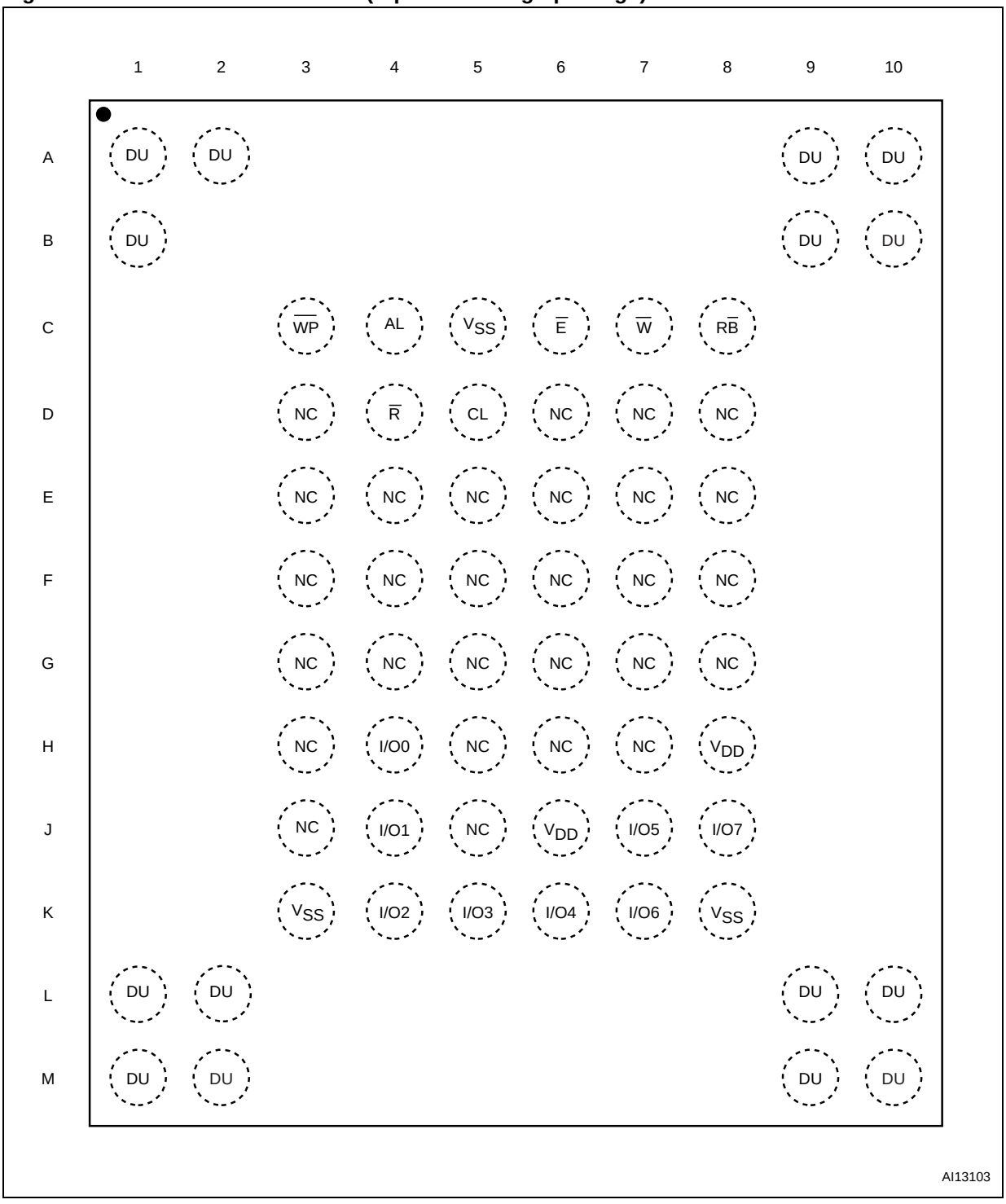
Signal	Function	Direction
I/O8-15	Data input/outputs for x16 devices	I/O
I/O0-7	Data input/outputs, address inputs, or command inputs for x8 and x16 devices	I/O
AL	Address Latch Enable	Input
CL	Command Latch Enable	Input
$\overline{E}$	Chip Enable	Input
$\overline{R}$	Read Enable	Input
$R\overline{B}$	Ready/Busy (open-drain output)	Output
$\overline{W}$	Write Enable	Input
$\overline{WP}$	Write Protect	Input
V_{DD}	Supply voltage	Supply
V_{SS}	Ground	Supply
NC	Not connected internally	–
DU	Do not use	–

Figure 3. TSOP48 connections



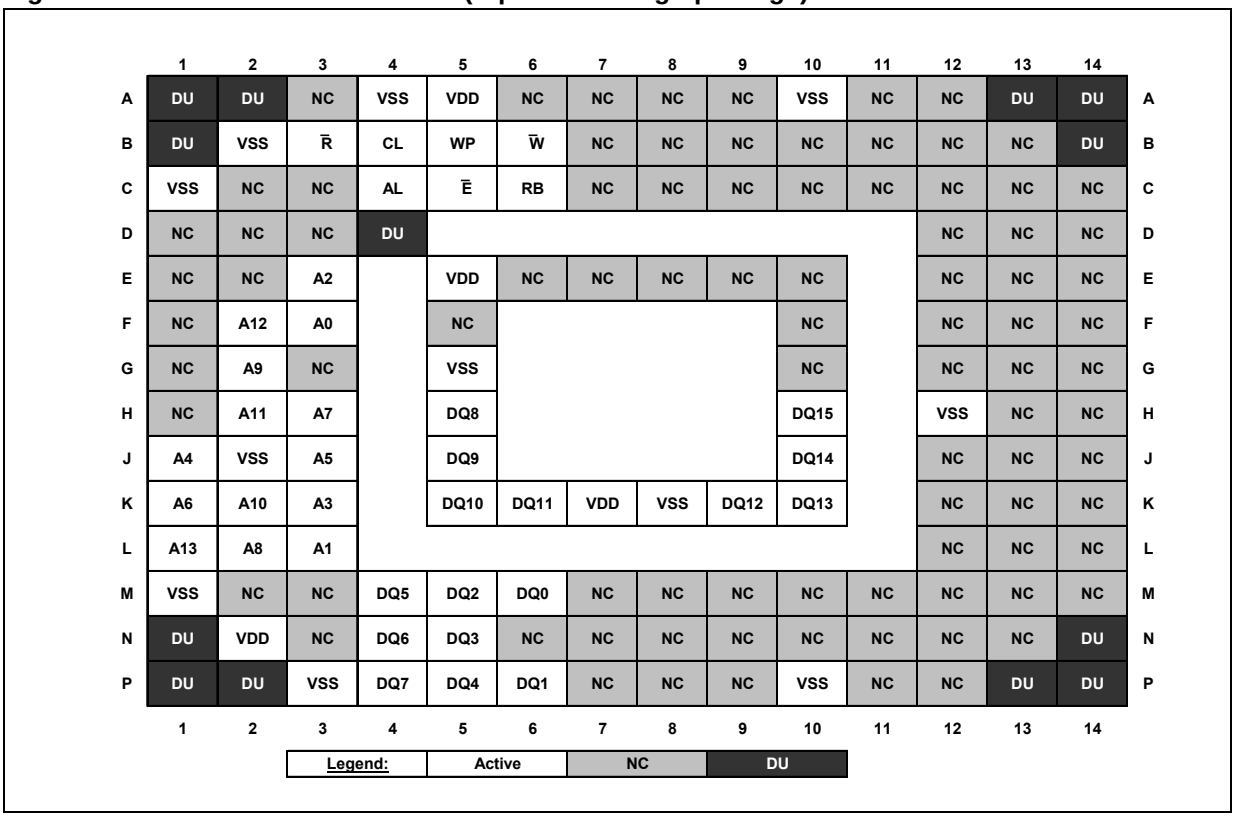
1. Only available for 3 V devices.

Figure 4. VFBGA63 connections (top view through package)



1. Only available for 3 V devices.

Figure 5. VFBGA153 connections (top view through package)



2 Memory array organization

The memory array is made up of two NAND structures where 32 cells are connected in series.

The memory array is organized in blocks where each block contains 64 pages. The array is split into two areas, the main area and the spare area. The main area of the array is used to store data whereas the spare area is typically used to store error correction codes, software flags or bad block identification.

In x8 devices the pages are split into a 2048-byte main area and a spare area of 64 bytes. In the x16 devices the pages are split into a 1024-word main area and a 32-word spare area. Refer to *Figure 6: Memory array organization*.

2.1 Bad blocks

The NAND flash 2112-byte/1056-word page devices may contain bad blocks, that is blocks that contain one or more invalid bits whose reliability is not guaranteed. Additional bad blocks may develop during the lifetime of the device.

The bad block Information is written prior to shipping (refer to *Section 8.1: Bad block management* for more details).

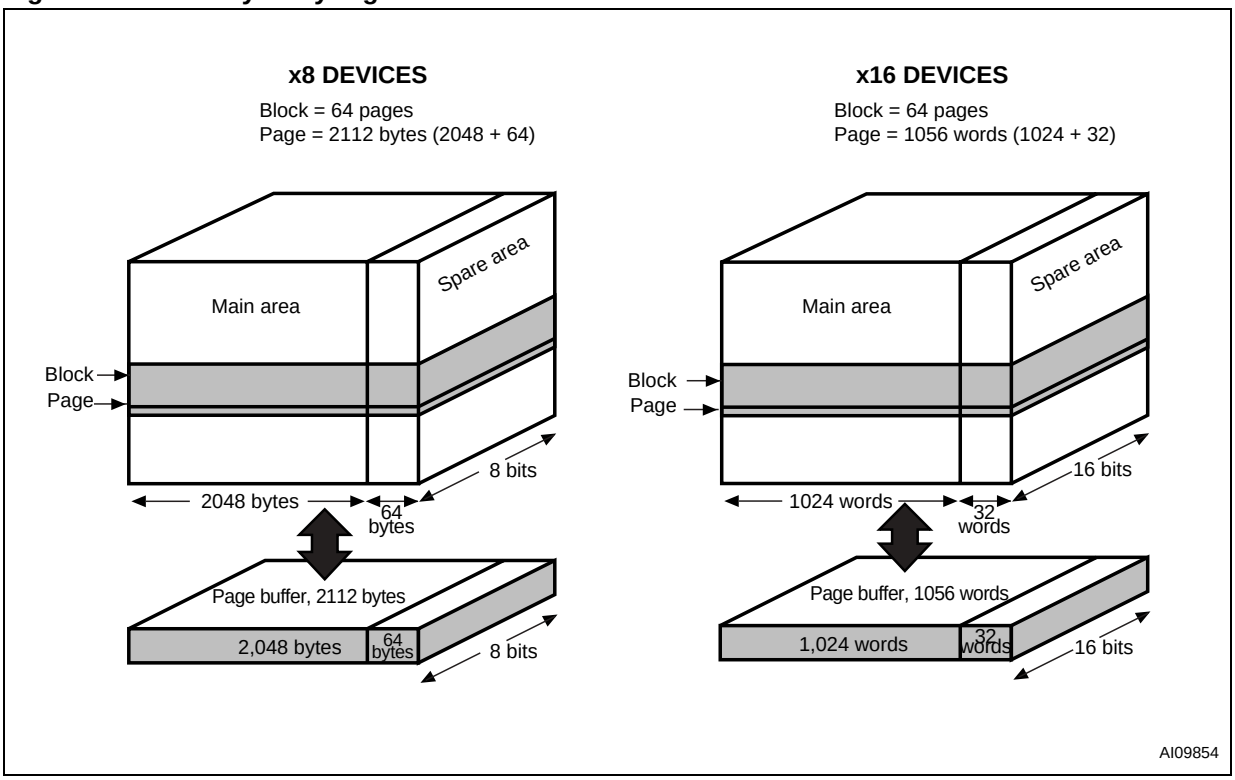
Table 4: Valid blocks shows the minimum number of valid blocks in the device. The values shown include both the bad blocks that are present when the device is shipped and the bad blocks that could develop later on.

These blocks need to be managed using bad blocks management, block replacement or error correction codes (refer to *Section 8: Software algorithms*).

Table 4. Valid blocks

Density of device	Min	Max
1 Gbit	1004	1024

Figure 6. Memory array organization



3 Signal descriptions

See *Figure 2: Logic diagram*, and *Table 3: Signal names*, for a brief overview of the signals connected to this device.

3.1 Inputs/outputs (I/O0-I/O7)

Input/outputs 0 to 7 are used to input the selected address, output the data during a read operation or input a command or data during a write operation. The inputs are latched on the rising edge of Write Enable. I/O0-I/O7 are left floating when the device is deselected or the outputs are disabled.

3.2 Inputs/outputs (I/O8-I/O15)

Input/outputs 8 to 15 are only available in x16 devices. They are used to output the data during a read operation or input data during a write operation. Command and address inputs only require I/O0 to I/O7.

The inputs are latched on the rising edge of Write Enable. I/O8-I/O15 are left floating when the device is deselected or the outputs are disabled.

3.3 Address Latch Enable (AL)

The Address Latch Enable activates the latching of the address inputs in the command interface. When AL is High, the inputs are latched on the rising edge of Write Enable.

3.4 Command Latch Enable (CL)

The Command Latch Enable activates the latching of the command inputs in the command interface. When CL is High, the inputs are latched on the rising edge of Write Enable.

3.5 Chip Enable ($\overline{E}$)

The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is Low, V_{IL}, the device is selected. If Chip Enable goes High, V_{IH}, while the device is busy, the device remains selected and does not go into standby mode.

3.6 Read Enable ($\overline{R}$)

The Read Enable pin, $\overline{R}$, controls the sequential data output during read operations. Data is valid t_{RLQV} after the falling edge of $\overline{R}$. The falling edge of $\overline{R}$ also increments the internal column address counter by one.

3.7 Write Enable ($\overline{W}$)

The Write Enable input, $\overline{W}$, controls writing to the command interface, input address and data latches. Both addresses and data are latched on the rising edge of Write Enable.

During power-up and power-down a recovery time of 10 µs (min) is required before the command interface is ready to accept a command. It is recommended to keep Write Enable High during the recovery time.

3.8 Write Protect ($\overline{WP}$)

The Write Protect pin is an input that gives a hardware protection against unwanted program or erase operations. When Write Protect is Low, V_{IL}, the device does not accept any program or erase operations.

It is recommended to keep the Write Protect pin Low, V_{IL}, during power-up and power-down.

3.9 Ready/Busy ($R\overline{B}$)

The Ready/Busy output, $R\overline{B}$, is an open-drain output that can be used to identify if the P/E/R controller is currently active. When Ready/Busy is Low, V_{OL}, a read, program or erase operation is in progress. When the operation completes Ready/Busy goes High, V_{OH}.

The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A Low will then indicate that one, or more, of the memories is busy.

Refer to the *Section 11.1: Ready/Busy signal electrical characteristics* for details on how to calculate the value of the pull-up resistor.

During power-up and power-down a minimum recovery time of 10 µs is required before the command interface is ready to accept a command. During this period the $R\overline{B}$ signal is Low, V_{OL}.

3.10 V_{DD} supply voltage

V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (read, program and erase).

An internal voltage detector disables all functions whenever V_{DD} is below V_{LKO} (see *Table 22* and *Table 23*) to protect the device from any involuntary program/erase during power-transitions.

Each device in a system should have V_{DD} decoupled with a 0.1 µF capacitor. The PCB track widths should be sufficient to carry the required program and erase currents.

3.11 V_{SS} ground

Ground, V_{SS}, is the reference for the power supply. It must be connected to the system ground.

4 Bus operations

There are six standard bus operations that control the memory. Each of these is described in this section, see *Table 5: Bus operations*, for a summary.

Typically, glitches of less than 5 ns on Chip Enable, Write Enable and Read Enable are ignored by the memory and do not affect bus operations.

4.1 Command input

Command input bus operations are used to give commands to the memory. Commands are accepted when Chip Enable is Low, Command Latch Enable is High, Address Latch Enable is Low and Read Enable is High. They are latched on the rising edge of the Write Enable signal. For commands that start a modify operation (write/erase) the Write Protect pin must be High.

Only I/O0 to I/O7 are used to input commands.

See *Figure 21* and *Table 24* for details of the timings requirements.

4.2 Address input

Address input bus operations are used to input the memory addresses. Four bus cycles are required to input the addresses for 1-Gbit devices (refer to *Table 6* and *Table 7*, Address insertion).

The addresses are accepted when Chip Enable is Low, Address Latch Enable is High, Command Latch Enable is Low and Read Enable is High. They are latched on the rising edge of the Write Enable signal. For commands that start a modify operation (write/erase) the Write Protect pin must be High. Only I/O0 to I/O7 are used to input addresses.

See *Figure 22* and *Table 24* for details of the timings requirements.

4.3 Data input

Data input bus operations are used to input the data to be programmed.

Data is accepted only when Chip Enable is Low, Address Latch Enable is Low, Command Latch Enable is Low, Read Enable, and Write Protect is High. The data is latched on the rising edge of the Write Enable signal. The data is input sequentially using the Write Enable signal.

See *Figure 23* and *Table 24* and *Table 25* for details of the timings requirements.

4.4 Data output

Data output bus operations are used to read: the data in the memory array, the status register, the electronic signature and the unique identifier.

Data is output when Chip Enable is Low, Write Enable is High, Address Latch Enable is Low, and Command Latch Enable is Low. The data is output sequentially using the Read Enable signal.

See *Figure 24* and *Table 25* for details of the timings requirements.

4.5 Write Protect

Write Protect bus operations are used to protect the memory against program or erase operations. When the Write Protect signal is Low the device will not accept program or erase operations and so the contents of the memory array cannot be altered. The Write Protect signal is not latched by Write Enable to ensure protection even during power-up.

4.6 Standby

When Chip Enable is High the memory enters standby mode, the device is deselected, outputs are disabled and power consumption is reduced.

Table 5. Bus operations

Bus operation	$\overline{E}$	AL	CL	$\overline{R}$	$\overline{W}$	$\overline{WP}$	I/O0 - I/O7	I/O8 - I/O15(1)
Command input	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Rising	X(2)	Command	X
Address input	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Rising	X	Address	X
Data input	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Rising	V_{IH}	Data input	Data input
Data output	V_{IL}	V_{IL}	V_{IL}	Falling	V_{IH}	X	Data output	Data output
Write Protect	X	X	X	X	X	V_{IL}	X	X
Standby	V_{IH}	X	X	X	X	V_{IL}/V_{DD}	X	X

1. Only for x16 devices.
2. $\overline{WP}$ must be V_{IH} when issuing a program or erase command.

Table 6. Address insertion, x8 devices

Bus cycle(1)	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st	A7	A6	A5	A4	A3	A2	A1	A0
2nd	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A11	A10	A9	A8
3rd	A19	A18	A17	A16	A15	A14	A13	A12
4th	A27	A26	A25	A24	A23	A22	A21	A20

1. Any additional address input cycles will be ignored.

Table 7. Address insertion, x16 devices

Bus cycle(1)	I/O8-I/O15	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st	X	A7	A6	A5	A4	A3	A2	A1	A0
2nd	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A10	A9	A8
3rd	X	A18	A17	A16	A15	A14	A13	A12	A11
4th	X	A26	A25	A24	A23	A22	A21	A20	A19

1. Any additional address input cycles will be ignored.

Table 8. Address definitions, x8 devices

Address	Definition
A0 - A11	Column address
A12 - A17	Page address
A18 - A27	Block address

Table 9. Address definitions, x16 devices

Address	Definition
A0 - A10	Column address
A11 - A16	Page address
A17 - A26	Block address

5 Command set

All bus write operations to the device are interpreted by the command interface. The commands are input on I/O0-I/O7 and are latched on the rising edge of Write Enable when the Command Latch Enable signal is High. Device operations are selected by writing specific commands to the command register. The two-step command sequences for program and erase operations are imposed to maximize data security.

The commands are summarized in *Table 10: Commands*.

Table 10. Commands

Command	Bus write operations(1)				Commands accepted during busy
	1st cycle	2nd cycle	3rd cycle	4th cycle	
Read	00h	30h	–	–	
Random Data Output	05h	E0h	–	–	
Cache Read	00h	31h	–	–	
Exit Cache Read	3Fh	–	–	–	
Page Program (sequential input default)	80h	10h	–	–	
Random Data Input	85h	–	–	–	
Copy Back Program	00h	35h	85h	10h	
Block Erase	60h	D0h	–	–	
Reset	FFh	–	–	–	Yes
Read Electronic Signature	90h	–	–	–	
Read Status Register	70h	–	–	–	Yes
Read ONFI Parameter Page	ECh	–	–	–	

1. The bus cycles are only shown for issuing the codes. The cycles required to input the addresses or input/output data are not shown.

6 Device operations

The following section gives the details of the device operations.

6.1 Read memory array

At power-up the device defaults to read mode. To enter read mode from another mode the Read command must be issued, see *Table 10: Commands*.

Once a Read command is issued two types of operations are available: random read and page read.

6.1.1 Random read

Each time the Read command is issued the first read is random read.

6.1.2 Page read

After the first random read access, the page data (2112 bytes or 1056 words) is transferred to the page buffer in a time of t_{WHBH} (refer to *Table 25* for value). Once the transfer is complete the Ready/Busy signal goes High. The data can then be read out sequentially (from selected column address to last column address) by pulsing the Read Enable signal.

Alternatively, the user may check the transfer completion by issuing the Read Status Register command and checking SR6 by toggling $\overline{R}$. In the latter case, the device will keep on outputting the read status register until the 00h command is issued.

The device can output random data in a page, instead of the consecutive sequential data, by issuing a Random Data Output command.

The Random Data Output command can be used to skip some data during a sequential data output.

The sequential operation can be resumed by changing the column address of the next data to be output, to the address which follows the Random Data Output command.

The Random Data Output command can be issued as many times as required within a page.

The Random Data Output command is not accepted during cache read operations.

Figure 7. Read operations

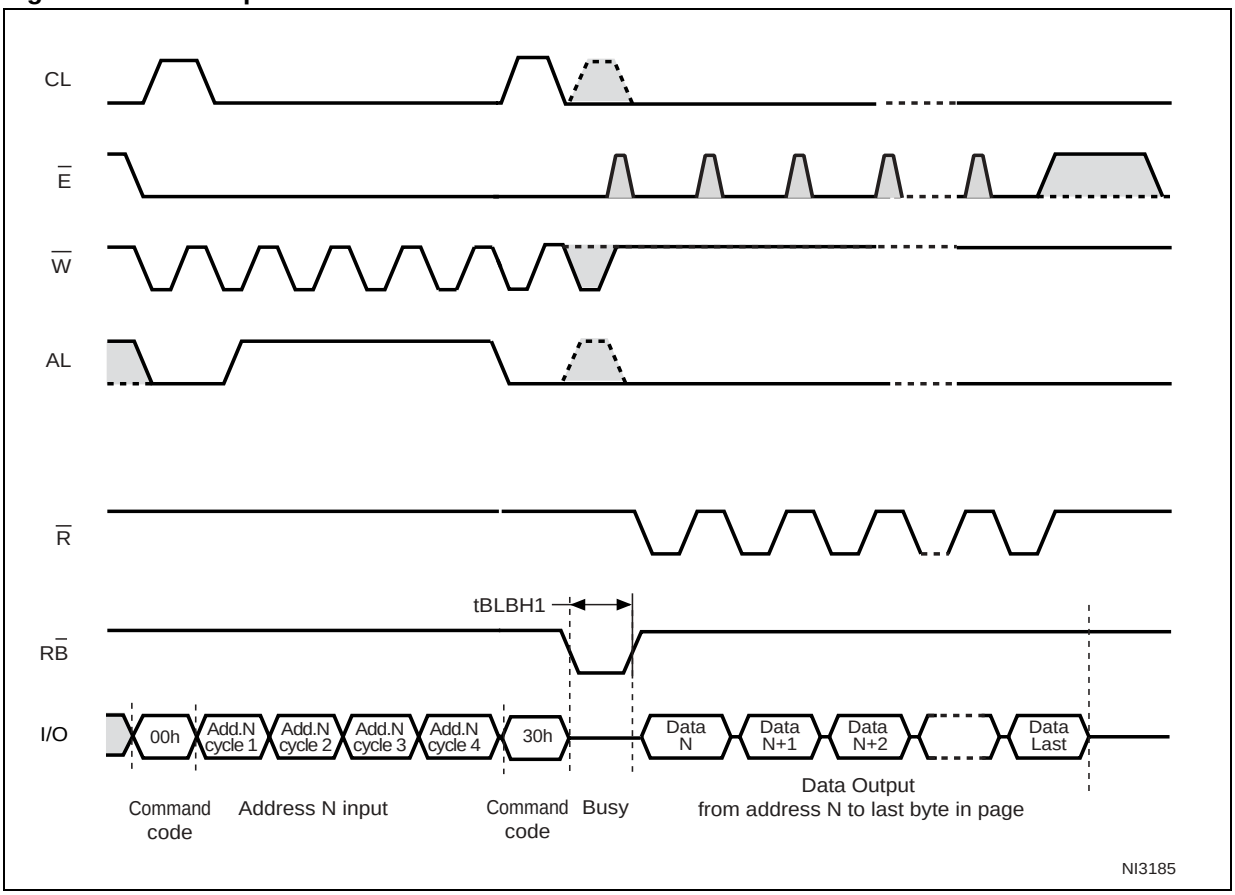


Figure 8. Read operations (intercepted by $\overline{E}$)

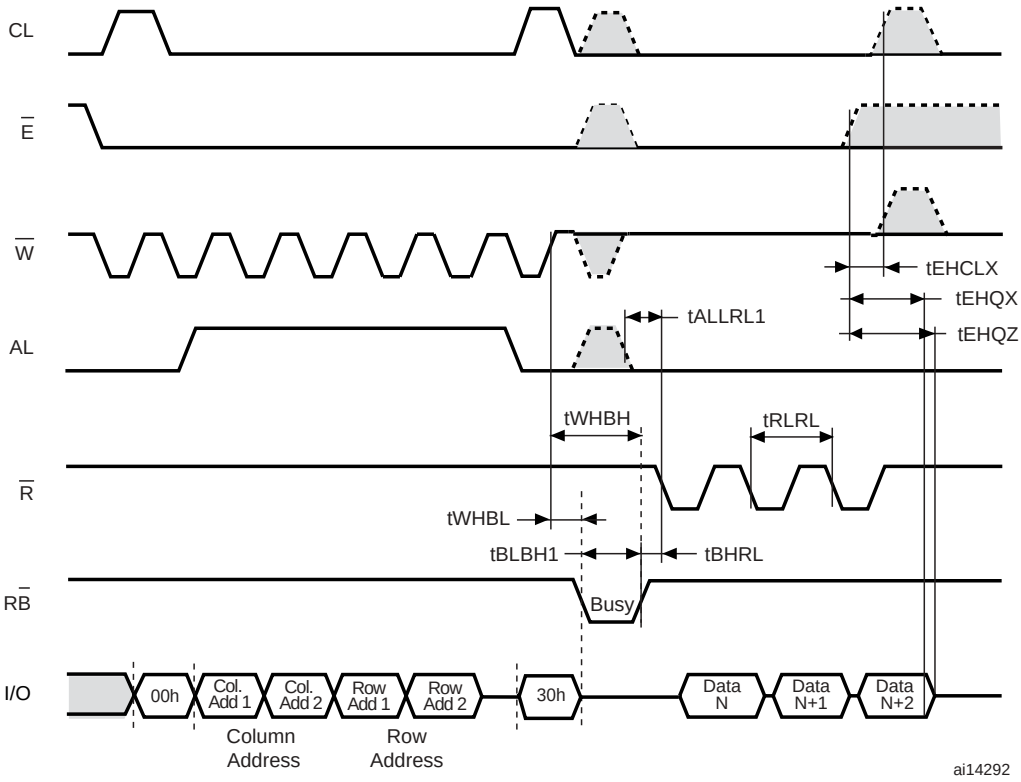
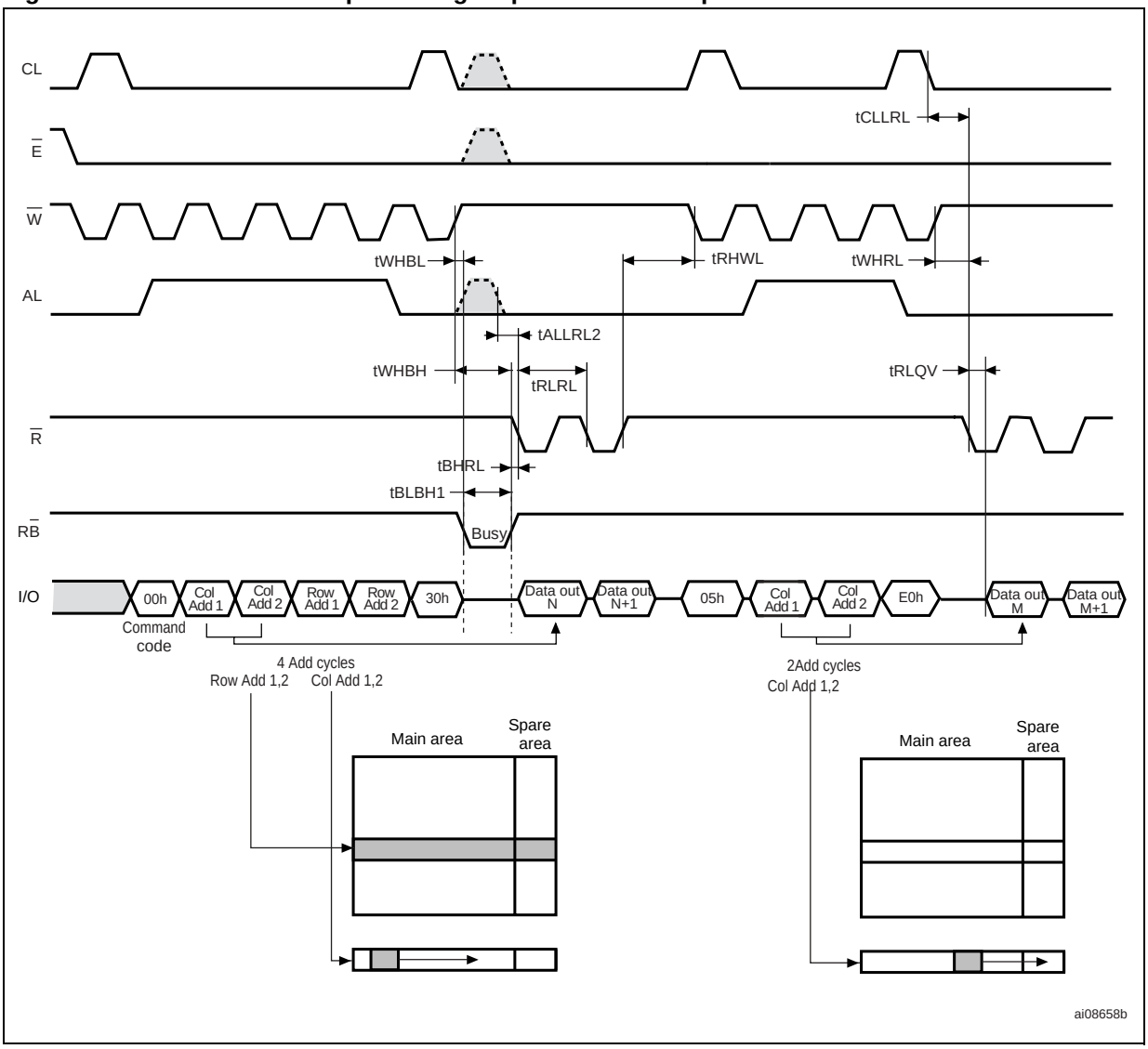


Figure 9. Random data output during sequential data output



6.2 Cache read

The cache read operation is used to improve the read throughput by reading data using the cache register. Since the device has only one cache register, serial data output on one page may be executed while data from another page is read into the cache register.

A Page Read command must be issued prior to the Sequential or Random Cache Read command in a cache read sequence. The Cache Read command can be issued only after the read function is complete (SR6 = ‘1’).

A cache read operation consists of three steps (see *Table 10: Commands*):

1. One bus cycle is required to setup the Cache Read command (the same as the standard Read command)
2. Four (refer to *Table 6* and *Table 7*) bus cycles are then required to input the start address. If the host does not enter an address, the next sequential page is read.
3. One bus cycle is required to issue the Cache Read Confirm command to start the P/E/R controller.

The start address must be at the beginning of a page (column address = 00h, see *Table 8* and *Table 9*). This allows the data to be output uninterrupted after the latency time (t_{BLBH1}), see *Figure 10*.

The Ready/Busy signal can be used to monitor the start of the operation. During the latency period the Ready/Busy signal goes Low, after this the Ready/Busy signal goes High, even if the device is internally downloading page n+1.

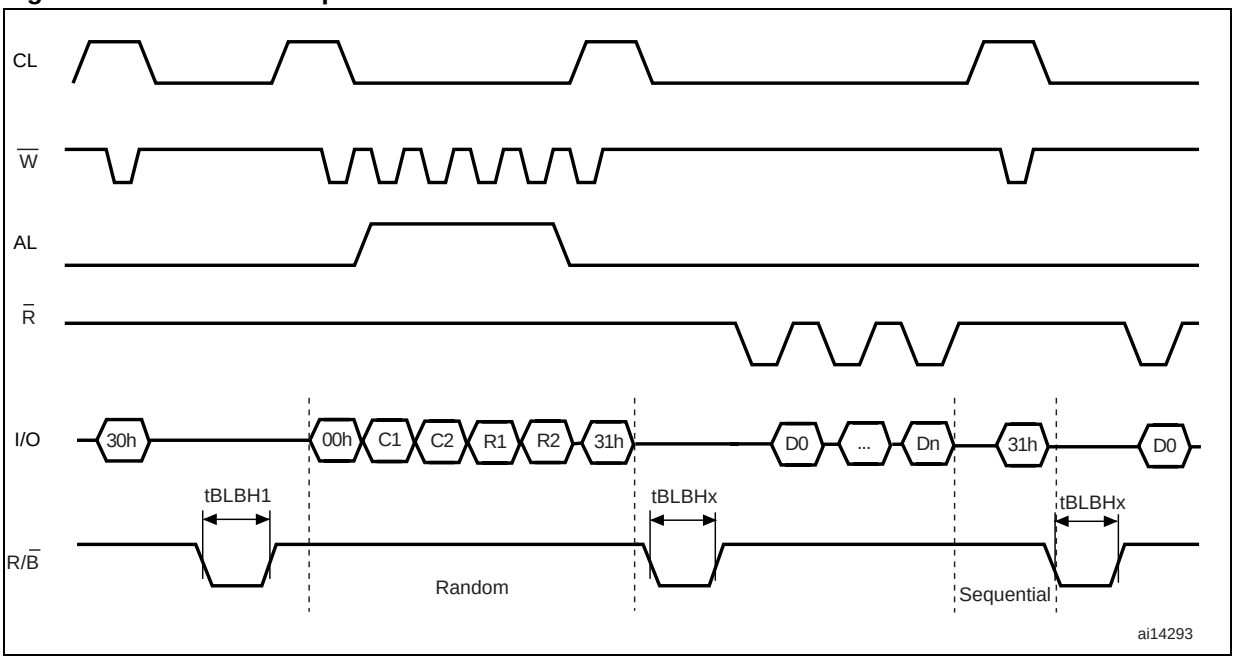
Once the cache read operation has started, the status register can be read using the Read Status Register command.

During the operation, SR5 can be read, to find out whether the internal reading is ongoing (SR5 = ‘0’), or has completed (SR5 = ‘1’), while SR6 indicates whether the cache register is ready to download new data.

To exit the cache read operation an Exit Cache Read command must be issued (see *Table 10*).

After the device has internally read page n, the user is allowed to download data of that page by toggling $\overline{R}$, but the device will not trigger internally the reading of a next page.

Figure 10. Cache read operation



6.3 Page program

The page program operation is the standard operation to program data to the memory array. Within a given block, the pages must be programmed sequentially. Random page address programming is not recommended.

The memory array is programmed by page, however partial page programming is allowed where any number of bytes (1 to 2112) or words (1 to 1056) can be programmed.

The maximum number of consecutive partial page program operations allowed in the same page is four. After exceeding this a Block Erase command must be issued before any further program operations can take place in that page.

6.3.1 Sequential input

To input data sequentially the addresses must be sequential and remain in one block.

For sequential input each page program operation consists of five steps (see *Figure 11*):

1. one bus cycle is required to setup the Page Program (sequential input) command (see *Table 10*)
2. four bus cycles are then required to input the program address (refer to *Table 6* and *Table 7*)
3. the data is then loaded into the data registers
4. one bus cycle is required to issue the Page Program Confirm command to start the P/E/R controller. The P/E/R will only start if the data has been loaded in step 3
5. the P/E/R controller then programs the data into the array.

6.3.2 Random data input in a page

During a sequential input operation, the next sequential address to be programmed can be replaced by a random address, by issuing a Random Data Input command. The following two steps are required to issue the command:

1. one bus cycle is required to setup the Random Data Input command (see *Table 10*)
2. two bus cycles are then required to input the new column address (refer to *Table 6*).

Random Data Input can be repeated as often as required in any given page.

Once the program operation has started the status register can be read using the Read Status Register command. During program operations the status register will only flag errors for bits set to '1' that have not been successfully programmed to '0'.

During the program operation, only the Read Status Register and Reset commands will be accepted, all other commands will be ignored.

Once the program operation has completed the P/E/R controller bit SR6 is set to ‘1’ and the Ready/Busy signal goes High.

The device remains in read status register mode until another valid command is written to the command interface.

Figure 11. Page program operation

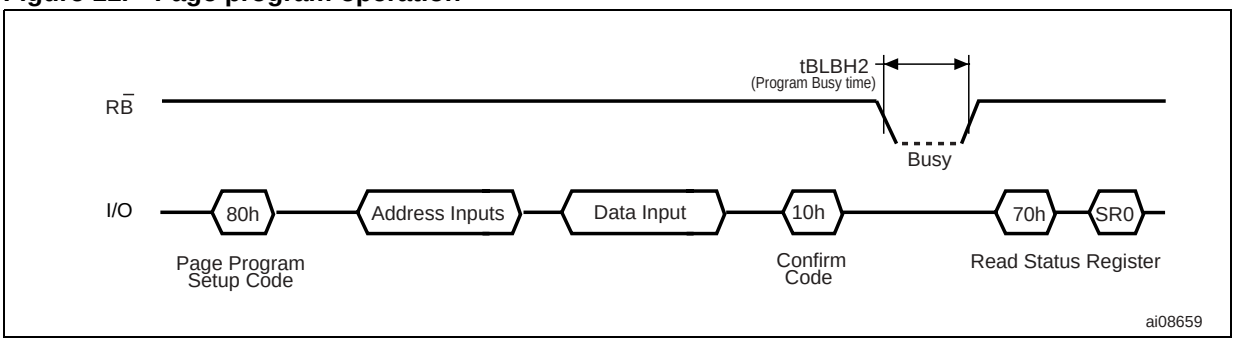
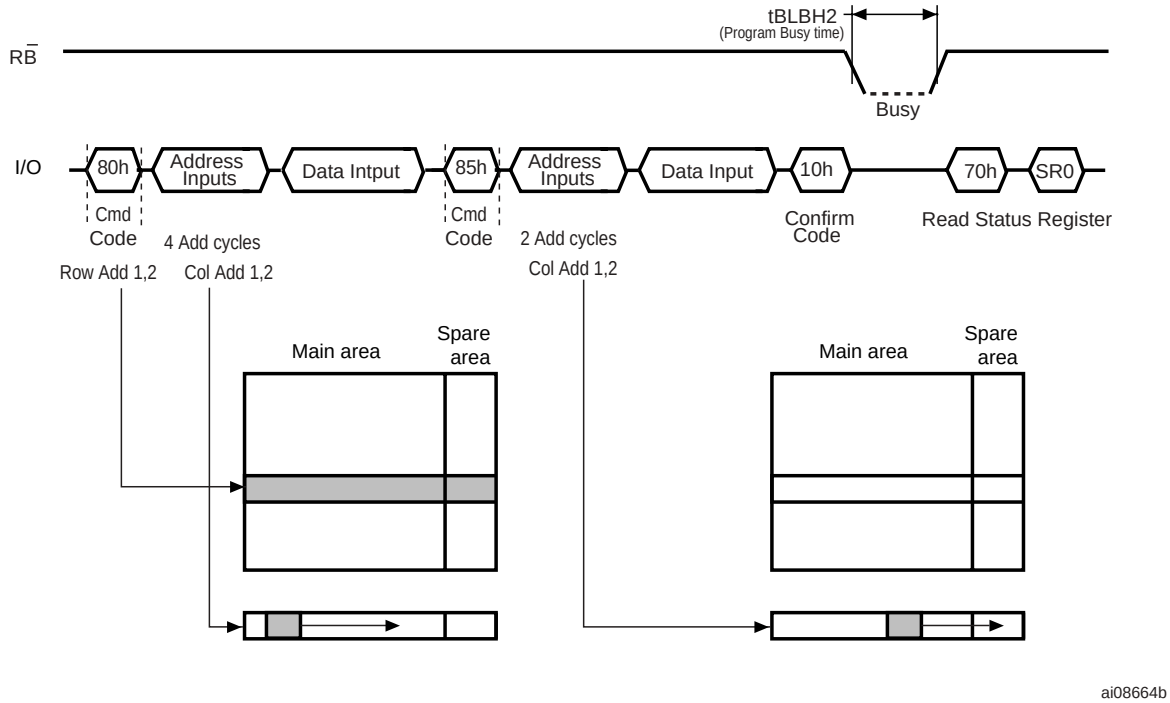


Figure 12. Random data input during sequential data input



6.4 Copy back program

The copy back program operation is used to copy the data stored in one page and reprogram it in another page.

The copy back program operation does not require external memory and so the operation is faster and more efficient because the reading and loading cycles are not required. The operation is particularly useful when a portion of a block is updated and the rest of the block needs to be copied to the newly assigned block.

If the copy back program operation fails, an error is signalled by the pass/fail status. However, if copy back operations are accumulated over time, a bit error due to charge loss is not checked by an external error detection/correction scheme. For this reason it is recommended to use a 2-bit error correction in a copy back operation.

The copy back program operation requires four steps:

1. The first step reads the source page. The operation copies all 1056 words/ 2112 bytes from the page into the data buffer. It requires:
   - one bus write cycle to setup the command
   - 4 bus write cycles to input the source page address (see *Table 6* and *Table 7*)
   - one bus write cycle to issue the confirm command code
2. When the device returns to the ready state (Ready/Busy High), the user may read the contents of the source page by toggling $\overline{R}$. In this case, random data output is also allowed. To proceed with the copy back of the page into the target location, the user will issue 85h followed by 4 bus cycles to input the target page address (see *Table 6* and *Table 7*).
3. Then the confirm command is issued to start the P/E/R controller.

For an example of the copy back program operation, refer to *Figure 13*, while *Figure 14* shows an example of Copy Back Program with Random Data Input.

A data input cycle to modify a portion or a multiple distant portion of the source page, is shown in *Figure 14*.

Figure 13. Copy back program

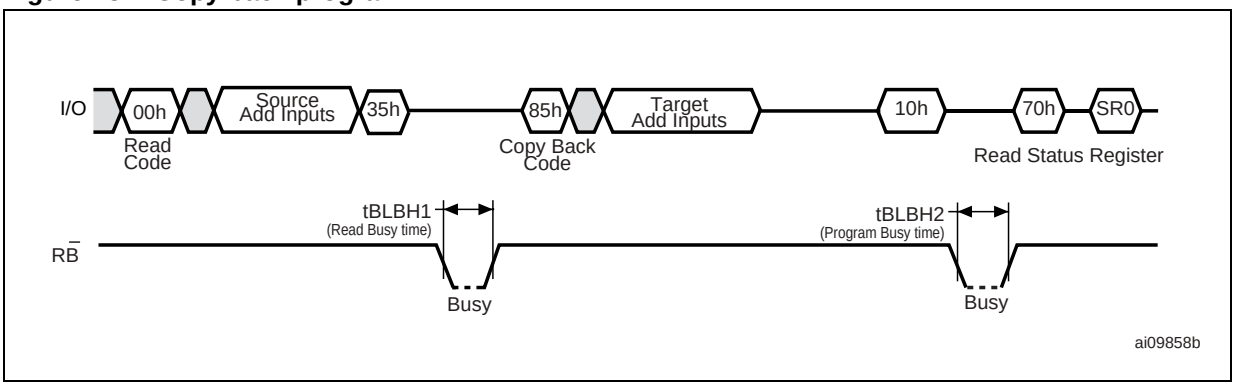
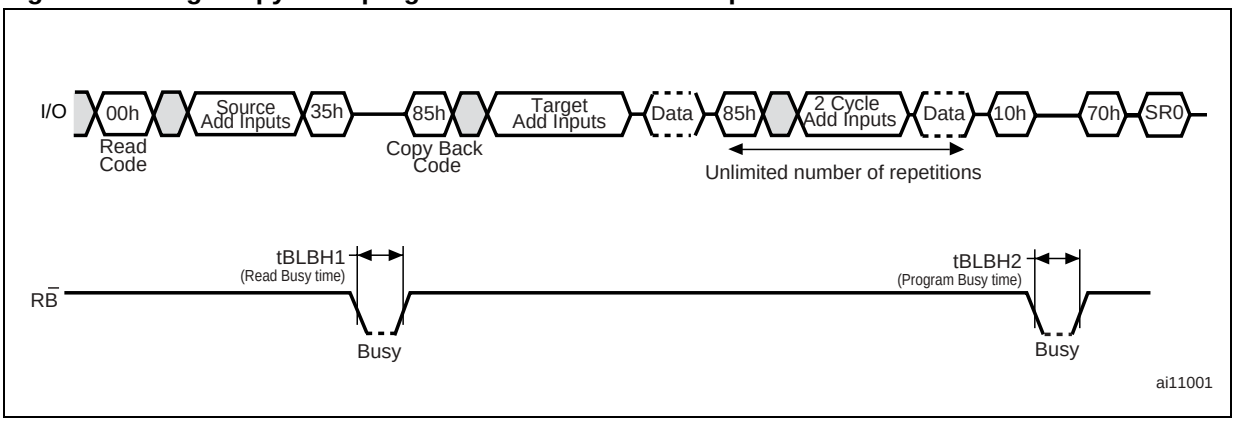


Figure 14. Page copy back program with random data input



6.5 Block erase

Erase operations are done one block at a time. An erase operation sets all of the bits in the addressed block to ‘1’. All previous data in the block is lost.

An erase operation consists of three steps (refer to *Figure 15*):

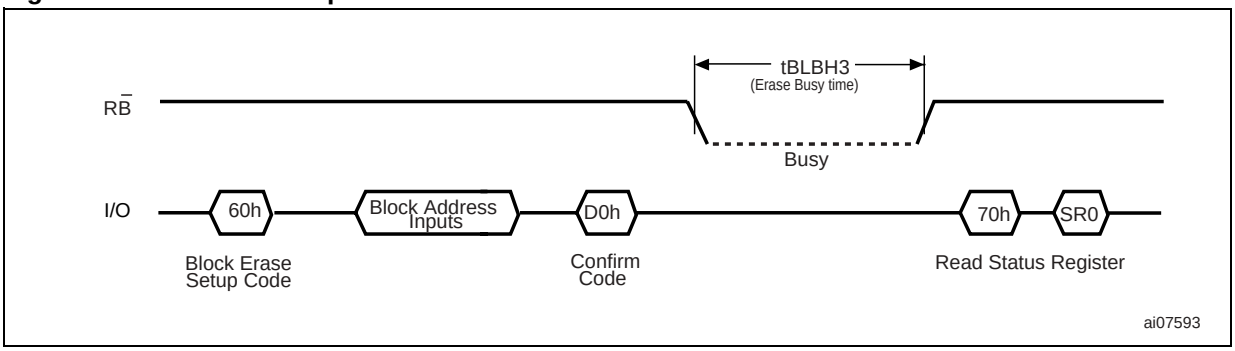
1. One bus cycle is required to setup the Block Erase command. Only addresses A18-A27 (x8) or A17-A26 (x16) are used, the other address inputs are ignored
2. Two bus cycles are then required to load the address of the block to be erased. Refer to *Table 8* and *Table 9* for the block addresses of each device
3. One bus cycle is required to issue the Block Erase Confirm command to start the P/E/R controller.

The operation is initiated on the rising edge of write Enable, $\overline{W}$, after the Confirm command is issued. The P/E/R controller handles block erase and implements the verify process.

During the block erase operation, only the Read Status Register and Reset commands will be accepted, all other commands will be ignored.

Once the program operation has completed the P/E/R controller bit SR6 is set to ‘1’ and the Ready/Busy signal goes High. If the operation completed successfully, the write status bit SR0 is ‘0’, otherwise it is set to ‘1’.

Figure 15. Block erase operation



6.6 Reset

The Reset command is used to reset the command interface and status register. If the Reset command is issued during any operation, the operation will be aborted. If it was a program or erase operation that was aborted, the contents of the memory locations being modified will no longer be valid as the data will be partially programmed or erased.

If the device has already been reset then the new Reset command will not be accepted.

The Ready/Busy signal goes Low for t_{BLBH4} after the Reset command is issued. The value of t_{BLBH4} depends on the operation that the device was performing when the command was issued, refer to *Table 25: AC characteristics for operations* for the values.

6.7 Read status register

The device contains a status register which provides information on the current or previous program or erase operation. The various bits in the status register convey information and errors on the operation.

The status register is read by issuing the Read Status Register command. The status register information is present on the output data bus (I/O0-I/O7) on the falling edge of Chip Enable or Read Enable, whichever occurs last. When several memories are connected in a system, the use of Chip Enable and Read Enable signals allows the system to poll each device separately, even when the Ready/Busy pins are common-wired. It is not necessary to toggle the Chip Enable or Read Enable signals to update the contents of the status register.

After the Read Status Register command has been issued, the device remains in read status register mode until another command is issued. Therefore if a Read Status Register command is issued during a random read cycle a new Read command must be issued to continue with a page read operation.

The Status Register bits are summarized in *Table 11: Status register bits*,. Refer to *Table 11* in conjunction with the following text descriptions.

6.7.1 Write protection bit (SR7)

The write protection bit can be used to identify if the device is protected or not. If the write protection bit is set to ‘1’ the device is not protected and program or erase operations are allowed. If the write protection bit is set to ‘0’ the device is protected and program or erase operations are not allowed.

6.7.2 P/E/R controller and cache ready/busy bit (SR6)

Status register bit SR6 has two different functions depending on the current operation.

During cache read operations SR6 indicates whether the next selected page can be read from the page register (SR6 is set to '1') or not (SR6 is set to '0').

During all other operations SR6 acts as a P/E/R controller bit, which indicates whether the P/E/R controller is active or inactive. When the P/E/R controller bit is set to ‘0’, the P/E/R controller is active (device is busy); when the bit is set to ‘1’, the P/E/R controller is inactive (device is ready).

6.7.3 P/E/R controller bit (SR5)

The program/erase/read controller bit indicates whether the P/E/R controller is active or inactive. When the P/E/R controller bit is set to ‘0’, the P/E/R controller is active (device is busy); when the bit is set to ‘1’, the P/E/R controller is inactive (device is ready).

6.7.4 Error bit (SR0)

The error bit is used to identify if any errors have been detected by the P/E/R controller. The error bit is set to ’1’ when a program or erase operation has failed to write the correct data to the memory. If the error bit is set to ‘0’ the operation has completed successfully.

6.7.5 SR4, SR3, SR2, and SR1 are reserved

Table 11. Status register bits

Bit	Name	Logic level	Definition
SR7	Write protection	'1'	Not protected
		'0'	Protected
SR6	Program/ erase/ read controller	'1'	P/E/R C inactive, device ready
		'0'	P/E/R C active, device busy
	Cache ready/busy	'1'	Cache register ready (cache operation only)
		'0'	Cache register busy (cache operation only)
SR5	Program/ erase/ read controller	'1'	P/E/R C inactive, device ready
		'0'	P/E/R C active, device busy
SR4, SR3, SR2, SR1	Reserved	Don’t care	
SR0	Generic error	‘1’	Error – operation failed
		‘0’	No error – operation successful

6.8 Read electronic signature

The device contains a manufacturer code and device code. To read these codes three steps are required:

1. One bus write cycle to issue the Read Electronic Signature command (90h)
2. One bus write cycle to input the address (00h)
3. Four bus read cycles to sequentially output the data (as shown in *Table 12: Electronic signature*).

Table 12. Electronic signature

Part number	byte/word 1	byte/word 2	byte/word 3 (see *Table 13*)	byte/word 4 (see *Table 14*)
	Manufacturer code	Device code		
NAND01GR3B2C	20h	A1h	00h	15h
NAND01GW3B2C		F1h		1Dh
NAND01GR4B2C		B1h		55h
NAND01GW4B2C		C1h		5Dh

Table 13. Electronic signature byte 3

I/O	Definition	Value	Description
I/O1-I/O0	Internal chip number	0 0 0 1 1 0 1 1	1 2 4 Reserved
I/O3-I/O2	Cell type	0 0 0 1 1 0 1 1	Single level cell 2x multilevel cell Reserved Reserved
I/O5-I/O4	Number of simultaneously programmed pages	0 0 0 1 1 0 1 1	1 2 3 4
I/O6	Interleaved programming between multiple devices	0 1	Not supported Supported
I/O7	Cache program	0 1	Not supported Supported

Table 14. Electronic signature byte/word 4

I/O	Definition	Value	Description
I/O1-I/O0	Page size (without spare area)	0 0 0 1 1 0 1 1	1 Kbyte 2 Kbytes Reserved Reserved
I/O2	Spare area size (byte / 512-byte)	0 1	8 16
I/O3	Minimum sequential access time	0 1	50 ns 30 ns
I/O5-I/O4	Block size (without spare area)	0 0 0 1 1 0 1 1	64 Kbytes 128 Kbytes 256 Kbytes Reserved
I/O6	Organization	0 1	x8 x16
I/O7	Not used		Reserved

6.9 Read ONFI signature

To recognize NAND flash devices that are compatible with ONFI 1.0 command set, the Read Electronic Signature command can be issued, followed by an address of 20h. The next four-byte output is the ONFI signature, which is the ASCII encoding of the ‘ONFI’ word.

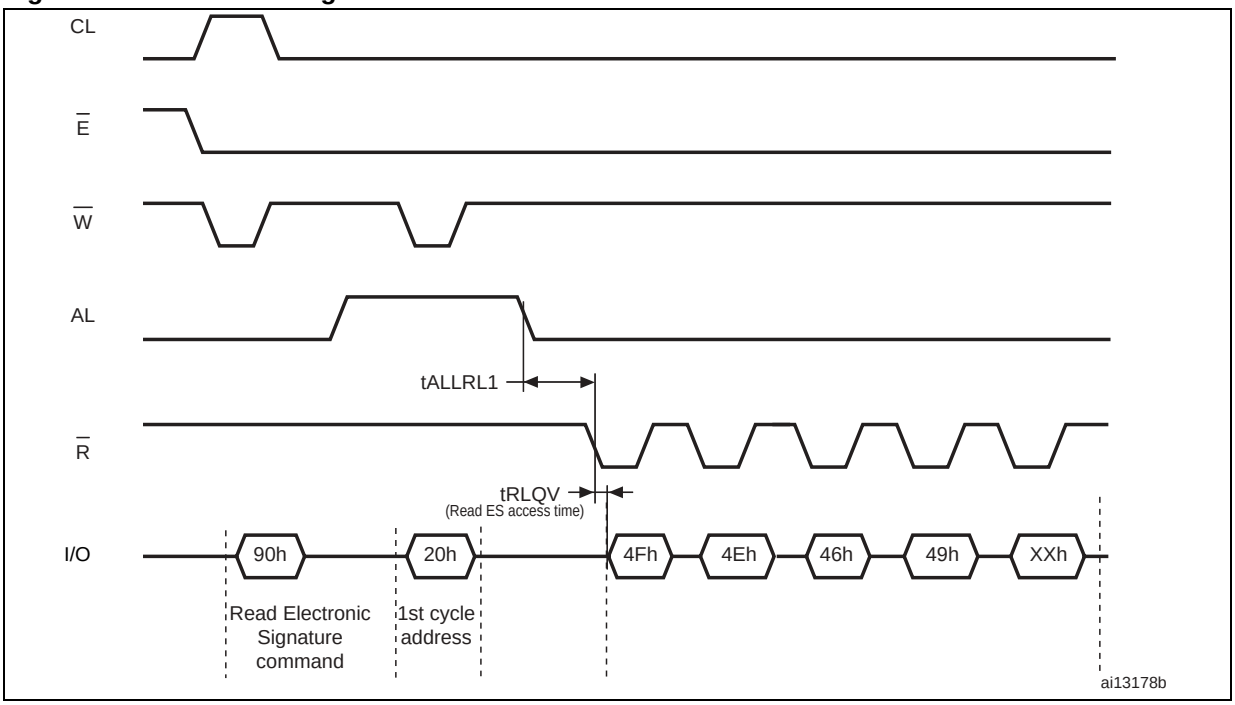
Reading beyond four bytes produces indeterminate values. The device remains in this state until a new command is issued.

Figure 16 describes the read ONFI signature waveforms and *Table 15* defines the output bytes.

Table 15. Read ONFI signature

Byte	Value	ASCII character
1st byte	4Fh	O
2nd byte	4Eh	N
3rd byte	46h	F
4th byte	49h	I
5th byte	Undefined	Undefined

Figure 16. Read ONFI signature waveforms



6.10 Read parameter page

The Read Parameter Page command retrieves the data structure that describes the NAND flash organization, features, timings and other behavioral parameters. This data structure enables the host processor to automatically recognize the NAND flash configuration of a device. The whole data structure is repeated at least five times.

See *Figure 17* for a description of the read parameter page waveforms.

The Random Data Read command can be issued during execution of the read parameter page to read specific portions of the parameter page.

The Read Status command may be used to check the status of read parameter page during execution. After completion of the Read Status command, 00h is issued by the host on the command line to continue with the data output flow for the Read Parameter Page command.

Read status enhanced is not be used during execution of the Read Parameter Page command.

Table 16 defines the parameter page data structure. For parameters that span multiple bytes, the least significant byte of the parameter corresponds to the first byte.

Values are reported in the parameter page in bytes when referring to items related to the size of data access (as in an x8 data access device). For example, the chip returns how many data bytes are in a page. For a device that supports x16 data access, the host is required to convert byte values to word values for its use. Unused fields are set to 0h.

For more detailed information about parameter page data bits, refer to ONFI Specification 1.0 section 5.4.1.

Figure 17. Read parameter page waveforms

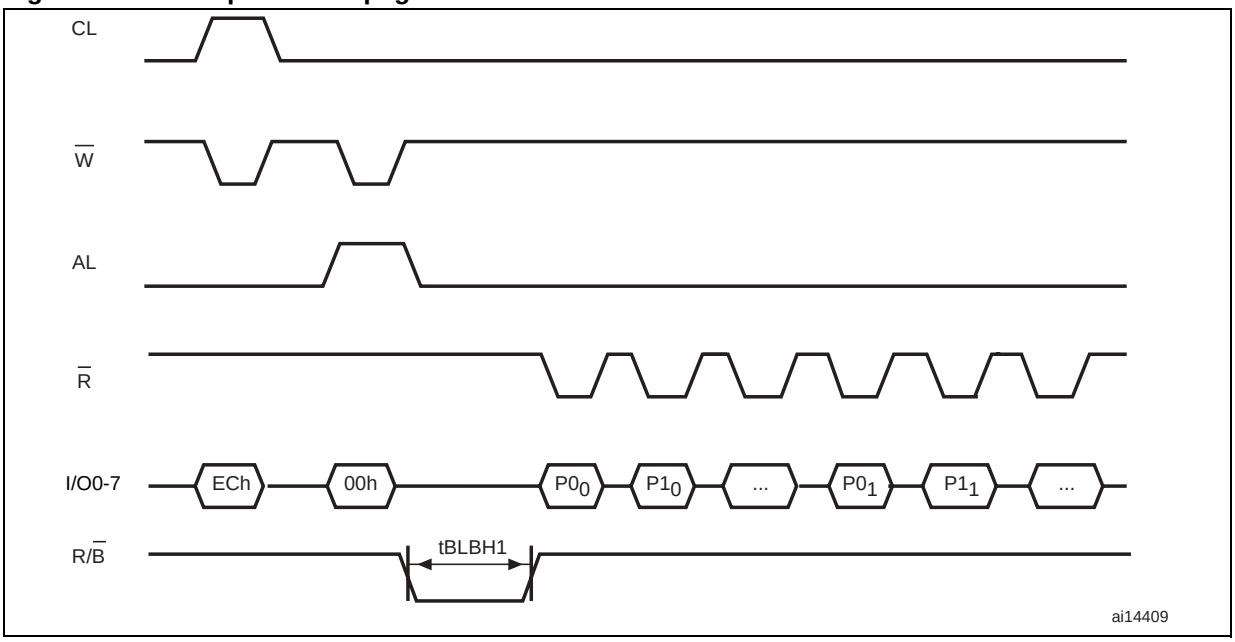


Table 16. Parameter page data structure

	Byte	O/M(1)	Description	
Revision information and features block	0-3	M	Parameter page signature – Byte 0: 4Fh, 'O' – Byte 1: 4Eh, 'N' – Byte 2: 46h, 'F' – Byte 3: 49h, 'I'	
	4-5	M	**Revision number**	
			Bit 2 to bit 15	Reserved (0)
			Bit 1	1 = supports ONFI version 1.0
			Bit 0	Reserved (0)
	6-7	M	**Features supported**	
			Bit 5 to bit 15	Reserved (0)
			Bit 4	1 = supports odd to even page copy back
			Bit 3	1 = supports interleaved operations
			Bit 2	1 = supports non-sequential page programming
			Bit 1	1 = supports multiple LUN operations
			Bit 0	1 = supports 16-bit data bus width
	8-9	M	**Optional commands supported**	
			Bit 6 to bit 15	Reserved (0)
			Bit 5	1 = supports read unique ID
			Bit 4	1 = supports copy back
			Bit 3	1 = supports read status enhanced
			Bit 2	1 = supports get features and set features
			Bit 1	1 = supports read cache commands
			Bit 0	1 = supports page cache program command
	10-31			Reserved (0)
Manufacturer information block	32-43	M	Device manufacturer (12 ASCII characters)	
	44-63	M	Device model (20 ASCII characters)	
	64	M	JEDEC manufacturer ID	
	65-66	O	Date code	
	67-79		Reserved (0)	

Table 16. Parameter page data structure (continued)

	Byte	O/M(1)	Description	
Memory organization block	80-83	M		Number of data bytes per page
	84-85	M		Number of spare bytes per page
	86-89	M		Number of data bytes per partial page
	90-91	M		Number of spare bytes per partial page
	92-95	M		Number of pages per block
	96-99	M		Number of blocks per logical unit (LUN)
	100	M		Number of logical units (LUNs)
	101	M	**Number of address cycles**	
			Bit 4 to bit 7	Column address cycles
			Bit 0 to bit 3	Row address cycles
	102	M		Number of bits per cell
	103-104	M		Bad blocks maximum per LUN
	105-106	M		Block endurance
	107	M		Guaranteed valid blocks at beginning of target
	108-109	M		Block endurance for guaranteed valid blocks
	110	M		Number of programs per page
	111	M	**Partial programming attributes**	
			Bit 5 to bit 7	Reserved
			4	1 = partial page layout is partial page data followed by partial page spare
			Bit 1 to bit 3	Reserved
			0	1 = partial page programming has constraints
	112	M		Number of bits ECC correctability
	113	M	**Number of interleaved address bits**	
			Bit 4 to bit 7	Reserved (0)
			Bit 0 to bit 3	Number of interleaved address bits
	114	O	**Interleaved operation attributes**	
			Bit 4 to bit 7	Reserved (0)
			Bit 3	Address restrictions for program cache
			Bit 2	1 = program cache supported
			Bit 1	1 = no block address restrictions
			Bit 0	Overlapped / concurrent interleaving support
	115-127			Reserved (0)

Table 16. Parameter page data structure (continued)

	Byte	O/M[1]	Description	
	128	M		I/O pin capacitance
Electrical parameter block	129-130	M	**Timing mode support**	
			Bit 6 to bit 15	Reserved (0)
			Bit 5	1 = supports timing mode 5
			Bit 4	1 = supports timing mode 4
			Bit 3	1 = supports timing mode 3
			Bit 2	1 = supports timing mode 2
			Bit 1	1 = supports timing mode 1
			Bit 0	1 = supports timing mode 0, shall be 1
	131-132	O	**Program cache timing mode support**	
			Bit 6 to bit 15	Reserved (0)
			Bit 5	1 = supports timing mode 5
			Bit 4	1 = supports timing mode 4
			Bit 3	1 = supports timing mode 3
			Bit 2	1 = supports timing mode 2
			Bit 1	1 = supports timing mode 1
			Bit 0	1 = supports timing mode 0
	133-134	M		t_{PROG} maximum page program time (µs)
	135-136	M		t_{BERS} maximum block erase time (µs)
	137-138	M		t_R maximum page read time (µs)
	139-140	M		t_{CCS} minimum change column setup time (ns)
	141-163	M		Reserved (0)
Vendor block	164-165	M		Vendor specific revision number
	166-253	M		Vendor specific
	254-255	M		Integrity CRC
Red. param. pages	256-511	M		Value of bytes 0-255
	512-767	M		Value of bytes 0-255
	768+	O		Additional redundant parameter pages

1. O = optional, M = mandatory.

7 Data protection

The device has hardware features to protect against program and erase operations.

It features a Write Protect, $\overline{WP}$, pin, which can be used to protect the device against program and erase operations. It is recommended to keep $\overline{WP}$ at V_{IL} during power-up and power-down.

In addition, to protect the memory from any involuntary program/erase operations during power-transitions, the device has an internal voltage detector which disables all functions whenever V_{DD} is below V_{LKO} (see *Table 22* and *Table 23*).

8 Software algorithms

This section gives information on the software algorithms that Numonyx recommends to implement to manage the bad blocks and extend the lifetime of the NAND device.

NAND flash memories are programmed and erased by Fowler-Nordheim tunneling using a high voltage. Exposing the device to a high voltage for extended periods can cause the oxide layer to be damaged. For this reason, the number of program and erase cycles is limited (see *Table 18* for value) and it is mandatory to implement error correction code algorithms to extend the number of program and erase cycles and increase data retention.

To help integrate a NAND memory into an application, Numonyx can provide a full range of software solutions: file system, sector manager, drivers and code management.

Contact the nearest Numonyx sales office or visit www.numonyx.com for more details.

8.1 Bad block management

Devices with bad blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A bad block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor.

The devices are supplied with all the locations inside valid blocks erased (FFh). The bad block information is written prior to shipping. Any block, where the 1st and 6th bytes (x8 device)/1st word (x16 device), in the spare area of the 1st page, does not contain FFh, is a bad block.

The bad block Information must be read before any erase is attempted as the bad block information may be erased. For the system to be able to recognize the bad blocks based on the original information it is recommended to create a bad block table following the flowchart shown in *Figure 18*.

8.2 NAND flash memory failure modes

Over the lifetime of the device additional bad blocks may develop.

To implement a highly reliable system, all the possible failure modes must be considered:

- **Program/erase failure:** in this case the block has to be replaced by copying the data to a valid block. These additional bad blocks can be identified as attempts to program or erase them will give errors in the status register
  As the failure of a page program operation does not affect the data in other pages in the same block, the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block. The Copy Back Program command can be used to copy the data to a valid block. See *Section 6.4: Copy back program* for more details
- **Read failure:** in this case, ECC correction must be implemented. To efficiently use the memory space, it is recommended to recover single-bit error in read by ECC, without replacing the whole block.

Refer to *Table 17* for the procedure to follow if an error occurs during an operation.

Table 17. NAND flash failure modes

Operation	Procedure
Erase	Block replacement
Program	Block replacement or ECC
Read	ECC

Figure 18. Bad block management flowchart

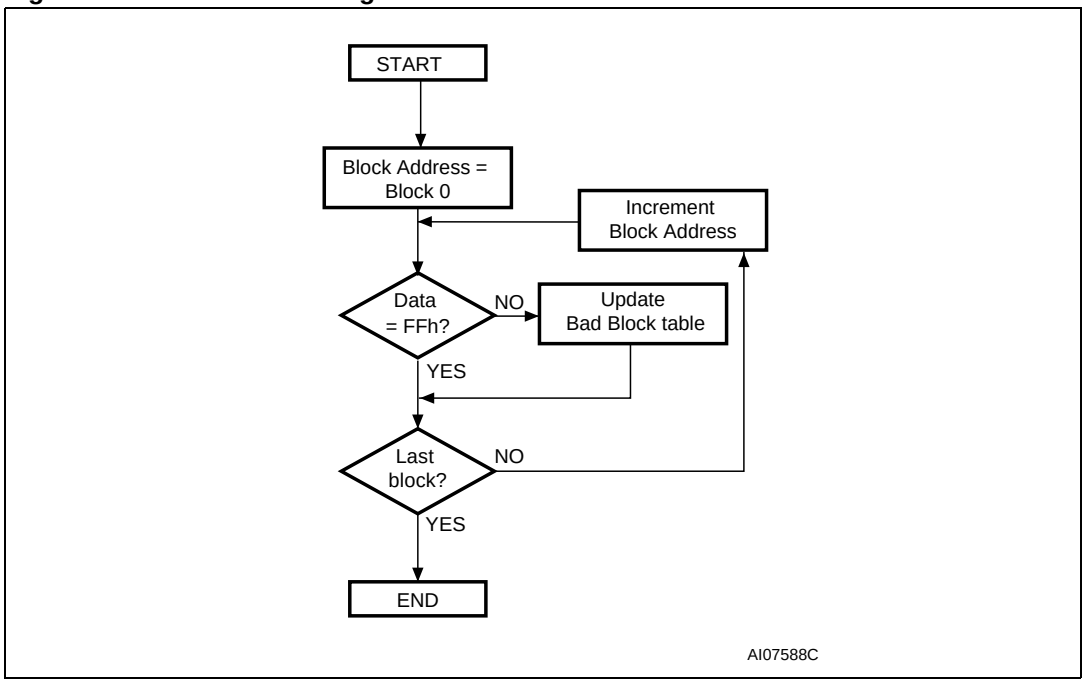
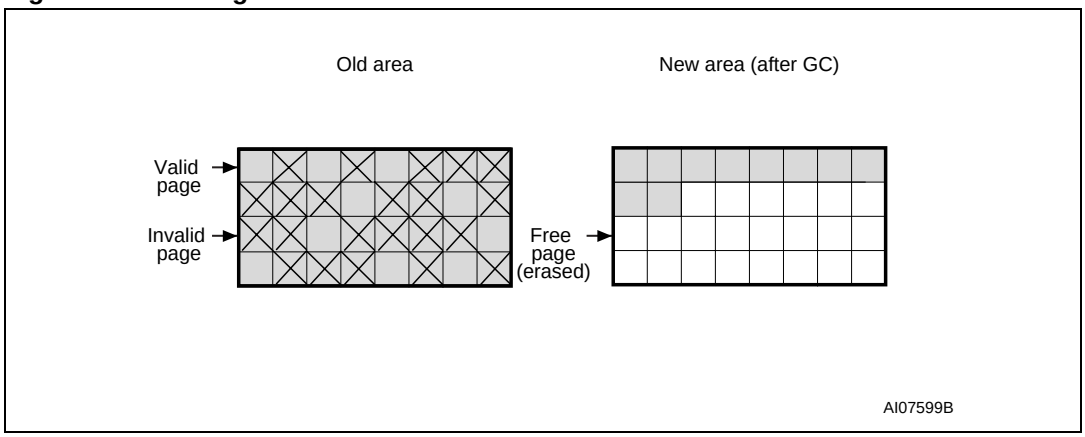


Figure 19. Garbage collection



8.3 Garbage collection

When a data page needs to be modified, it is faster to write to the first available page, and the previous page is marked as invalid. After several updates it is necessary to remove invalid pages to free some memory space.

To free this memory space and allow further program operations it is recommended to implement a garbage collection algorithm. In a garbage collection software the valid pages are copied into a free area and the block containing the invalid pages is erased (see *Figure 19*).

8.4 Wear-leveling algorithm

For write-intensive applications, it is recommended to implement a wear-leveling algorithm to monitor and spread the number of write cycles per block.

In memories that do not use a wear-leveling algorithm not all blocks get used at the same rate. Blocks with long-lived data do not endure as many write cycles as the blocks with frequently-changed data.

The wear-leveling algorithm ensures that equal use is made of all the available write cycles for each block. There are two wear-leveling levels:

- First level wear-leveling, new data is programmed to the free blocks that have had the fewest write cycles
- Second level wear-leveling, long-lived data is copied to another block so that the original block can be used for more frequently-changed data.

The second level wear-leveling is triggered when the difference between the maximum and the minimum number of write cycles per block reaches a specific threshold.

8.5 Error correction code

Users must implement an error correction code (ECC) to identify and correct errors in data stored in NAND flash memories. The ECC implemented must be able to correct 1 bit every 512 bytes. Sensible data stored in spare area must be covered by ECC as well.

8.6 Hardware simulation models

8.6.1 Behavioral simulation models

Denali Software Corporation models are platform independent functional models designed to assist customers in performing entire system simulations (typical VHDL/Verilog). These models describe the logic behavior and timings of NAND flash devices, and so allow software to be developed before hardware.

8.6.2 IBIS simulation models

IBIS (I/O buffer information specification) models describe the behavior of the I/O buffers and electrical characteristics of flash devices.

These models provide information such as AC characteristics, rise/fall times and package mechanical data, all of which are measured or simulated at voltage and temperature ranges wider than those allowed by target specifications.

IBIS models are used to simulate PCB connections and can be used to resolve compatibility issues when upgrading devices. They can be imported into SPICETOOLS.

9 Program and erase times and endurance cycles

The program and erase times and the number of program/erase cycles per block are shown in *Table 18*.

Table 18. Program, erase times and program erase endurance cycles

Parameters	NAND flash			Unit
	Min	Typ	Max	
Page program time		200	700	µs
Block erase time		2	3	ms
Program/erase cycles per block (with ECC)	100,000			cycles
Data retention	10			years

10 Maximum ratings

Stressing the device above the ratings listed in *Table 19: Absolute maximum ratings*, may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 19. Absolute maximum ratings

Symbol	Parameter		Value		Unit
			Min	Max	
T_{BIAS}	Temperature under bias		– 50	125	°C
T_{STG}	Storage temperature		– 65	150	°C
V_{IO}(1)	Input or output voltage	1.8 V devices	– 0.6	2.7	V
		3 V devices	– 0.6	4.6	V
V_{DD}	Supply voltage	1.8 V devices	– 0.6	2.7	V
		3 V devices	– 0.6	4.6	V

1. Minimum voltage may undershoot to –2 V for less than 20 ns during transitions on input and I/O pins. Maximum voltage may overshoot to V_{DD} + 2 V for less than 20 ns during transitions on I/O pins.

11 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables that follow, are derived from tests performed under the measurement conditions summarized in *Table 20: Operating and AC measurement conditions*. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 20. Operating and AC measurement conditions

Parameter		NAND flash		Units
		Min	Max	
Supply voltage (V_{DD})	1.8 V devices	1.7	1.95	V
	3 V devices	2.7	3.6	V
Ambient temperature (T_A)	Grade 1	0	70	°C
	Grade 6	–40	85	°C
Load capacitance (C_L) (1 TTL GATE and C_L)	1.8 V devices	30		pF
	3 V devices (2.7 - 3.6 V)	50		pF
Input pulses voltages	1.8 V devices	0	V_{DD}	V
	3 V devices	0	V_{DD}	V
Input and output timing ref. voltages		$V_{DD}/2$		V
Output circuit resistor R_{ref}		8.35		kΩ
Input rise and fall times		5		ns

Table 21. Capacitance(1)

Symbol	Parameter	Test condition	Typ	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V		10	pF
$C_{I/O}$	Input/output capacitance(2)	V_{IL} = 0 V		10	pF

1. T_A = 25 °C, f = 1 MHz. C_{IN} and $C_{I/O}$ are not 100% tested.
2. Input/output capacitances double in stacked devices.

Figure 20. Equivalent testing circuit for AC characteristics measurement

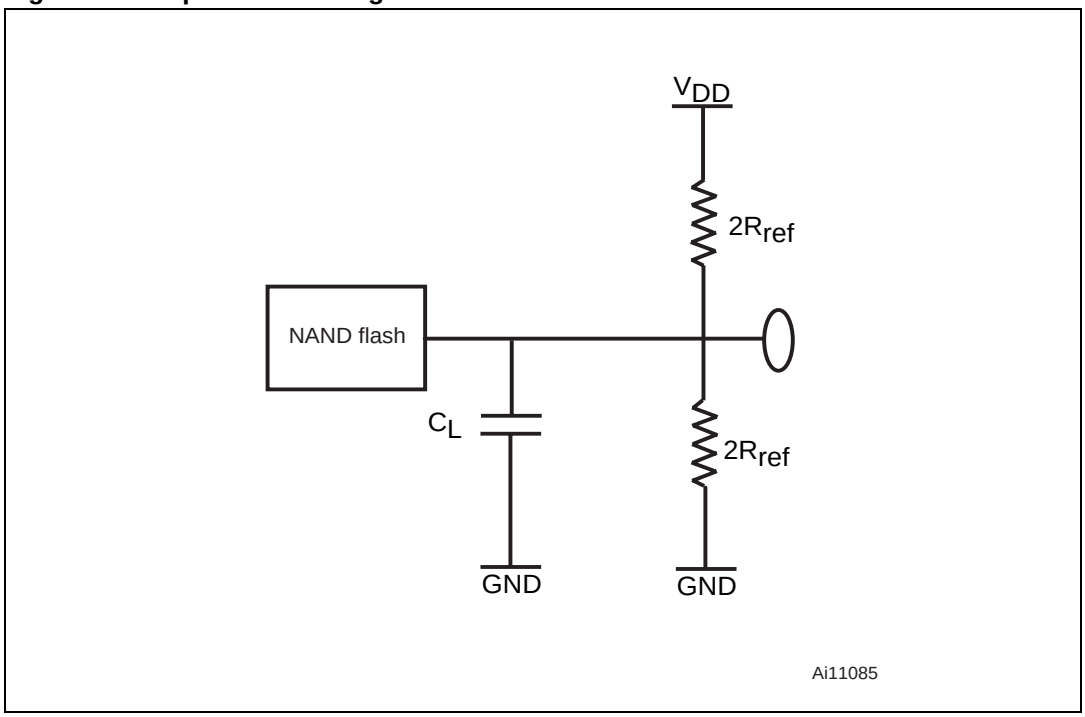


Table 22. DC characteristics, 1.8 V devices

Symbol	Parameter		Test conditions	Min	Typ	Max	Unit
I_{DD1}	Operating current	Sequential read	$\overline{E}$ = V_{IL}, I_{OUT} = 0 mA, t_{RLRL} minimum	–	10	20	mA
I_{DD2}		Program	–	–	10	20	mA
I_{DD3}		Erase	–	–	10	20	mA
I_{DD5}	Standby current (CMOS)(1)		$\overline{E}$ = V_{DD} – 0.2, $\overline{WP}$ = 0/V_{DD}	–	10	50	µA
I_{LI}	Input leakage current(1)		V_{IN} = 0 to V_{DD}max	–	–	±10	µA
I_{LO}	Output leakage current(1)		V_{OUT} = 0 to V_{DD}max	–	–	±10	µA
V_{IH}	Input high voltage		–	0.8xV_{DD}	–	V_{DD} + 0.3	V
V_{IL}	Input low voltage		–	-0.3	–	0.2xV_{DD}	V
V_{OH}	Output high voltage level		I_{OH} = –100 µA	V_{DD} - 0.1	–	–	V
V_{OL}	Output low voltage level		I_{OL} = 100 µA	–	–	0.1	V
I_{OL} ($R\overline{B}$)	Output low current ($R\overline{B}$)		V_{OL} = 0.1 V	3	4		mA
V_{LKO}	V_{DD} supply voltage (erase and program lockout)		–	–	1.1		V

1. Leakage current and standby current double in stacked devices.

Table 23. DC characteristics, 3 V devices

Symbol	Parameter		Test conditions	Min	Typ	Max	Unit
I_{DD1}	Operating current	Sequential Read	$\overline{E}$ = V_{IL}, I_{OUT} = 0 mA, t_{RLRL} minimum	–	15	30	mA
I_{DD2}		Program	–	–	15	30	mA
I_{DD3}		Erase	–	–	15	30	mA
I_{DD4}	Standby current (TTL)(1)		$\overline{E}$ = V_{IH}, $\overline{WP}$ = 0/V_{DD}			1	mA
I_{DD5}	Standby current (CMOS)(1)		$\overline{E}$ = V_{DD} – 0.2, $\overline{WP}$ = 0/V_{DD}	–	10	50	µA
I_{LI}	Input leakage current(1)		V_{IN} = 0 to V_{DD}max	–	–	±10	µA
I_{LO}	Output leakage current(1)		V_{OUT} = 0 to V_{DD}max	–	–	±10	µA
V_{IH}	Input high voltage		–	0.8xV_{DD}	–	V_{DD} + 0.3	V
V_{IL}	Input low voltage		–	-0.3	–	0.2xV_{DD}	V
V_{OH}	Output high voltage level		I_{OH} = –400 µA	2.4	–	–	V
V_{OL}	Output low voltage level		I_{OL} = 2.1 mA	–	–	0.4	V
I_{OL} ($R\overline{B}$)	Output low current ($R\overline{B}$)		V_{OL} = 0.4 V	8	10		mA
V_{LKO}	V_{DD} supply voltage (erase and program lockout)		–	–	1.8		V

1. Leakage current and standby current double in stacked devices.

Table 24. AC characteristics for command, address, data input

Symbol	Alt. symbol	Parameter			1.8 V devices	3 V devices	Unit
t_{ALLWH}	t_{ALS}	Address Latch Low to Write Enable High	AL setup time	Min	25	12	ns
t_{ALHWH}		Address Latch High to Write Enable High					
t_{CLHWH}	t_{CLS}	Command Latch High to Write Enable High	CL setup time	Min	25	12	ns
t_{CLLWH}		Command Latch Low to Write Enable High					
t_{DVWH}	t_{DS}	Data Valid to Write Enable High	Data setup time	Min	20	12	ns
t_{ELWH}	t_{CS}	Chip Enable Low to Write Enable High	$\overline{E}$ setup time	Min	35	20	ns
t_{WHALH}	t_{ALH}	Write Enable High to Address Latch High	AL hold time	Min	10	5	ns
t_{WHALL}		Write Enable High to Address Latch Low	AL hold time	Min			
t_{WHCLH}	t_{CLH}	Write Enable High to Command Latch High	CL hold time	Min	10	5	ns
t_{WHCLL}		Write Enable High to Command Latch Low					
t_{WHDX}	t_{DH}	Write Enable High to Data Transition	Data hold time	Min	10	5	ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	$\overline{E}$ hold time	Min	10	5	ns
t_{WHWL}	t_{WH}	Write Enable High to Write Enable Low	$\overline{W}$ High hold time	Min	15	10	ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	$\overline{W}$ pulse width	Min	25	12	ns
t_{WLWL}	t_{WC}	Write Enable Low to Write Enable Low	Write cycle time	Min	45	25	ns

Table 25. AC characteristics for operations(1)

Symbol	Alt. symbol	Parameter			1.8 V devices	3 V devices	Unit
t_{ALLRL1}	t_{AR}	Address Latch Low to Read Enable Low	Read electronic signature	Min	10	10	ns
t_{ALLRL2}			Read cycle	Min	10	10	ns
t_{BHRL}	t_{RR}	Ready/Busy High to Read Enable Low		Min	20	20	ns
t_{BLBHx}		Busy time during cache read		Typ	3	3	µs
				Max	25	25	µs
t_{BLBH1}		Ready/Busy Low to Ready/Busy High	Read busy time	Max	25	25	µs
t_{BLBH2}	t_{PROG}		Program busy time	Max	700	700	µs
t_{BLBH3}	t_{BERS}		Erase busy time	Max	3	3	ms
t_{BLBH4}	t_{RST}		Reset busy time, during ready	Max	5	5	µs
			Reset busy time, during read	Max	5	5	µs
			Reset busy time, during program	Max	10	10	µs
			Reset busy time, during erase	Max	500	500	µs
t_{CLLRL}	t_{CLR}	Command Latch Low to Read Enable Low		Min	10	10	ns
t_{DZRL}	t_{IR}	Data Hi-Z to Read Enable Low		Min	0	0	ns
t_{EHQZ}	t_{CHZ}	Chip Enable High to Output Hi-Z		Max	30	30	ns
t_{RHQZ}	t_{RHZ}	Read Enable High to Output Hi-z		Max	100	100	ns
t_{WHWH}	t_{ADL}(2)	Last address latched to data loading time during program operations		Min	100	70	ns
t_{VHWH} t_{VLWH}	t_{WW}(3)	Write protection time		Min	100	100	ns
t_{ELQV}	t_{CEA}	Chip Enable Low to Output Valid		Max	45	25	ns
t_{RHRL}	t_{REH}	Read Enable High to Read Enable Low	Read Enable High hold time	Min	15	10	ns
t_{EHQX} t_{RHQX}(4)	t_{OH}	Chip Enable High or Read Enable High to Output Hold		Min	15	15	ns
t_{RLQX}(4)	t_{RLOH}	Read Enable Low to Output Hold				5	ns
t_{RLRH}	t_{RP}	Read Enable Low to Read Enable High	Read Enable pulse width	Min	25	12	ns
t_{RLRL}	t_{RC}	Read Enable Low to Read Enable Low	Read cycle time	Min	45	25	ns
t_{RLQV}	t_{REA}	Read Enable Low to Output Valid	Read Enable access time	Max	30	20	ns
			Read ES access time(5)				
t_{WHBH}	t_{R}	Write Enable High to Ready/Busy High	Read busy time	Max	25	25	µs
t_{WHBL}	t_{WB}	Write Enable High to Ready/Busy Low		Max	100	100	ns
t_{WHRL}	t_{WHR}	Write Enable High to Read Enable Low		Min	60	60	ns
t_{EHALX} t_{EHCLX}	t_{CSD}	Chip Enable High to Address Latch or Command Latch don't care		Min	10	10	ns
t_{RHWL}	t_{RHW}	Read Enable High to Write Enable Low		Min	100	100	ns

1. The time to ready depends on the value of the pull-up resistor tied to the ready/busy pin. See *Figure 34*, *Figure 35* and *Figure 36*.
2. t_{WHWH} is the time from $\overline{W}$ rising edge during the final address cycle to $\overline{W}$ rising edge during the first data cycle.
3. During a program/erase enable operation, t_{WW} is the delay from $\overline{WP}$ high to $\overline{W}$ High.
   During a program/erase disable Operation, t_{WW} is the delay from $\overline{WP}$ Low to $\overline{W}$ High.
4. t_{RLQX} is valid when frequency is higher than 33 MHz, t_{RHQX} is valid for frequency lower than 33 MHz.
5. ES = electronic signature.

Figure 21. Command Latch AC waveforms

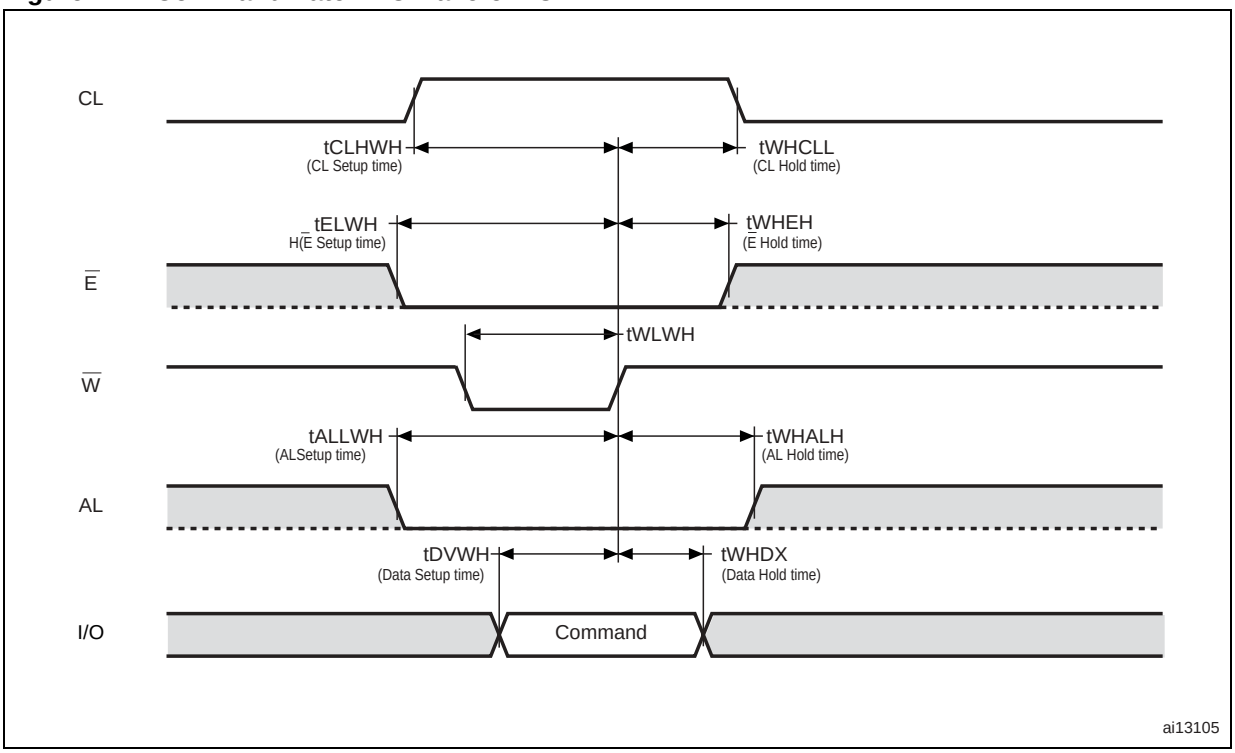


Figure 22. Address Latch AC waveforms

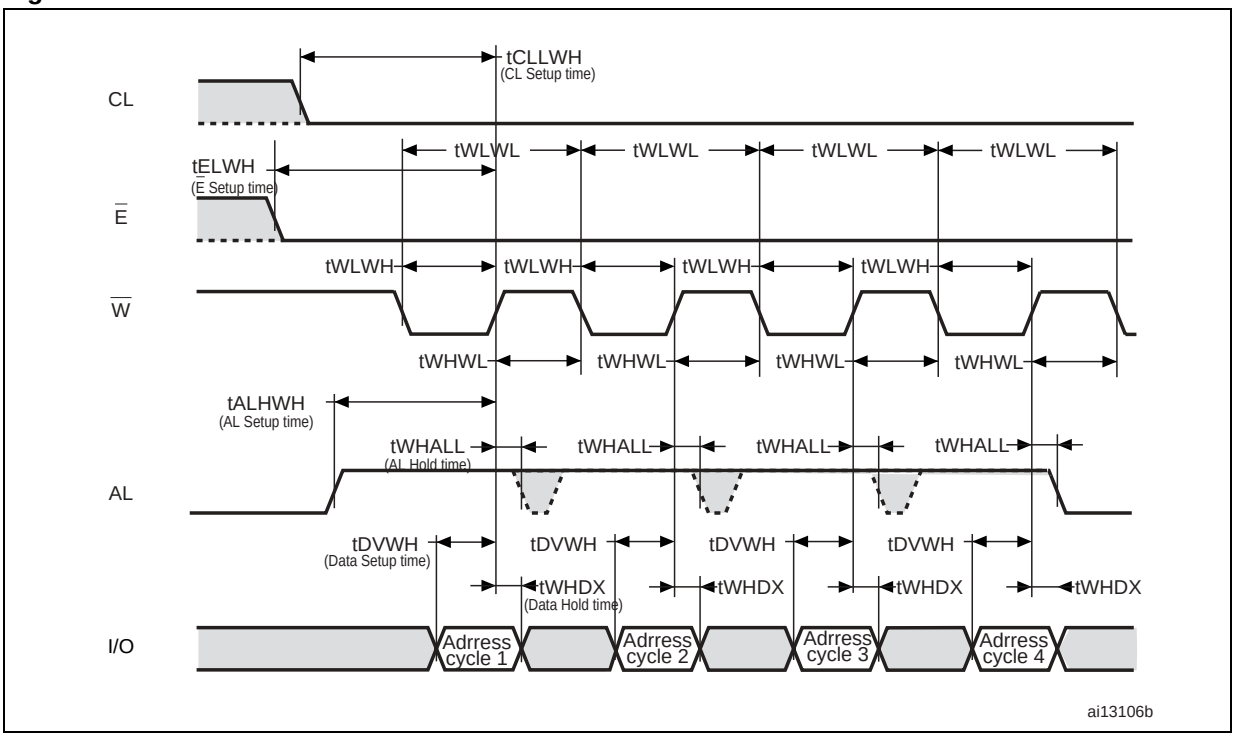
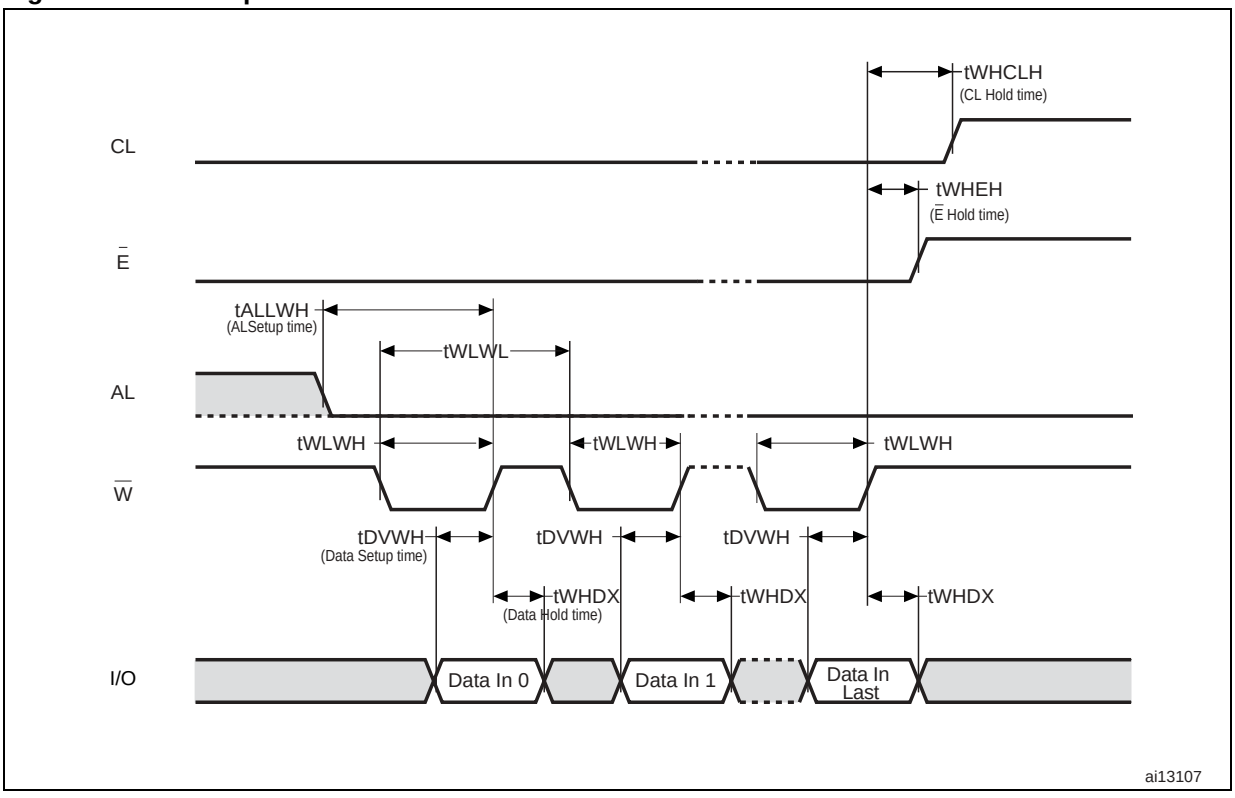
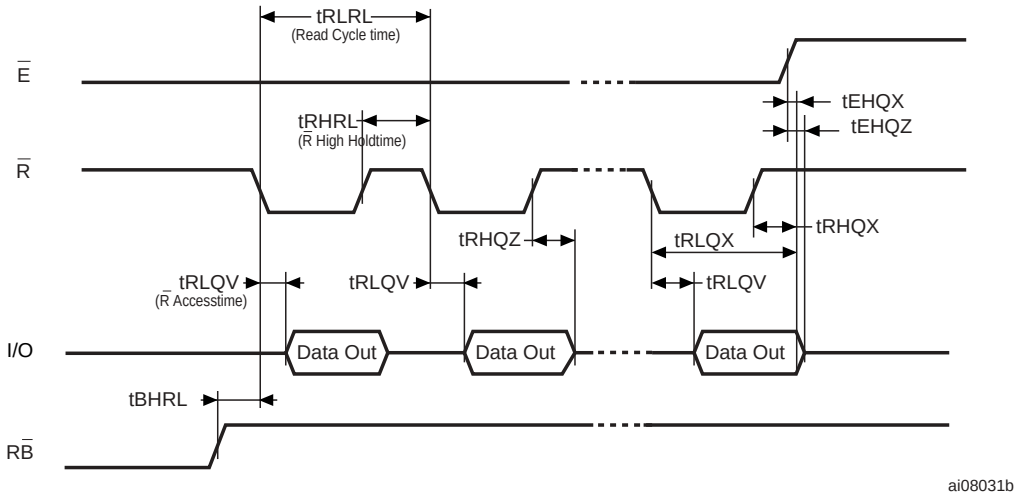


Figure 23. Data Input Latch AC waveforms



1. Data in last is 2112 in x8 devices and 1056 in x16 devices.

Figure 24. Sequential data output after read AC waveforms



1. CL = Low, AL = Low, $\overline{W}$ = High.

Figure 25. Serial access cycle after read, for frequency higher than 33 MHz

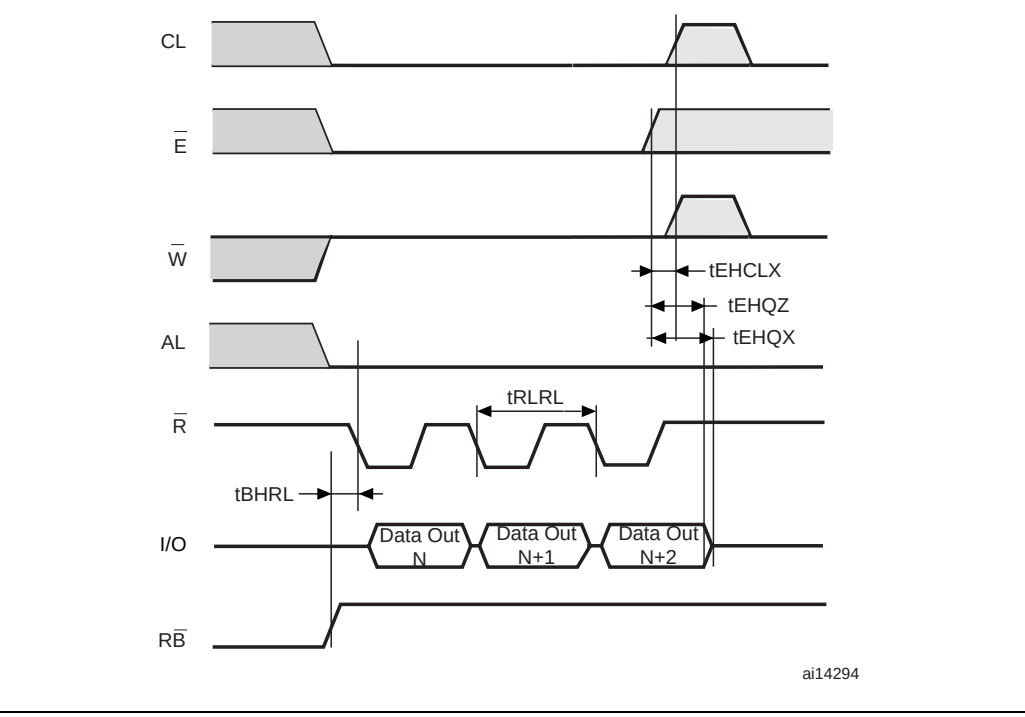


Figure 26. Read status register AC waveforms

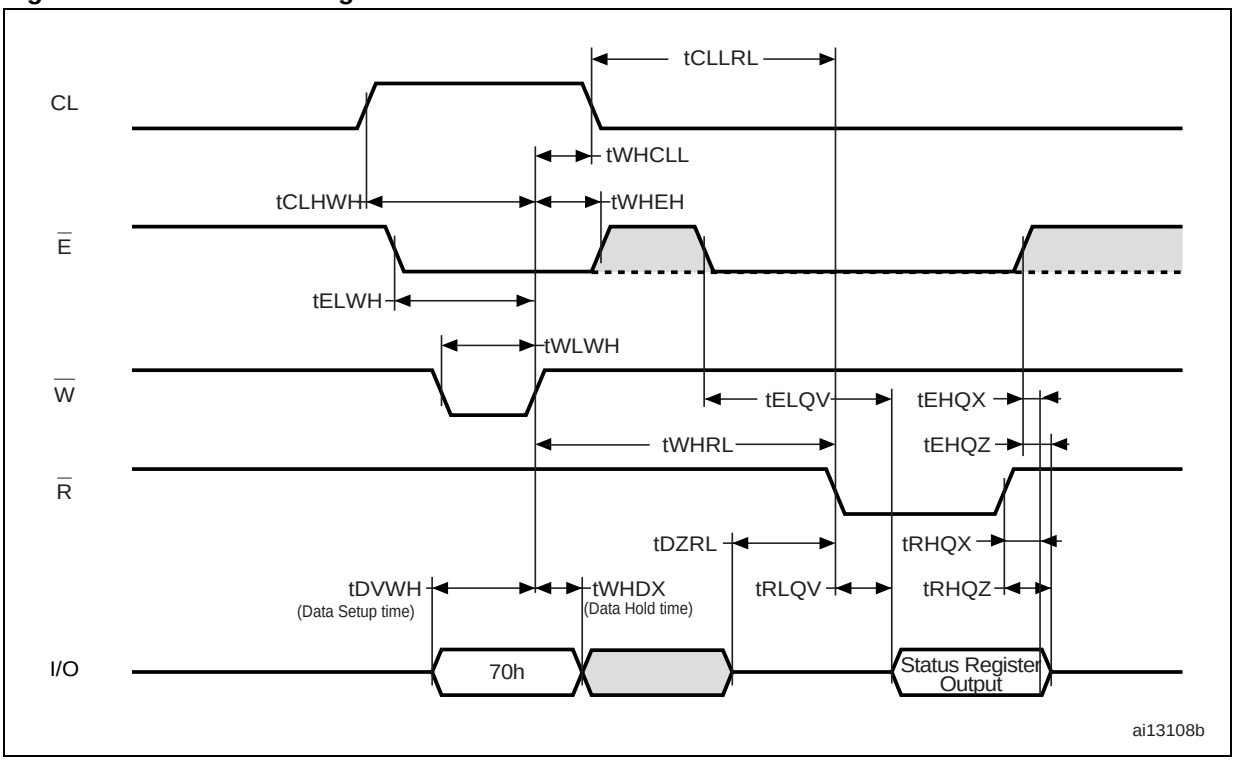
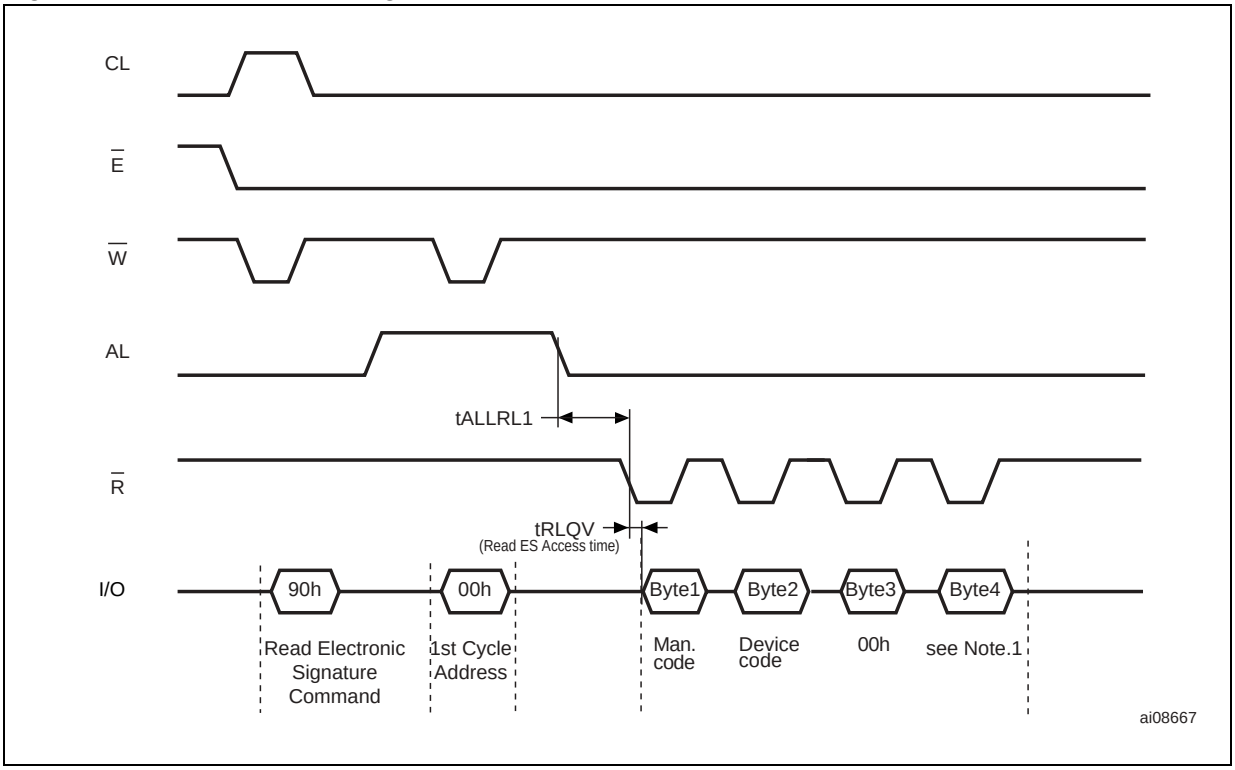


Figure 27. Read electronic signature AC waveforms



1. Refer to *Table 12* for the values of the manufacturer and device codes, and to *Table 13* and *Table 14* for the information contained in byte 3 and 4.

Figure 28. Page read operation AC waveforms

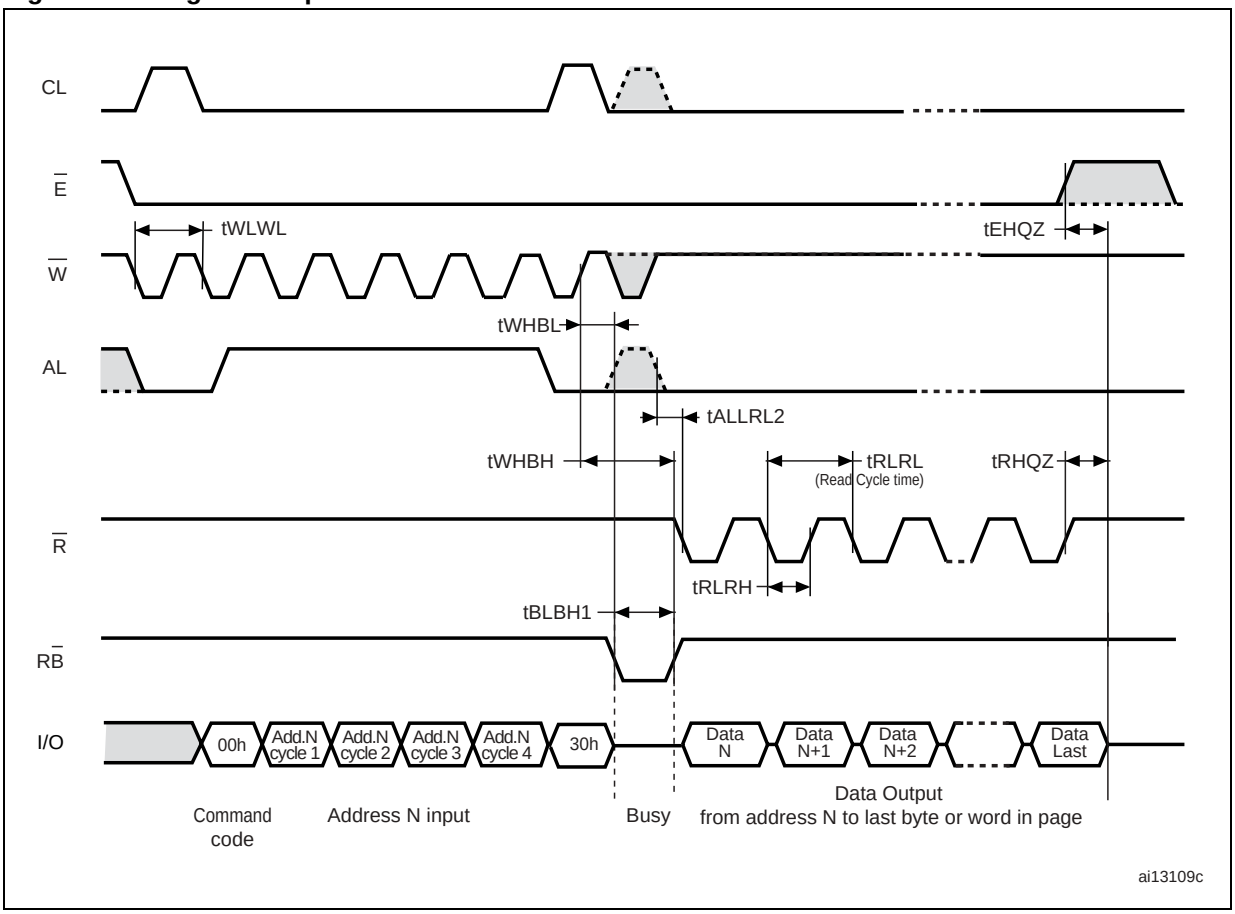


Figure 29. Page program AC waveforms

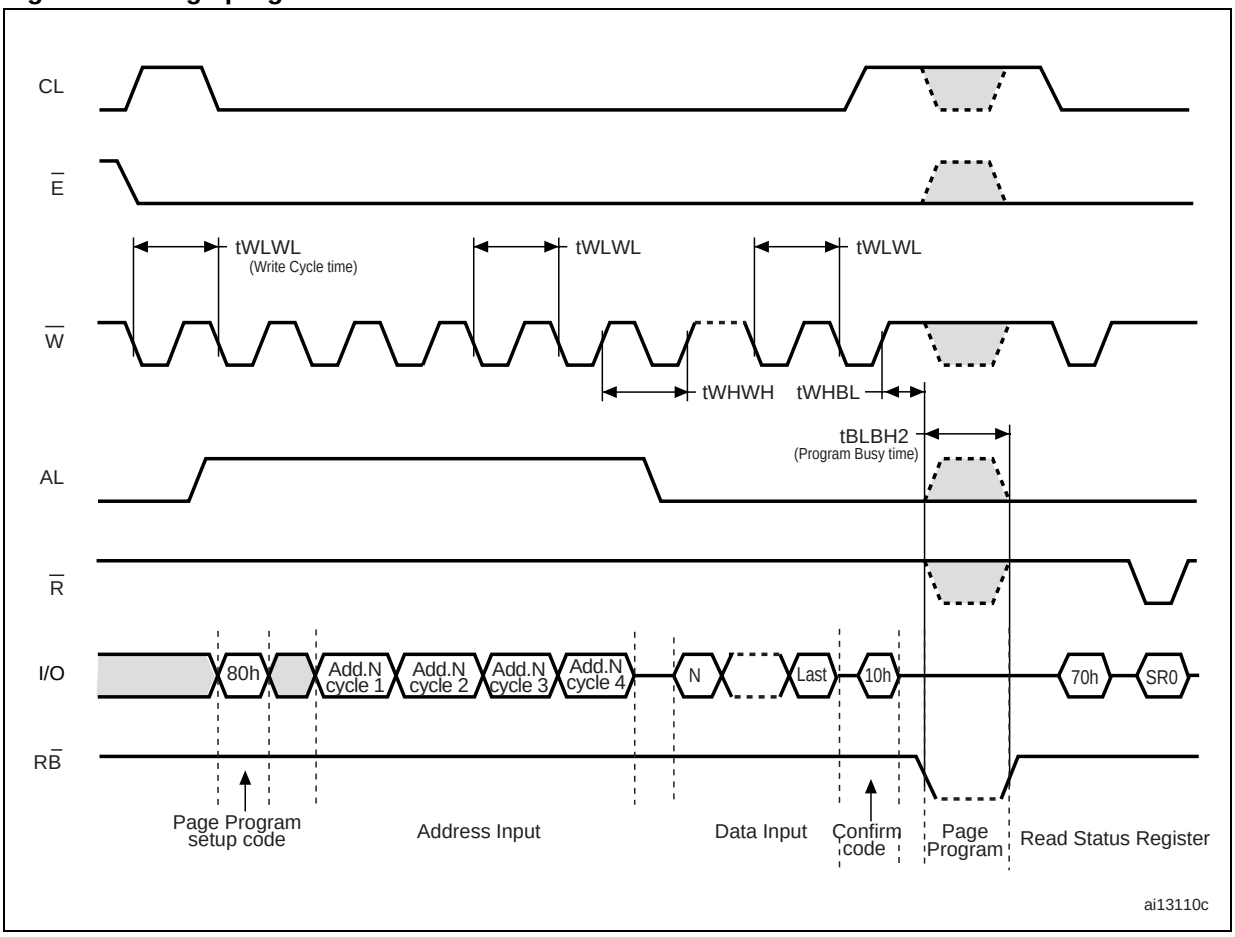


Figure 30. Block erase AC waveforms

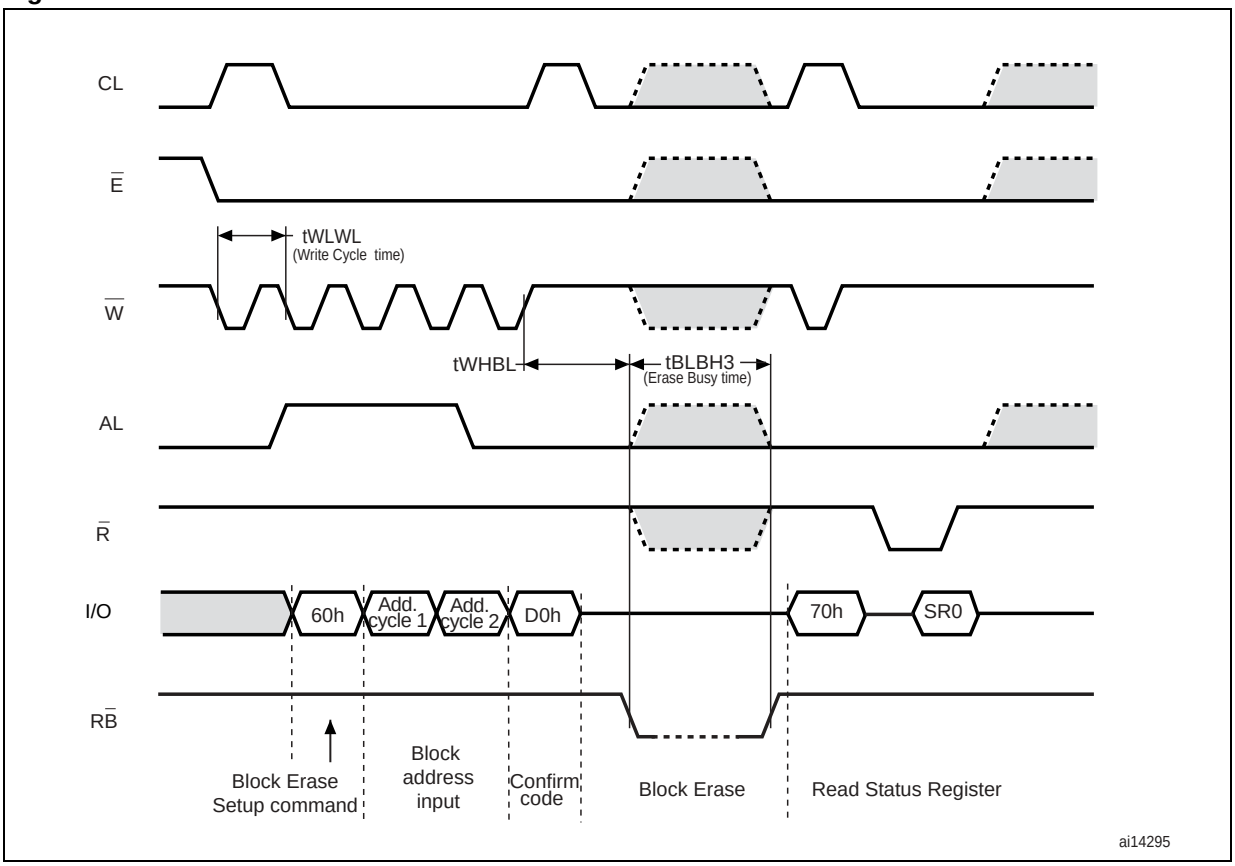


Figure 31. Reset AC waveforms

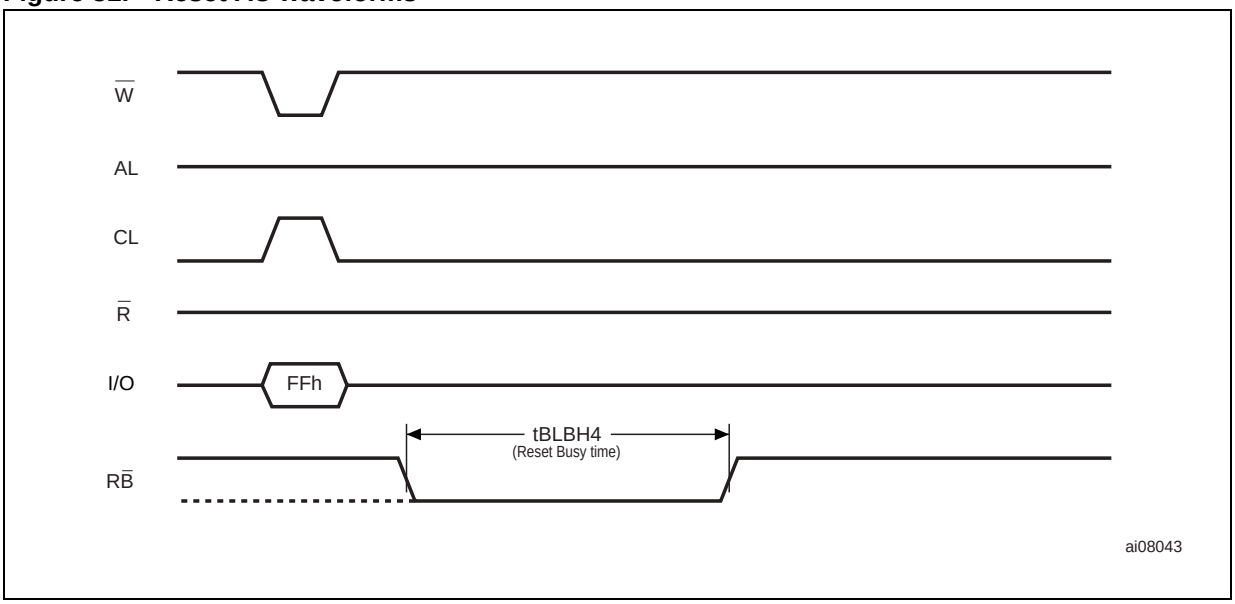


Figure 32. Program/erase enable waveforms

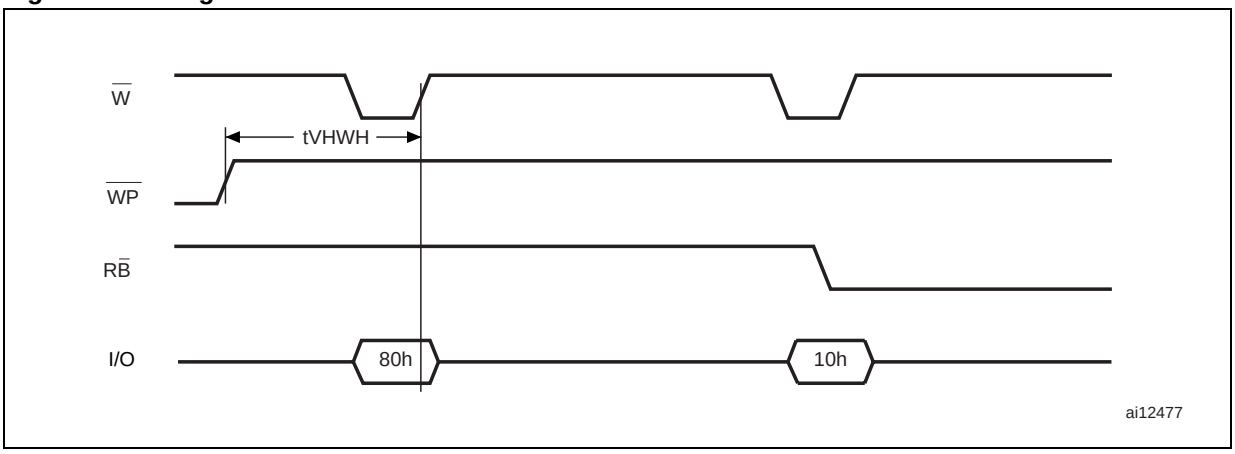
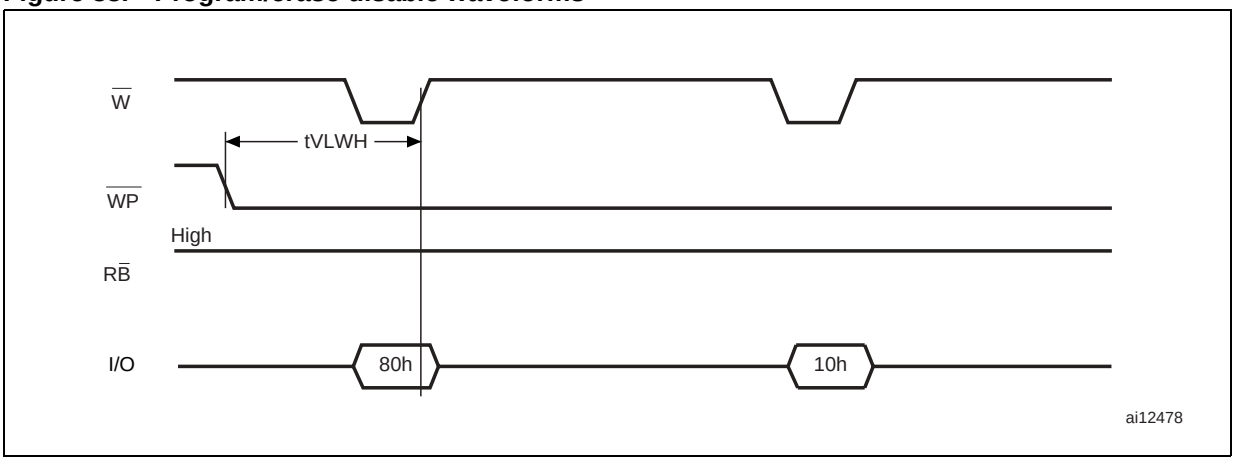


Figure 33. Program/erase disable waveforms



11.1 Ready/Busy signal electrical characteristics

Figure 35, *Figure 34* and *Figure 36* show the electrical characteristics for the Ready/Busy signal. The value required for the resistor R_P can be calculated using the following equation:

$$R_P min = \frac{(V_{DDmax} - V_{OLmax})}{I_{OL} + I_L}$$

So,

$$R_P min(1.8V) = \frac{1.85V}{3mA + I_L}$$

$$R_P min(3V) = \frac{3.2V}{8mA + I_L}$$

where I_L is the sum of the input currents of all the devices tied to the Ready/Busy signal. R_P max is determined by the maximum value of t_r.

Figure 34. Ready/Busy AC waveform

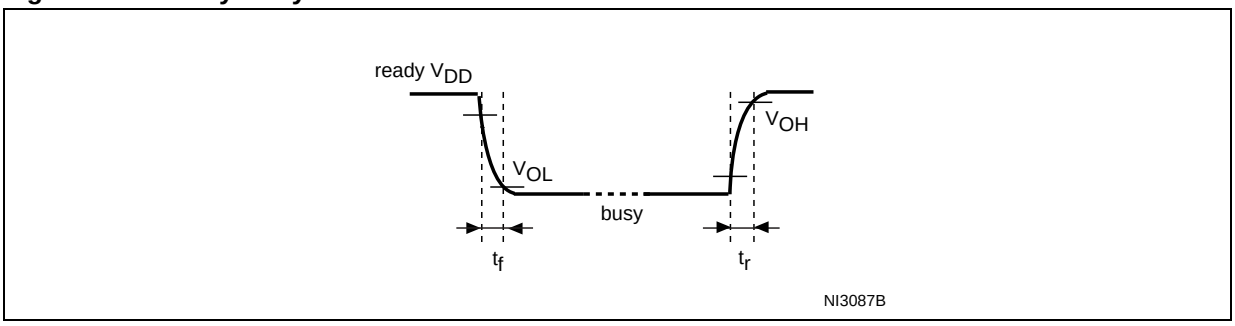


Figure 35. Ready/Busy load circuit

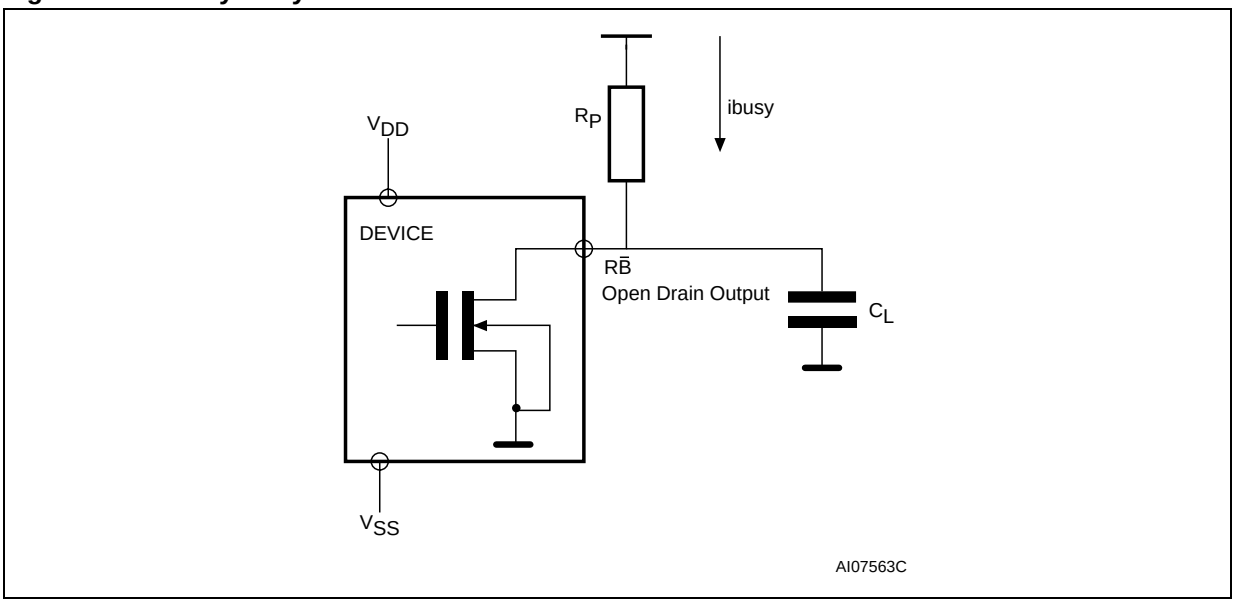
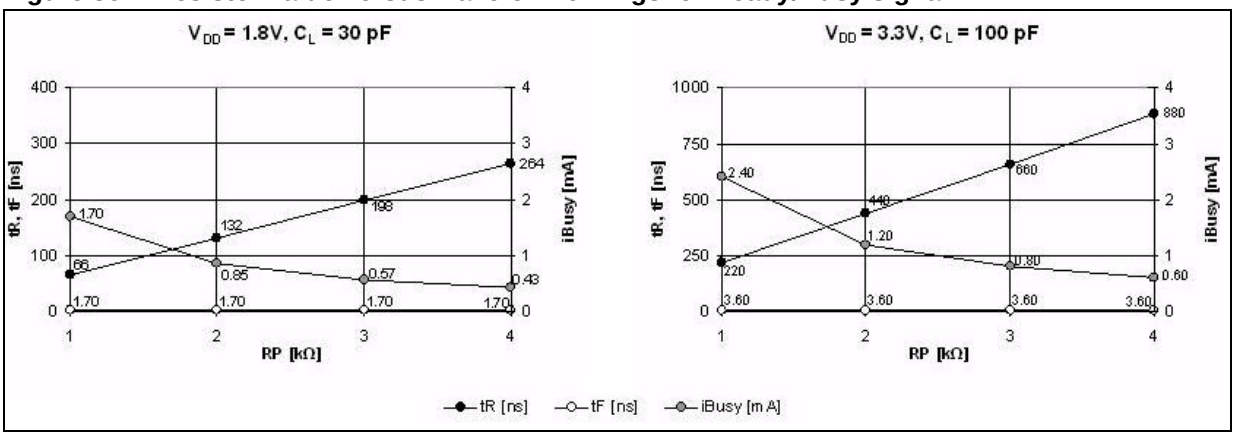


Figure 36. Resistor value versus waveform timings for Ready/Busy signal



1. T = 25°C.

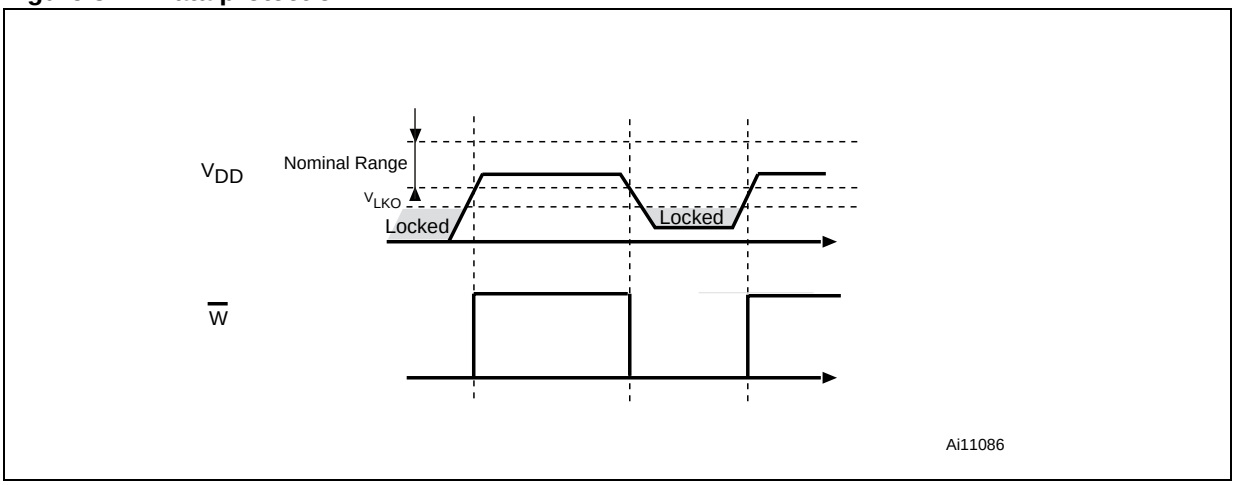
11.2 Data protection

The Numonyx NAND device is designed to guarantee data protection during power transitions.

A V_{DD} detection circuit disables all NAND operations, if V_{DD} is below the V_{LKO} threshold.

In the V_{DD} range from V_{LKO} to the lower limit of nominal range, the $\overline{WP}$ pin should be kept low (V_{IL}) to guarantee hardware protection during power transitions as shown in the below figure.

Figure 37. Data protection

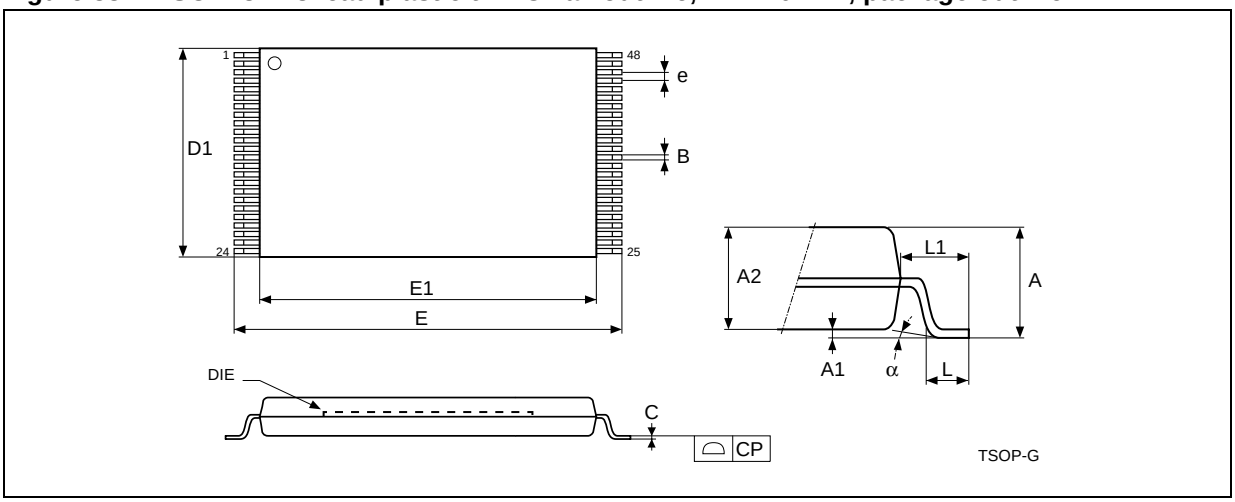


12 Package mechanical

To meet environmental requirements, Numonyx offers these devices in RoHS compliant packages, which have a lead-free second-level interconnect. The category of second-level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

RoHS compliant specifications are available at www.numonyx.com.

Figure 38. TSOP48 - 48 lead plastic thin small outline, 12 x 20 mm, package outline

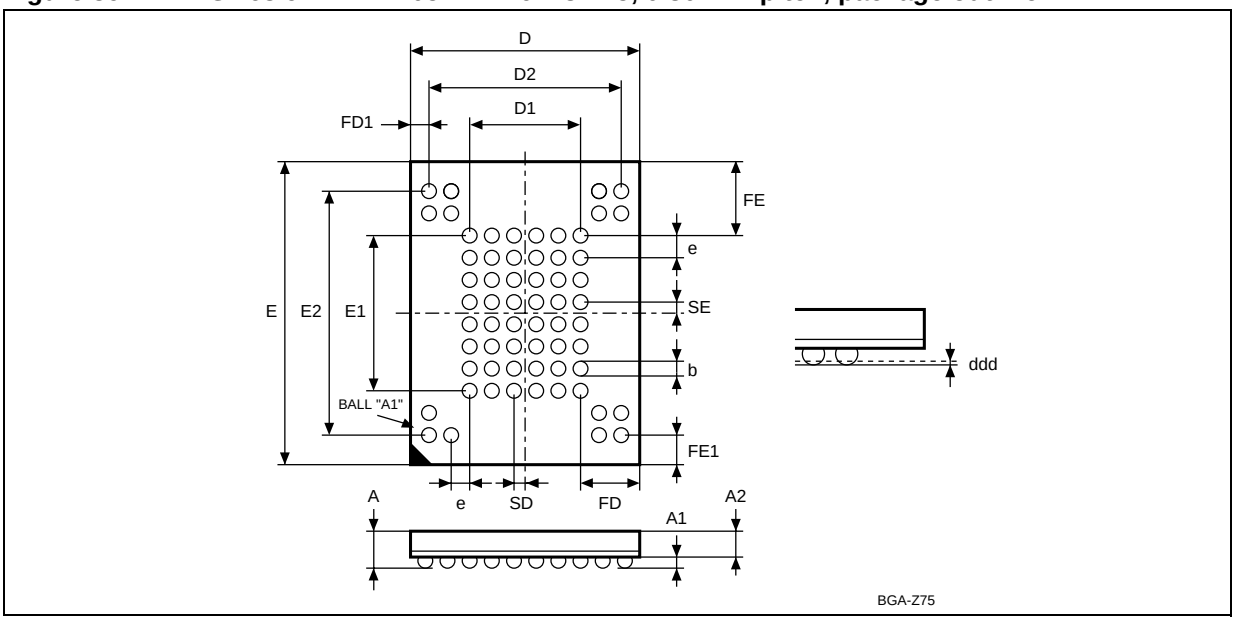


1. Drawing is not to scale.

Table 26. TSOP48 - 48 lead plastic thin small outline, 12 x 20 mm, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1	0.10	0.05	0.15	0.004	0.002	0.006
A2	1.00	0.95	1.05	0.039	0.037	0.041
B	0.22	0.17	0.27	0.009	0.007	0.011
C		0.10	0.21		0.004	0.008
CP			0.08			0.003
D1	12.00	11.90	12.10	0.472	0.468	0.476
E	20.00	19.80	20.20	0.787	0.779	0.795
E1	18.40	18.30	18.50	0.724	0.720	0.728
e	0.50	–	–	0.020	–	
L	0.60	0.50	0.70	0.024	0.020	0.028
L1	0.80			0.031		
α	3°	0°	5°	3°	0°	5°

Figure 39. VFBGA63 9 x 11 x 1.05 mm - 6 x 8 +15, 0.80 mm pitch, package outline

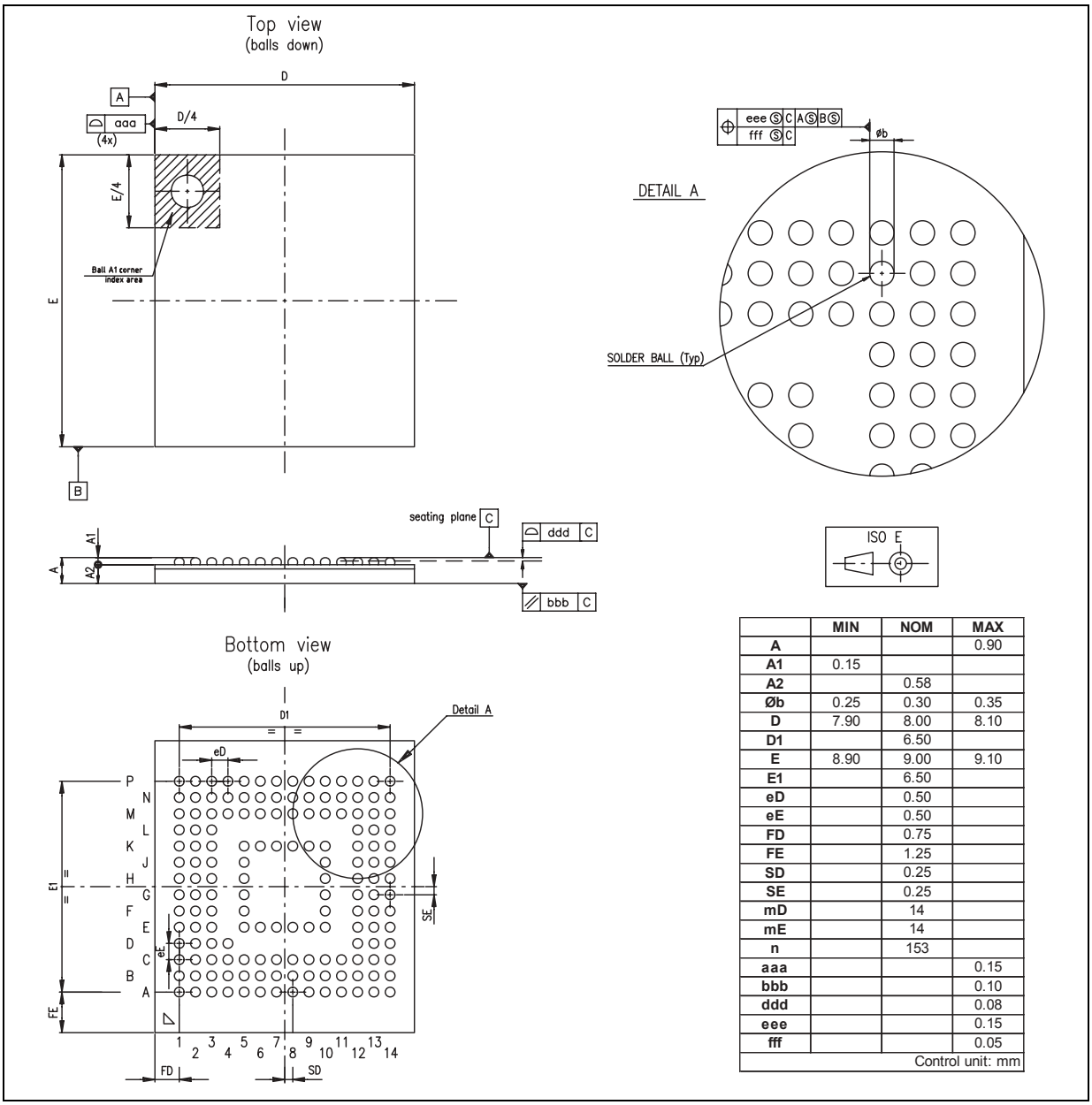


1. Drawing is not to scale

Table 27. VFBGA63 9 x 11 x 1.05 mm - 6 x 8 +15, 0.80 mm pitch, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.05			0.041
A1		0.25			0.010	
A2	0.65			0.026		
b	0.45	0.40	0.50	0.018	0.016	0.020
D	9.00	8.90	9.10	0.354	0.350	0.358
D1	4.00			0.157		
D2	7.20			0.283		
ddd			0.10			0.004
E	11.00	10.90	11.10	0.433	0.429	0.437
E1	5.60			0.220		
E2	8.80			0.346		
e	0.80	–	–	0.031	–	–
FD	2.50			0.098		
FD1	0.90			0.035		
FE	2.70			0.106		
FE1	1.10			0.043		
SD	0.40	–	–	0.016	–	–
SE	0.40	–	–	0.016	–	–

Figure 40. VFBGA153 8 x 9 x 0.9 mm - 132+21 3R14, 0.50 mm pitch, package outline and mechanical data



	MIN	NOM	MAX
A			0.90
A1	0.15		
A2		0.58	
Øb	0.25	0.30	0.35
D	7.90	8.00	8.10
D1		6.50	
E	8.90	9.00	9.10
E1		6.50	
eD		0.50	
eE		0.50	
FD		0.75	
FE		1.25	
SD		0.25	
SE		0.25	
mD		14	
mE		14	
n		153	
aaa			0.15
bbb			0.10
ddd			0.08
eee			0.15
fff			0.05

Control unit: mm

13 Ordering information

Table 28. Ordering information scheme

Example: NAND01GW3B2C ZA 6 E

Device type
NAND flash memory

Density
01G = 1 Gbit

Operating voltage
R = V_{DD} = 1.7 to 1.95 V
W = V_{DD} = 2.7 to 3.6 V

Bus width
3 = x8
4 = x16(1)

Family identifier
B = 2112-byte/ 1056-word page

Device options
2 = chip enable don't care enabled

Product version
B = second version
C = third version

Package
N = TSOP48 12 x 20 mm
ZA = VFBGA63 9 x 11 x 1.05 mm, 0.8 mm pitch
ZF = VFBGA153 8 x 9 x 0.9 mm. 0.5 mm pitch

Temperature range
5 = –25 to 85 °C
6 = –40 to 85 °C

Option
E = RoHS compliant package, standard packing
F = RoHS compliant package, tape & reel packing

1. x16 organization only available for MCP products.

Note: Not all combinations are necessarily available. For a list of available devices or for further information on any aspect of these products, please contact your nearest Numonyx sales office.

14 Revision history

Table 29. Document revision history

Date	Version	Changes
24-Jun-2008	1	Initial release.
16-Jan-2009	2	Modified *Section 8.5: Error correction code*, *Figure 34: Ready/Busy AC waveform*, and *Figure 36: Resistor value versus waveform timings for Ready/Busy signal*. Removed Figure 19: Error detection.
23-Feb-2009	3	Modified *Figure 7: Read operations*, *Table 12: Electronic signature* and *Table 16: Parameter page data structure*. Added security features on the cover page and in *Section 1: Description*. Removed references to ECOPACK packages throughout the document.
08-Jun-2009	4	Document status promoted from preliminary data to full datasheet. Modified dimension A2 of the VFBGA63 package in *Table 27: VFBGA63 9 x 11 x 1.05 mm - 6 x 8 +15, 0.80 mm pitch, package mechanical data*.
29-Jan-2010	5	Added references to the VFBGA153 8 x 9 x 0.9 mm package throughout the document. Removed temperature range 1 and added temperature range 5 in *Table 28: Ordering information scheme*.

Please Read Carefully: