NCV4299

150 mA Low-Dropout Voltage Regulator

The NCV4299 is a family of precision micropower voltage regulators with an output current capability of 150 mA. It is available in 5.0 V or 3.3 V output voltage, and is housed in an 8−lead SON and in a 14−lead SON (fused) package.

The output voltage is accurate within ±2% with a maximum dropout voltage of 0.5 V at 100 mA. Low Quiescent current is a feature drawing only 90 μA with a 1 mA load. This part is ideal for any and all battery operated microprocessor equipment.

The device features microprocessor interfaces including an adjustable reset output and adjustable system monitor to provide shutdown early warning. An inhibit function is available on the 14−lead part. With inhibit active, the regulator turns off and the device consumes less than 1.0 μA of quiescent current.

The part can withstand load dump transients making it suitable for use in automotive environments.

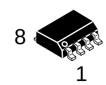
Features

- 5.0 V, 3.3 V ±2%, 150 mA
- Extremely Low Current Consumption
  - 90 μA (Typ) in the ON Mode
  - <1.0 μA in the Off Mode
- Early Warning
- Reset Output Low Down to V_Q = 1.0 V
- Adjustable Reset Threshold
- Wide Temperature Range
- Fault Protection
  - 60 V Peak Transient Voltage
  - −40 V Reverse Voltage
  - Short Circuit
  - Thermal Overload
- Internally Fused Leads in the SO−14 Package
- Inhibit Function with μA Current Consumption in the Off Mode
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Control
- Pb−Free Packages are Available

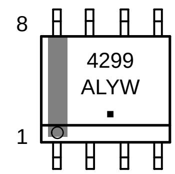
ON Semiconductor®

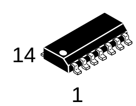
http://onsemi.com

MARKING DIAGRAMS

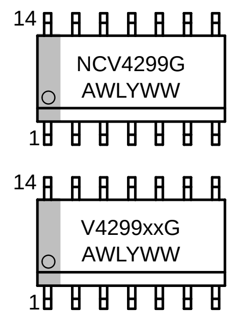


SO−8
D SUFFIX
CASE 751





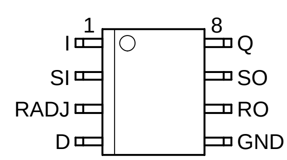
SO−14
D SUFFIX
CASE 751A

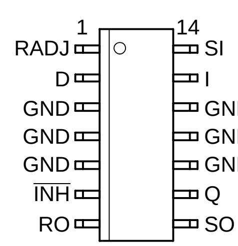


xx	= 33 (3.3 V Version)
	= 50 (5.0 V Version)
A	= Assembly Location
L, WL	= Wafer Lot
Y	= Year
W, WW	= Work Week
G	= Pb−Free Package
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS





ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 21 of this data sheet.

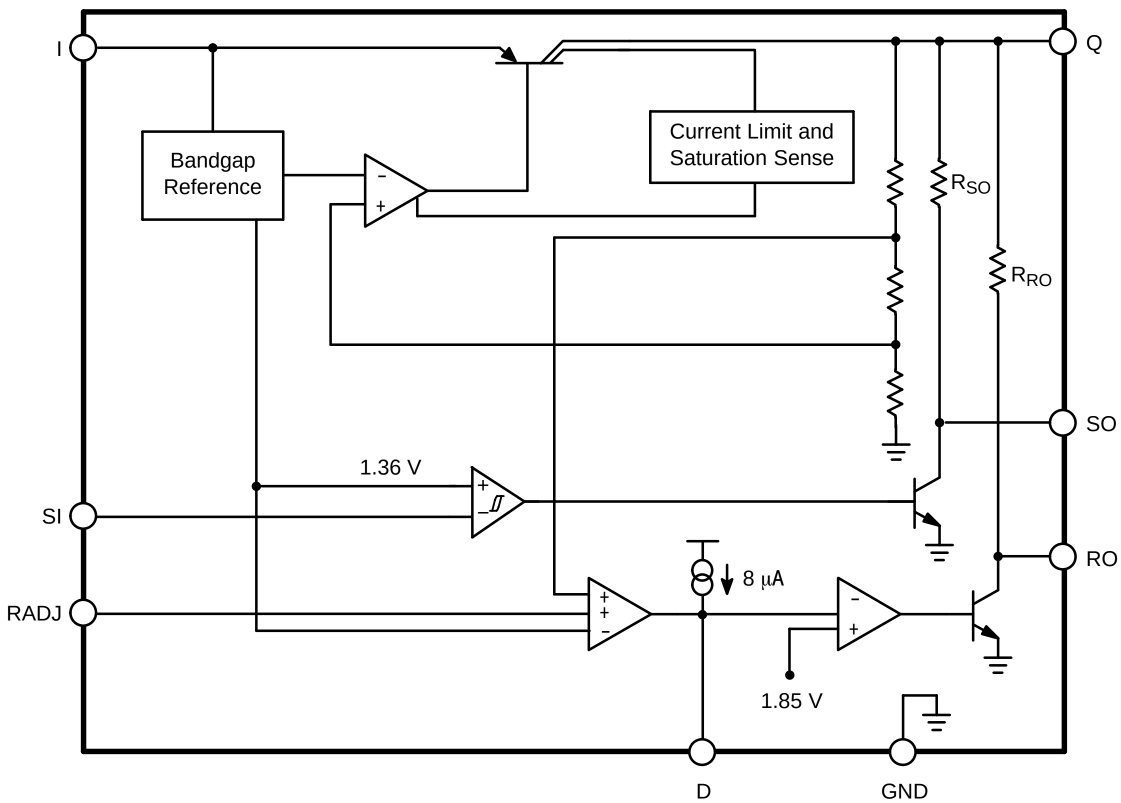


Figure 1. SO−8 Simplified Block Diagram

PIN FUNCTION DESCRIPTION − SO−8 PACKAGE

Pin	Symbol	Description
1	I	Input. Battery Supply Input Voltage. Bypass directly to GND with ceramic capacitor.
2	SI	Sense Input. Can provide an early warning signal of an impending reset condition when used with SO. Connect to Q if not used.
3	RADJ	Reset Adjust. Use resistor divider to Q to adjust reset threshold lower. Connect to GND if not used.
4	D	Reset Delay. Connect external capacitor to ground to set delay time.
5	GND	Ground.
6	RO	Reset Output. NPN collector output with internal 20 kΩ pullup to Q. Notifies user of out of regulation condition. Leave open if not used.
7	SO	Sense Output. NPN collector output with internal 20 kΩ pullup to Q. Can be used to provide early warning of an impending reset condition. Leave open if not used.
8	Q	5.0 V, 3.3 V, ±2%, 150 mA output. Use 22 μF, ESR < 5.0 Ω to ground.

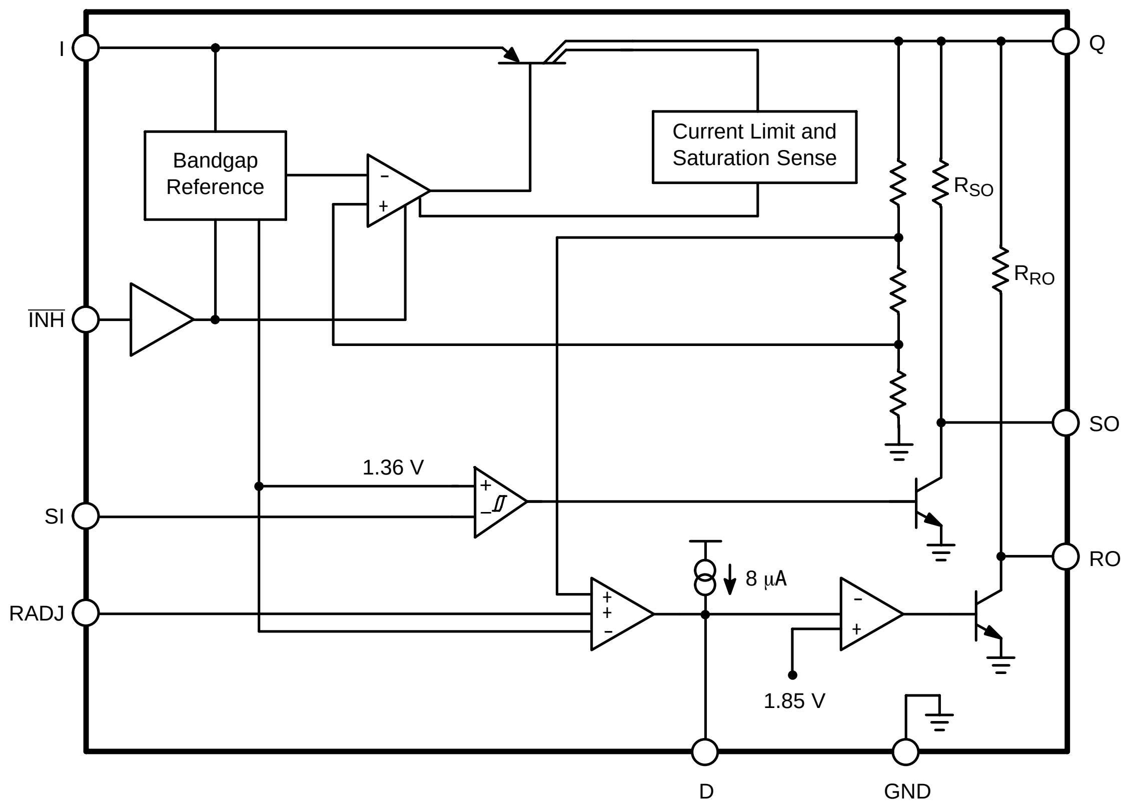


Figure 2. SO−14 Simplified Block Diagram

PIN FUNCTION DESCRIPTION − SO−14 PACKAGE

Pin	Symbol	Description
1	RADJ	Reset Adjust. Use resistor divider to Q to adjust reset threshold lower. Connect to GND if not used.
2	D	Reset Delay. Connect external capacitor to ground to set delay time.
3	GND	Ground.
4	GND	Ground.
5	GND	Ground.
6	$\overline{INH}$	Inhibit. Connect to I if not needed. A high turns the regulator on.
7	RO	Reset Output. NPN collector output with internal 20 kΩ pullup to Q. Notifies user of out of regulation condition.
8	SO	Sense Output. NPN collector output with internal 20 kΩ pullup to Q. Can be used to provide early warning of an impending reset condition.
9	Q	5.0 V, 3.3 V, ±2%, 150 mA output. Use 22 μF, ESR < 5.0 Ω to ground.
10	GND	Ground.
11	GND	Ground.
12	GND	Ground.
13	I	Input. Battery Supply Input Voltage.
14	SI	Sense Input. Can provide an early warning signal of an impending reset condition when used with SO.

MAXIMUM RATINGS

Rating	Symbol	Min	Max	Unit
Input Voltage to Regulator (DC)	V_I	−40	45	V
Input Peak Transient Voltage to Regulator wrt GND	−	−	60	V
Inhibit ($\overline{INH}$) (Note 1)	$V_{\overline{INH}}$	−40	45	V
Sense Input (SI)	V_{SI}	−0.3	45	V
Sense Input (SI)	I_{SI}	−1.0	1.0	mA
Reset Threshold (RADJ)	V_{RE}	−0.3	7.0	V
Reset Threshold (RADJ)	I_{RE}	−10	10	mA
Reset Delay (D)	V_D	−0.3	7.0	V
Reset Output (RO)	V_{RO}	−0.3	7.0	V
Sense Output (SO)	V_{SO}	−0.3	7.0	V
Output (Q)	V_Q	−0.3	16	V
Output (Q)	I_Q	−5.0	−	mA
ESD Capability, Human Body Model (Note 5)	ESD_{HB}	2.0	−	kV
ESD Capability, Machine Model (Note 5)	ESD_{MM}	200	−	V
ESD Capability, Charged Device Model (Note 5)	ESD_{CDM}	1.0	−	kV
Junction Temperature	T_J	−	150	°C
Storage Temperature	T_{stg}	−50	150	°C

OPERATING RANGE

Input Voltage 5.0 V Version 3.3 V Version	V_I	 4.5 4.4	 45 45	V
Junction Temperature	T_J	−40	150	°C

LEAD TEMPERATURE SOLDERING REFLOW (Note 3)

Lead Temperature Soldering (Note 5) Reflow (SMD styles only), leaded 60−150 sec above 183, 30 sec max at peak	T_{SLD}	−	240 Pk	°C
Reflow (SMD styles only), lead free 60s−150 sec above 217, 40 sec max at peak	T_{SLD}	−	265 Pk	°C
Moisture Sensitivity Level	MSL	Level 1		

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. 14 pin package only.
2. Preliminary numbers.
3. Per IPC / JEDEC J−STD−020C.
4. Measured to Pin 4. All ground pins connected to ground.
5. This device series incorporates ESD protection and is tested by the following methods:
   ESD HBM tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD MM tested per AEC−Q100−003 (EIA/JESD22−A115)
   ESD CDM tested per EIA/JES D22/C101, Field Induced Charge Model.

THERMAL CHARACTERISTICS

Characteristic	Test Conditions (Typical Value)			Unit
	Note 6	Note 7	Note 8	
SO−8 Junction−to−Tab (ψ_{JLx}, θ_{JLx}) Junction−to−Ambient ($R_{\theta JA}$, θ_{JA})	 54 172	 52 144	 48 118	°C/W
SO−14 Junction−to−Tab (ψ_{JLx}, θ_{JLx}) Junction−to−Ambient ($R_{\theta JA}$, θ_{JA})	 19 112	 21 89	 20 67	°C/W

6. 2 oz Copper, 50 mm sq Copper area, 1.5 mm thick FR4
7. 2 oz Copper, 150 mm sq Copper area, 1.5 mm thick FR4
8. 2 oz Copper, 500 mm sq Copper area, 1.5 mm thick FR4

ELECTRICAL CHARACTERISTICS (−40°C < T_J < 150°C; V_I = 13.5 V unless otherwise noted.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Q						
Output Voltage (5.0 V Version)	V_Q	1.0 mA < I_Q < 150 mA, 6.0 V < V_I < 16 V	4.9	5.0	5.1	V
Output Voltage (3.3 V Version)	V_Q	1.0 mA < I_Q < 150 mA, 5.5 V < V_I < 16 V	3.23	3.3	3.37	V
Current Limit	I_Q	−	250	400	500	mA
Quiescent Current ($I_q = I_I - I_Q$)	I_q	$\overline{INH}$ ON, I_Q < 1.0 mA, T_J = 25°C	−	86	100	μA
Quiescent Current ($I_q = I_I - I_Q$)	I_q	$\overline{INH}$ ON, I_Q < 1.0 mA	−	90	105	μA
Quiescent Current ($I_q = I_I - I_Q$)	I_q	$\overline{INH}$ ON, I_Q = 10 mA	−	170	500	μA
Quiescent Current ($I_q = I_I - I_Q$)	I_q	$\overline{INH}$ ON, I_Q = 50 mA	−	0.7	2.0	mA
Quiescent Current ($I_q = I_I - I_Q$)	I_q	$\overline{INH}$ = 0 V, T_J = 25°C	−	−	1.0	μA
Dropout Voltage (Note 9)	V_{dr}	I_Q = 100 mA	−	0.22	0.50	V
Load Regulation	ΔV_Q	I_Q = 1.0 mA to 100 mA	−	5.0	30	mV
Line Regulation	ΔV_Q	V_I = 6.0 V to 28 V, I_Q = 1.0 mA	−	10	25	mV
Power Supply Ripple Rejection	P_{SRR}	fr = 100 Hz, Vr = 1.0 Vpp, I_Q = 100 mA	−	66	−	dB
Inhibit ($\overline{INH}$) (14 Pin Package Only)						
Inhibit Off Voltage	$V_{\overline{INHOFF}}$	V_Q < 1.0 V	−	−	0.8	V
Inhibit On Voltage 5.0 V Version 3.3 V Version	$V_{\overline{INHON}}$	 V_Q > 4.85 V V_Q > 3.2 V	 3.5 3.5	 − −	 − −	V
Input Current	$I_{\overline{INH}ON}$ $I_{\overline{INH}OFF}$	$\overline{INH}$ ON $\overline{INH}$ = 0 V	− −	3.0 0.5	10 2.0	μA
Reset (RO)						
Switching Threshold 5.0 V Version 3.3 V Version	V_{rt}	−	 4.50 2.96	 4.60 3.06	 4.80 3.16	V
Output Resistance	R_{RO}	−	10	20	40	kΩ
Reset Output Low Voltage 5.0 V Version 3.3 V Version	V_{RO}	 Q < 4.5 V, Internal R_{RO}, I_{RO} = −1.0 mA Q < 2.96 V, Internal R_{RO}, I_{RO} = −1.0 mA	 − −	 0.17 0.17	 0.40 0.40	V
Allowable External Reset Pullup Resistor	V_{ROext}	External Resistor to Q	5.6	−	−	kΩ
Delay Upper Threshold	V_{UD}	−	1.5	1.85	2.2	V
Delay Lower Threshold	V_{LD}	−	0.4	0.5	0.6	V

9. Measured when the output voltage V_Q has dropped 100 mV from the nominal value obtained at V_I = 13.5 V.

ELECTRICAL CHARACTERISTICS (continued) ($-40°C < T_J < 150°C$; $V_I = 13.5$ V unless otherwise noted.)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Reset (RO)						
Delay Output Low Voltage 5.0 V Version 3.3 V Version	V_D	 Q < 4.5 V, Internal R_{RO} Q < 2.96 V, Internal R_{RO}	 – –	 – 0.017	 0.1 0.1	V
Delay Charge Current 5.0 V Version 3.3 V Version	I_D	 Q < 4.5 V, Internal R_{RO}, $V_D = 1.0$ V Q < 2.96 V, Internal R_{RO}, $V_D = 1.0$ V	 4.0 –	 7.1 –	 12 –	μA
Power On Reset Delay Time	t_d	$C_D = 100$ nF	17	28	35	ms
Reset Reaction Time	t_{rr}	$C_D = 100$ nF	0.5	2.2	4.0	μs
Reset Adjust Switching Threshold 5.0 V Version 3.3 V Version	$V_{RADJ,TH}$	 Q > 3.5 V Q > 2.3 V	 1.26 –	 1.36 –	 1.44 –	V
Input Voltage Sense (SI and SO)						
Sense Input Threshold High	$V_{SI,HIGH}$	–	1.34	1.45	1.54	V
Sense Input Threshold Low	$V_{SI,LOW}$	–	1.26	1.36	1.44	V
Sense Input Hysteresis	–	(Sense Threshold High) − (Sense Threshold Low)	50	90	130	mV
Sense Input Current	I_{SI}	–	−1.0	0.1	1.0	μA
Sense Output Resistance	R_{SO}	–	10	20	40	kΩ
Sense Output Low Voltage	V_{SO}	$V_{SI} < 1.20$ V, $V_I > 4.2$ V, $I_{SO} = 0$ μA	–	0.1	0.4	V
Allowable External Sense Out Pullup Resistor	R_{SOext}	–	5.6	–	–	kΩ
SI High to SO High Reaction Time	t_{pdSOLH}	–	–	4.4	8.0	μs
SI Low to SO Low Reaction Time	t_{pdSOHL}	–	–	3.8	5.0	μs

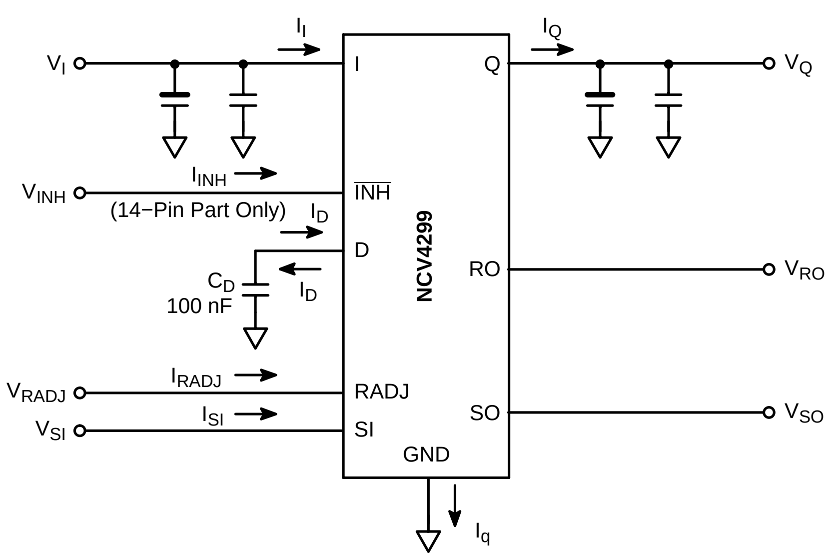


Figure 3. Measurement Circuit

TYPICAL PERFORMANCE CHARACTERISTICS − 5.0 V OPTION

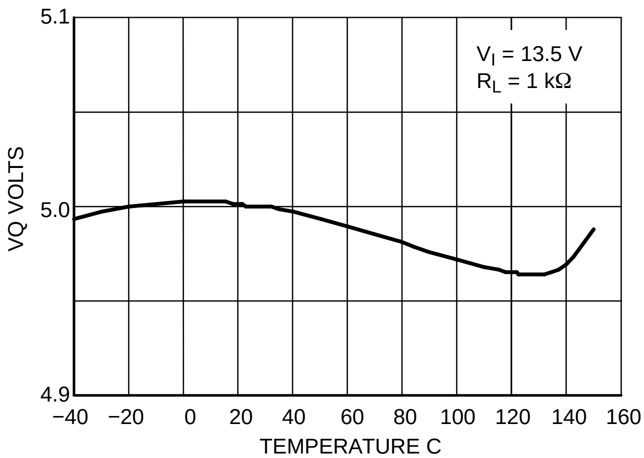


Figure 4. Output Voltage VQ vs. Temperature TJ

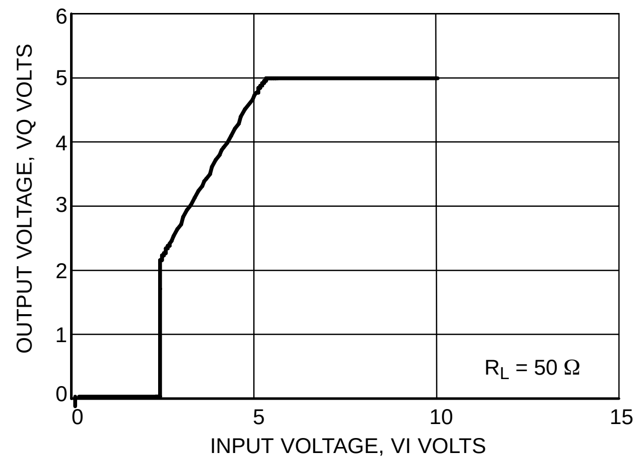


Figure 5. Output Voltage VQ vs. Input Voltage

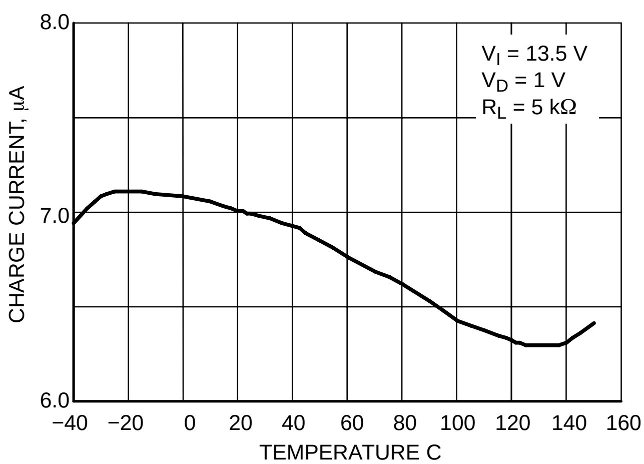


Figure 6. Charge Current Id, c vs. Temperature TJ

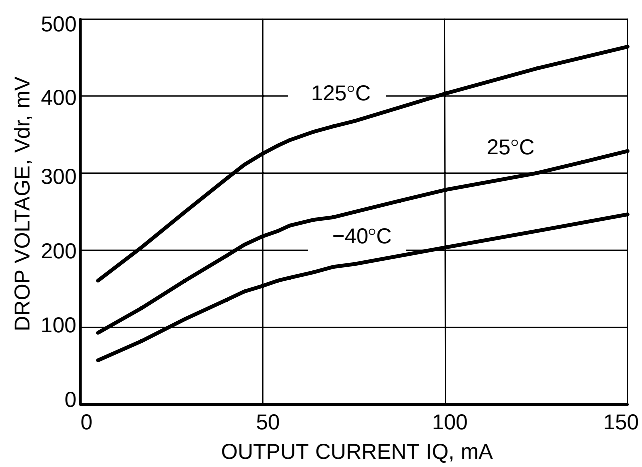


Figure 7. Drop Voltage Vdr vs. Output Current IQ

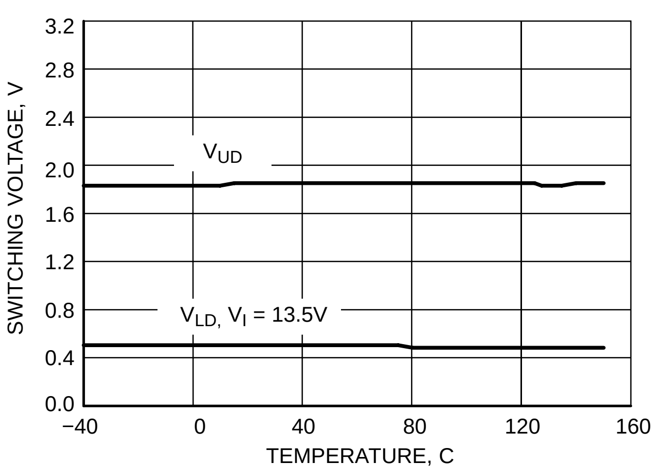


Figure 8. Switching Voltage VUD and VLD vs. Temperature TJ

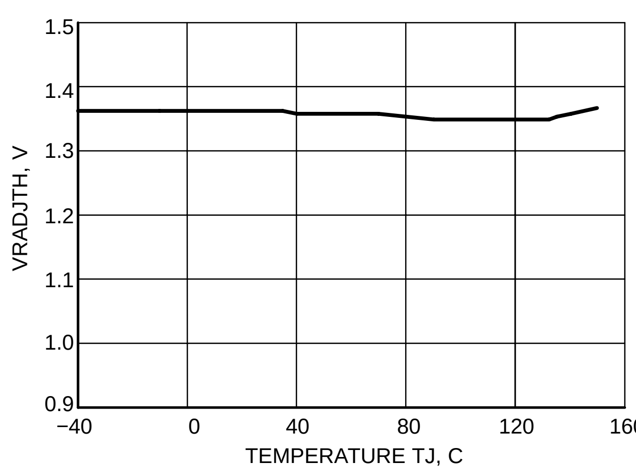


Figure 9. Reset Adjust Switching Threshold VRADJTH vs. Temperature TJ

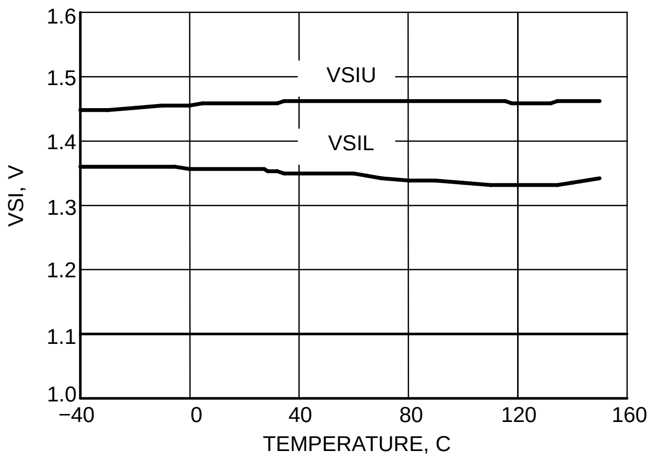


Figure 10. Sense Threshold VSI vs. Temperature TJ

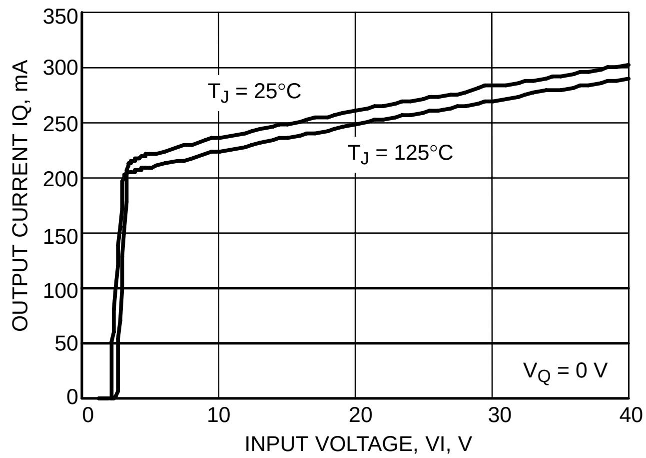


Figure 11. Output Current Limit IQ vs. Input Voltage, VI

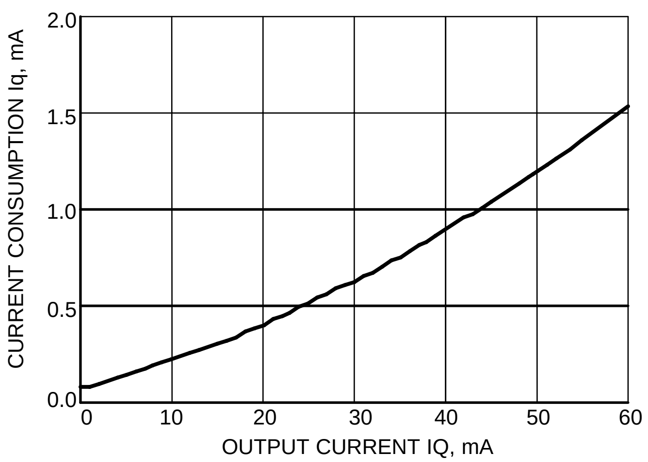


Figure 12. Current Consumption Iq vs. Output Current IQ

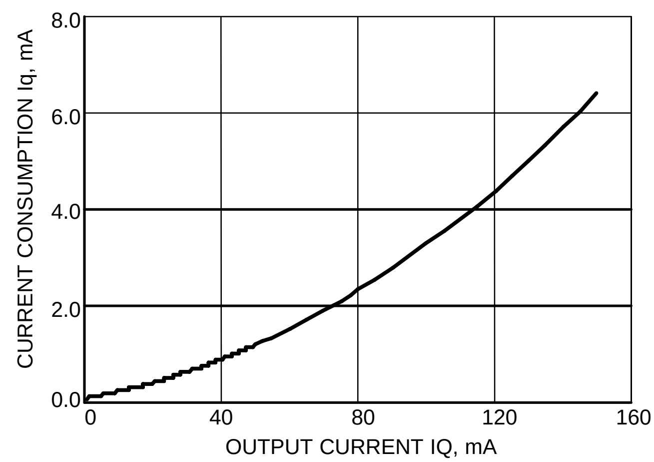


Figure 13. Current Consumption Iq vs. Output Current IQ

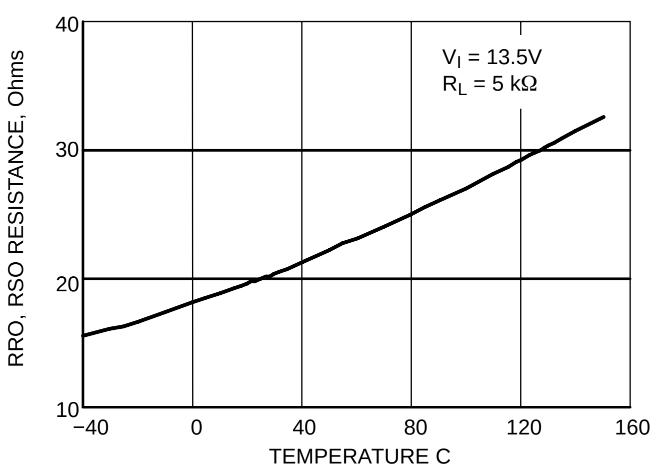


Figure 14. RRO, RSO Resistance vs. Temperature

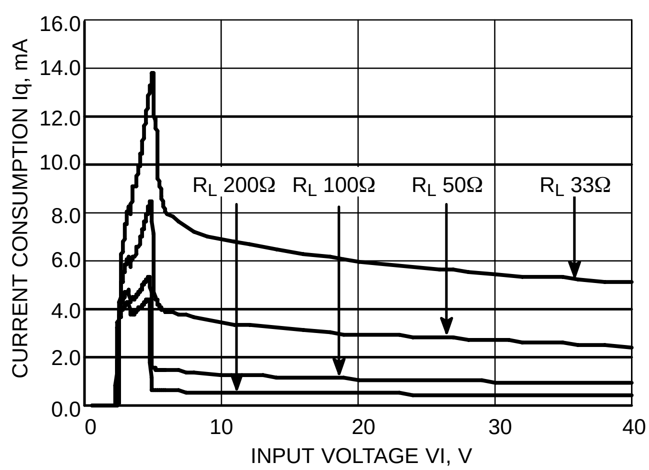


Figure 15. Current Consumption Iq vs. Input Voltage VI

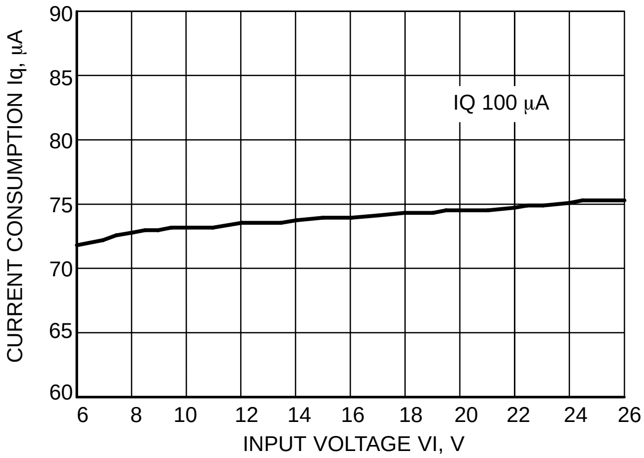


Figure 16. Current Consumption Iq vs. Input Voltage VI

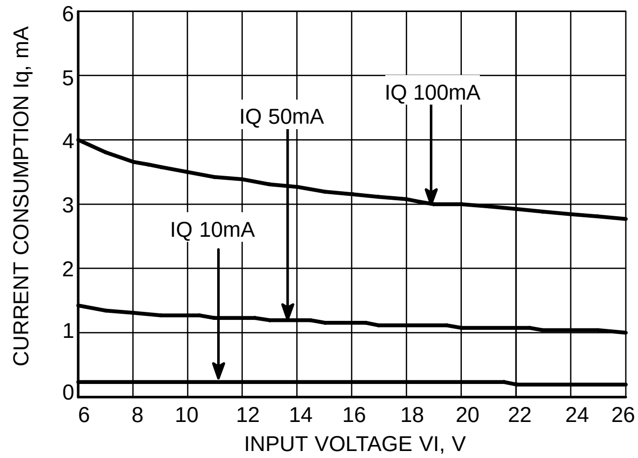


Figure 17. Current Consumption Iq vs. Input Voltage VI

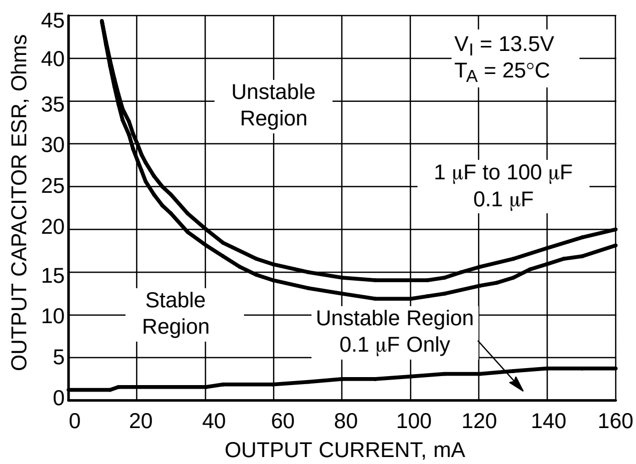


Figure 18. Stability vs. Output Capacitor ESR

TYPICAL PERFORMANCE CHARACTERISTICS − 3.3 V OPTION

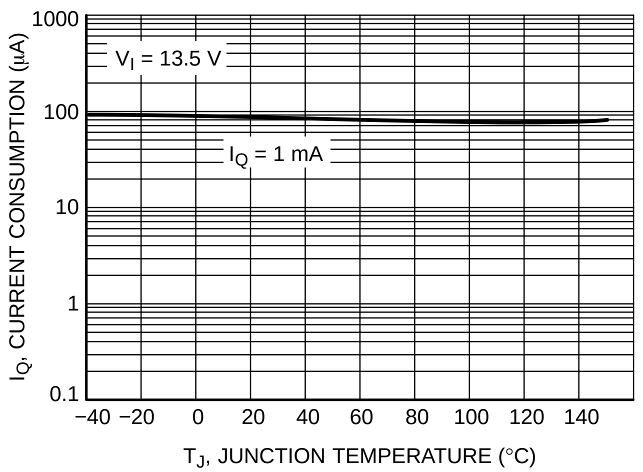


Figure 19. Current Consumption vs. Junction Temperature

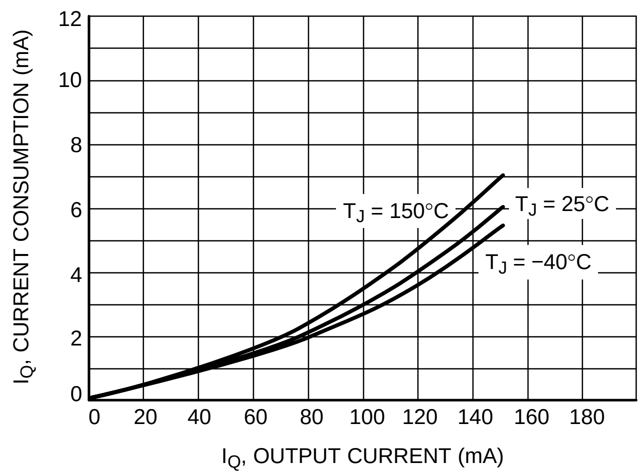


Figure 20. Current Consumption vs. Output Current

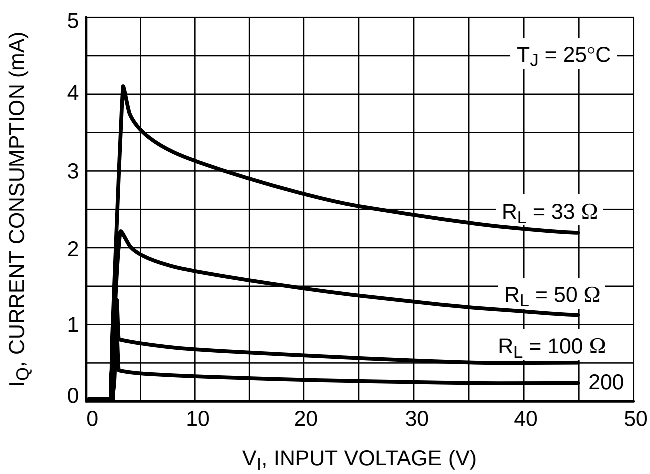


Figure 21. Current Consumption vs. Input Voltage

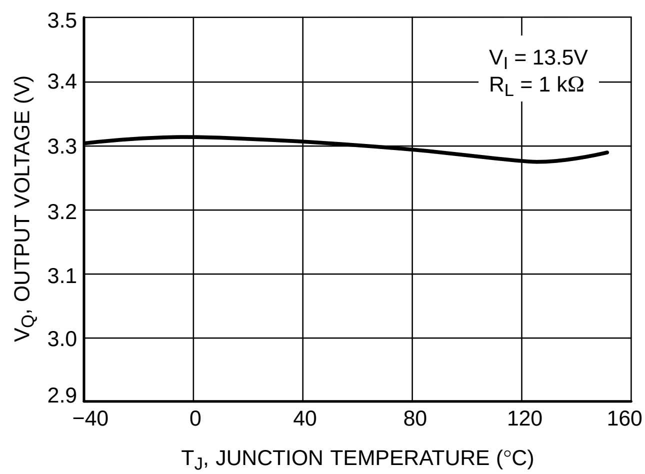


Figure 22. Output Voltage vs. Junction Temperature

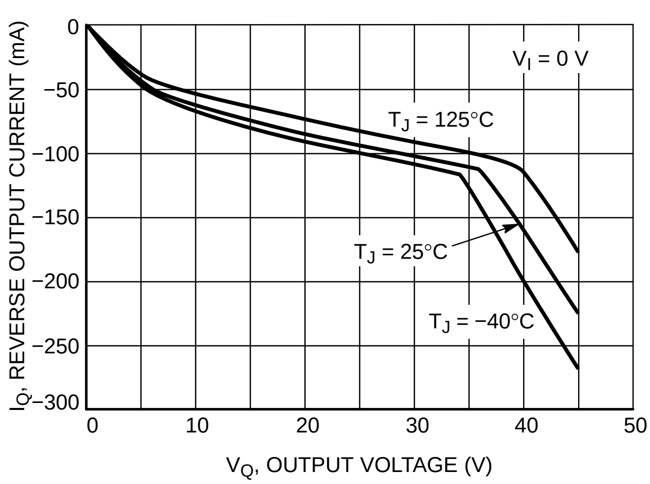


Figure 23. Reverse Output Current vs. Output Voltage

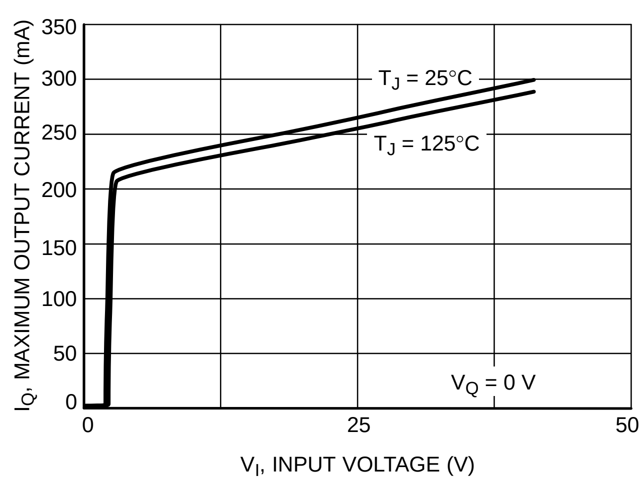


Figure 24. Maximum Output Current vs. Input Voltage

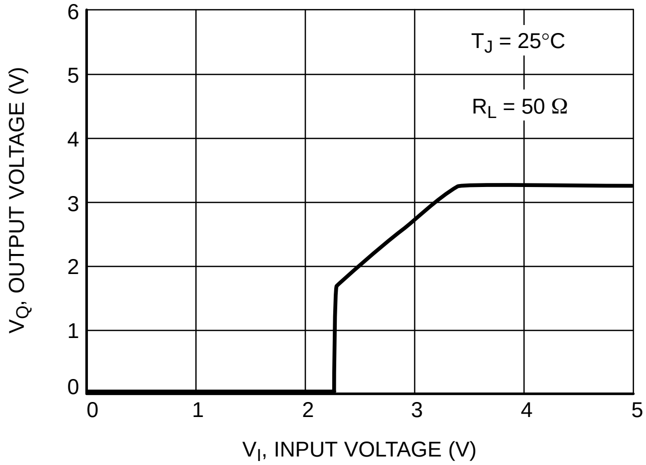


Figure 25. Output Voltage at Input Voltage Extremes

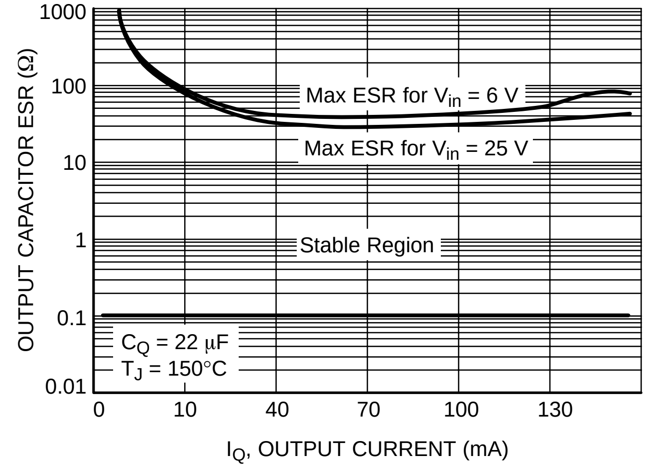


Figure 26. 3.3 V Output Stability with Output Capacitor ESR

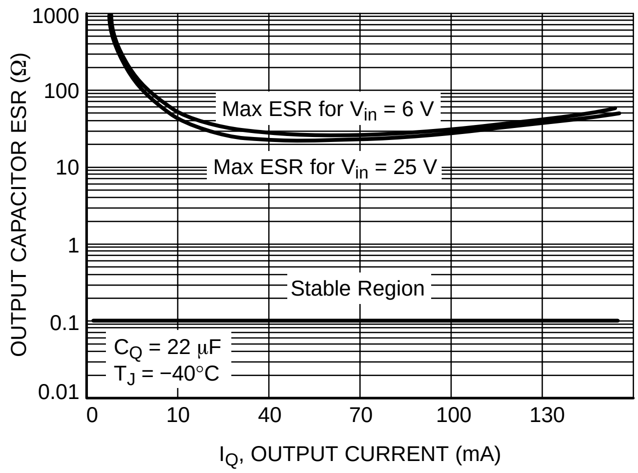


Figure 27. 3.3 V Output Stability with Output Capacitor ESR

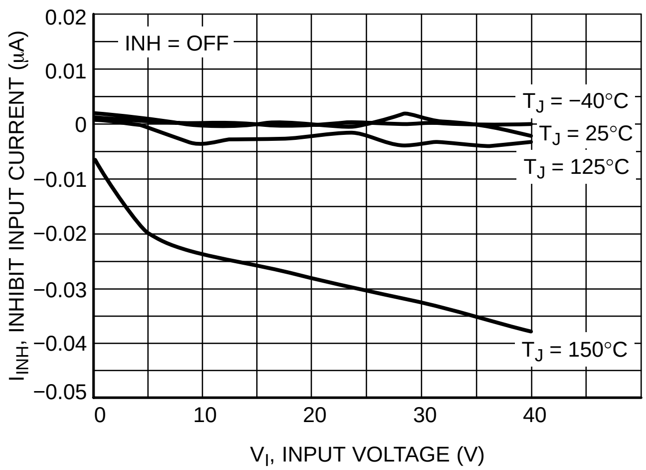


Figure 28. Inhibit Input Current at Input Voltage Extremes

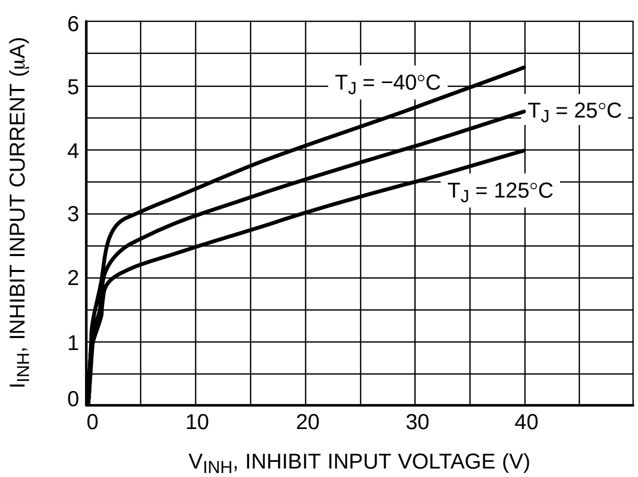


Figure 29. Inhibit Input Current at Inhibit Input Voltage Extremes

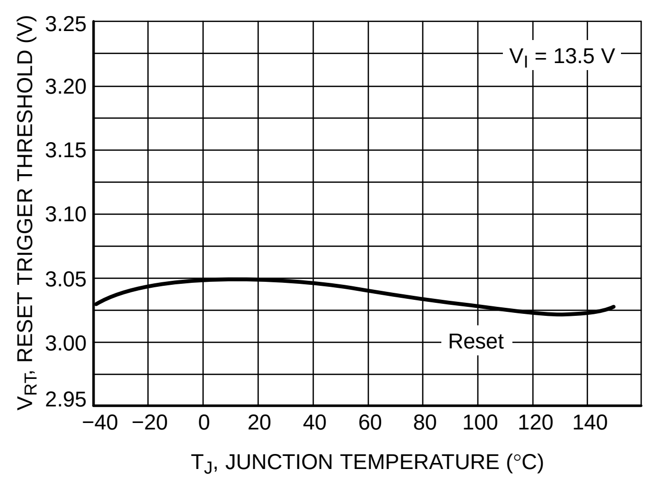


Figure 30. Reset Trigger Threshold vs. Junction Temperature

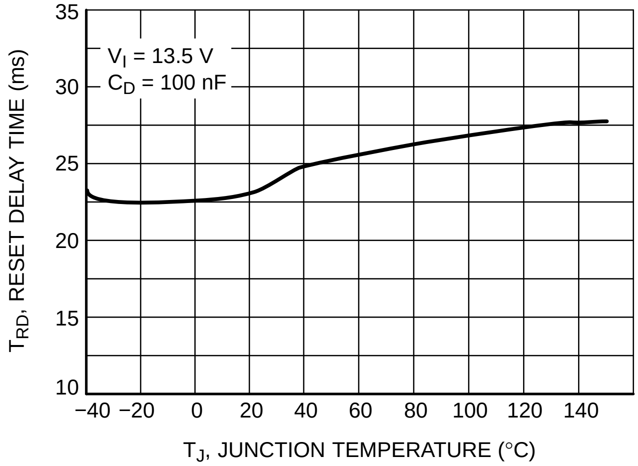


Figure 31. Reset Delay Time vs. Junction Temperature

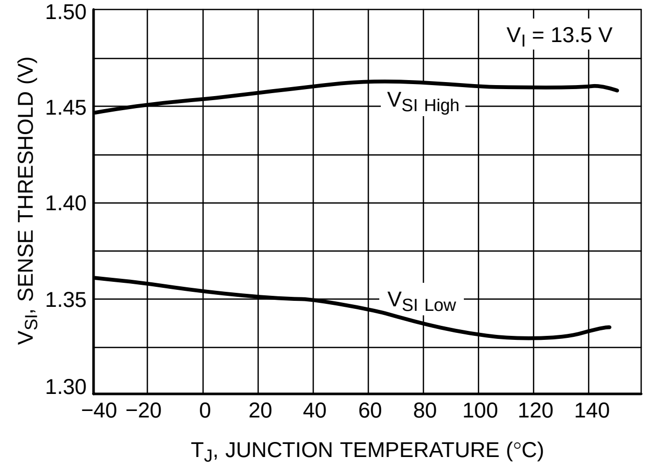


Figure 32. Sense Threshold vs. Junction Temperature

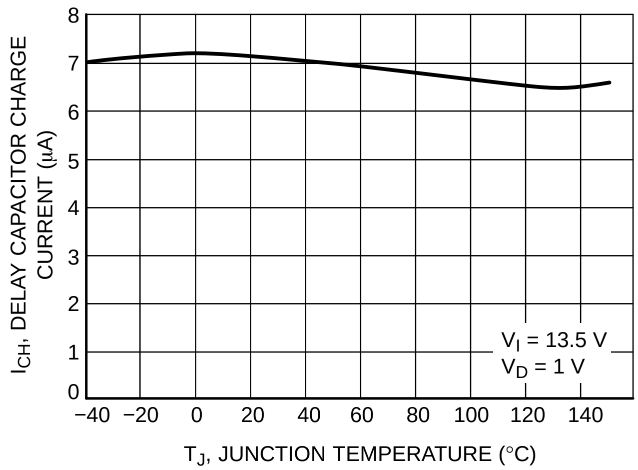


Figure 33. Delay Capacitor Charge Current vs. Junction Temperature

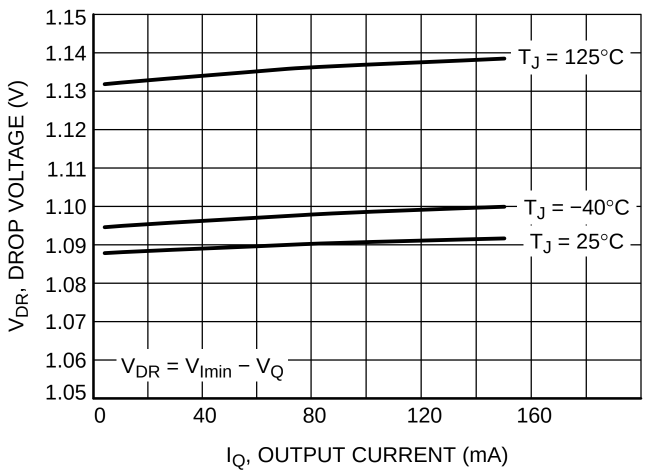


Figure 34. Drop Voltage vs. Output Current

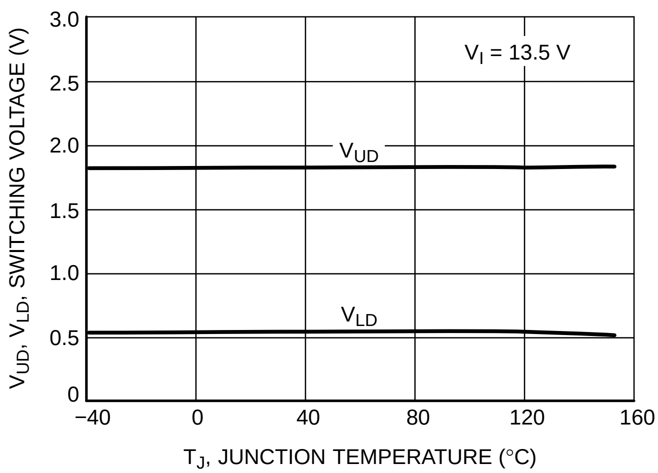


Figure 35. Switching Voltage V_{UD} and V_{LD} vs. Junction Temperature

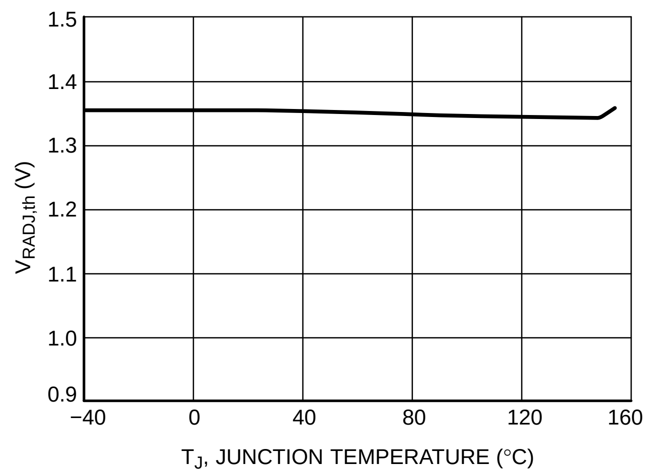


Figure 36. Reset Adjust Switching Threshold vs. Junction Temperature

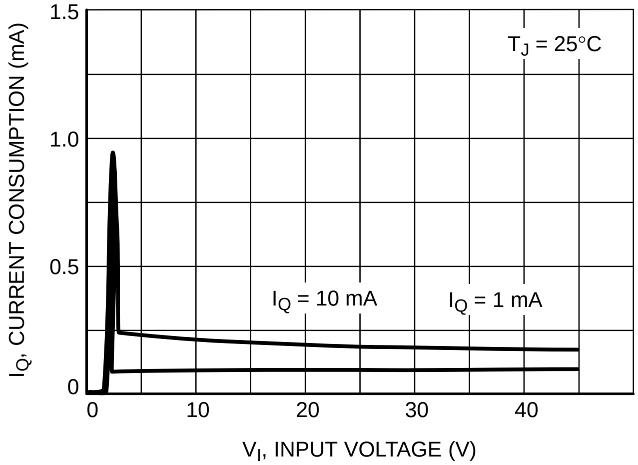


Figure 37. Current Consumption vs. Input Voltage

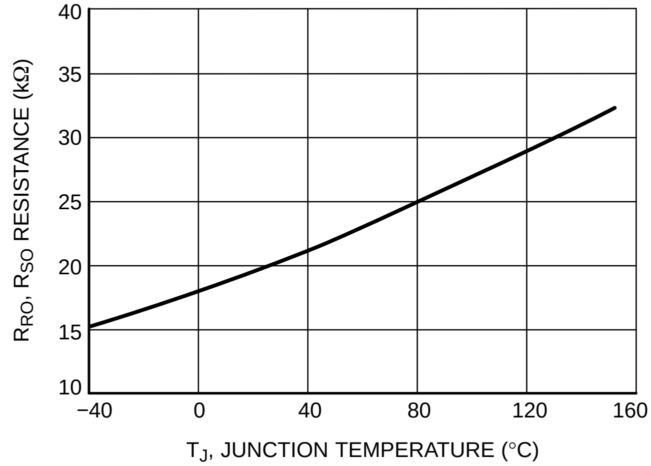


Figure 38. R_{RO}, R_{SO} Resistance vs. Junction Temperature

APPLICATION DESCRIPTION

NCV4299

The NCV4299 is a family of precision micropower voltage regulators with an output current capability of 150 mA at 5.0 V and 3.3 V.

The output voltage is accurate within ±2% with a maximum dropout voltage of 0.5 V at 100 mA. Low quiescent current is a feature drawing only 90 μA with a 100 μA load. This part is ideal for any and all battery operated microprocessor equipment.

Microprocessor control logic includes an active reset output RO (with delay), and a SI/SO monitor which can be used to provide an early warning signal to the microprocessor of a potential impending reset signal. The use of the SI/SO monitor allows the microprocessor to finish any signal processing before the reset shuts the microprocessor down. Internal output resistors on the RO and SO pins pulling up to the output pin Q reduce external component count. An inhibit function is available on the 14−lead part. With inhibit active, the regulator turns off and the device consumes less that 1.0 μA of quiescent current.

The active reset circuit operates correctly at an output voltage as low as 1.0 V. The reset function is activated during the powerup sequence or during normal operation if the output voltage drops outside the regulation limits.

The reset threshold voltage can be decreased by the connection of an external resistor divider to the RADJ lead. The regulator is protected against reverse battery, short circuit, and thermal overload conditions. The device can withstand load dump transients making it suitable for use in automotive environments.

NCV4299 Circuit Description

The low dropout regulator in the NCV4299 uses a PNP pass transistor to give the lowest possible dropout voltage capability. The current is internally monitored to prevent oversaturation of the device and to limit current during over current conditions. Additional circuitry is provided to protect the device during overtemperature operation.

The regulator provides an output regulated to 2%.

Other features of the regulator include an undervoltage reset function and a sense circuit. The reset function has an adjustable time delay and an adjustable threshold level. The sense circuit trip level is adjustable and can be used as an early warning signal to the controller. An inhibit function that turns off the regulator and reduces the current consumption to less than 1.0 μA is a feature available in the 14 pin package.

Output Regulator

The output is controlled by a precision trimmed reference. The PNP output has saturation control for regulation while the input voltage is low, preventing oversaturation. Current limit and voltage monitors complement the regulator design to give safe operating signals to the processor and control circuits.

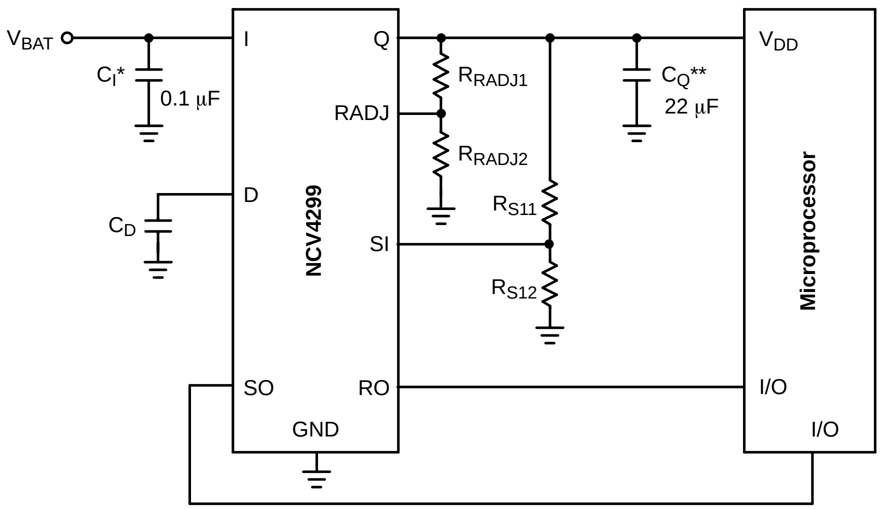
Stability Considerations

The input capacitor C_I is necessary for compensating input line reactance. Possible oscillations caused by input inductance and input capacitance can be damped by using a resistor of approximately 1.0 Ω in series with C_I.

The output or compensation capacitor helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability.

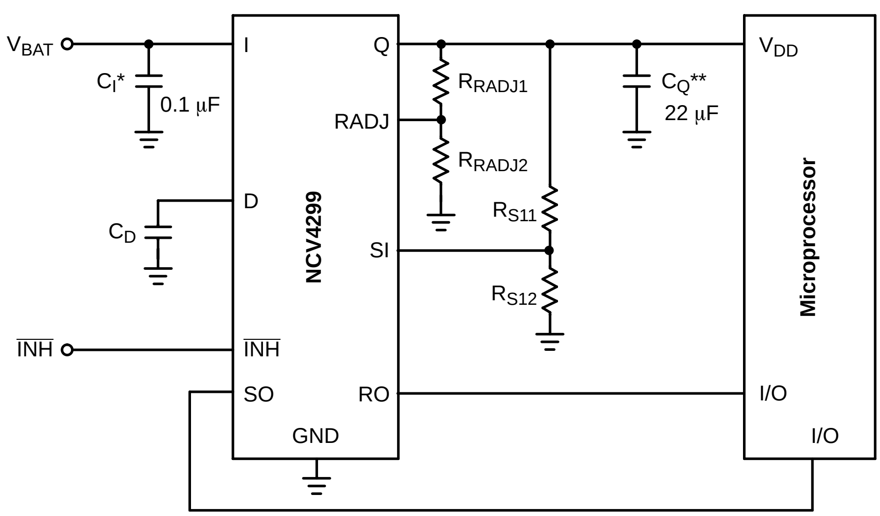
The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer’s data sheet usually provides this information.

The value for the output capacitor C_Q shown in Figures 39 and 40 should work for most applications, however, it is not necessarily the optimized solution. Stability is guaranteed at values $C_Q \geq 22$ μF and an ESR ≤ 5.0 Ω within the operating temperature range. Actual limits are shown in a graph in the typical performance characteristics section.



*C_I required if regulator is located far from the power supply filter.
**C_Q required for stability. Cap must operate at minimum temperature expected.

Figure 39. Test and Application Circuit Showing all Compensation and Sense Elements for the 8 Pin Package Part



*C_I required if regulator is located far from the power supply filter.
**C_Q required for stability. Cap must operate at minimum temperature expected.

Figure 40. Test and Application Circuit Showing all Compensation and Sense Elements for the 14 Pin Package Part with Inhibit Function

Reset Output (RO)

A reset signal, Reset Output (RO, low voltage) is generated as the IC powers up. After the output voltage V_Q increases above the reset threshold voltage V_{RT}, the delay timer D is started. When the voltage on the delay timer V_D passes V_{UD}, the reset signal RO goes high. A discharge of the delay timer (V_D) is started when V_Q drops and stays below the reset threshold voltage V_{RT}. When the voltage of the delay timer (V_D) drops below the lower threshold voltage V_{LD}, the reset output voltage V_{RO} is brought low to reset the processor.

The reset output RO is an open collector NPN transistor, controlled by a low voltage detection circuit. The circuit is functionally independent of the rest of the IC, thereby guaranteeing that RO is valid for V_Q as low as 1.0 V.

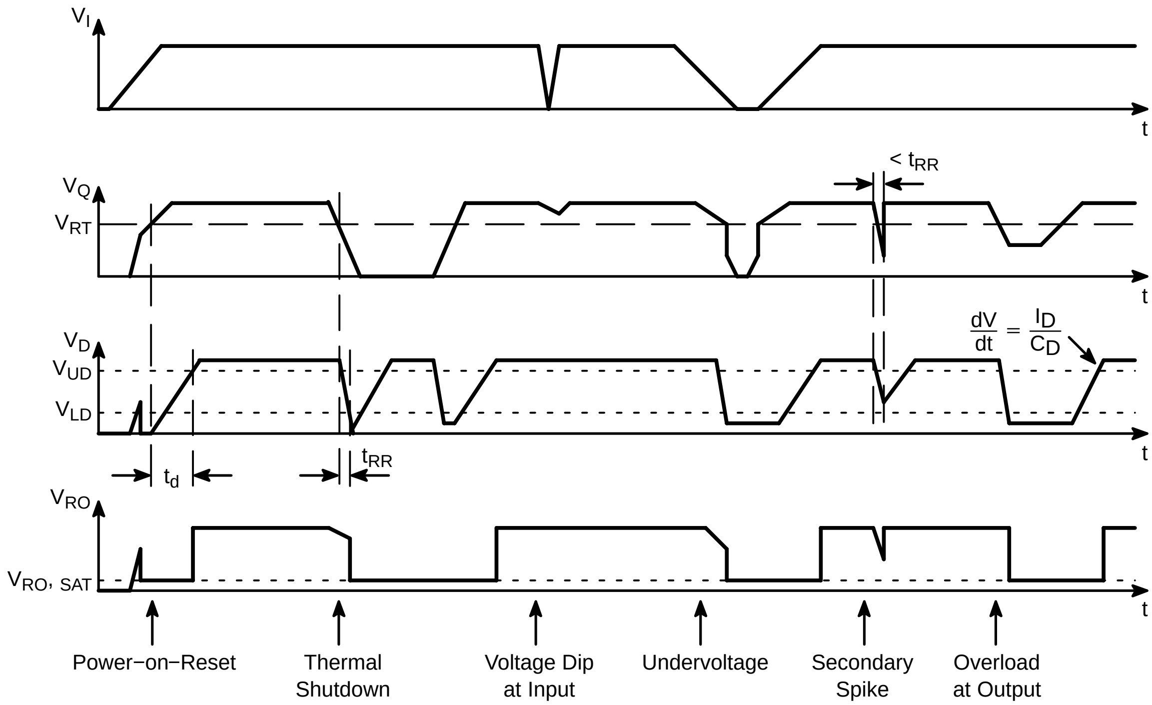


Figure 41. Reset Timing Diagram

Reset Adjust (RADJ)

The reset threshold V_{RT} can be decreased from a typical value of 4.65 V to as low as 3.5 V by using an external voltage divider connected from the Q lead to the pin RADJ, as shown in Figures 39 and 40. The resistor divider keeps the voltage above the $V_{RADJ,TH}$, (typ. 1.35 V), for the desired input voltages and overrides the internal threshold detector. Adjust the voltage divider according to the following relationship:

$$V_{THRES} = V_{RADJ,TH} \cdot (R_{ADJ1} + R_{ADJ2})/R_{ADJ2} \quad \text{(eq. 1)}$$

If the reset adjust option is not needed, the RADJ−pin should be connected to GND causing the reset threshold to go to its default value (typ. 4.65 V).

Reset Delay (D)

The reset delay circuit provides a delay (programmable by capacitor C_D) on the reset output RO lead. The delay lead D provides charge current I_D (typically 8.0 mA) to the external delay capacitor C_D during the following times:

1. During Powerup (once the regulation threshold has been exceeded).
2. After a reset event has occurred and the device is back in regulation. The delay capacitor is set to discharge when the regulation (V_{RT}, reset threshold voltage) has been violated. When the delay capacitor discharges to down to V_{LD}, the reset signal RO pulls low.

Setting the Delay Time

The delay time is set by the delay capacitor C_D and the charge current I_D. The time is measured by the delay capacitor voltage charging from the low level of $V_{D,sat}$ to the higher level V_{UD}. The time delay follows the equation:

$$t_d = [C_D (V_{UD} - V_{D,sat})]/I_D \quad \text{(eq. 2)}$$

Example:

Using C_D = 100 nF.
Use the typical value for $V_{D,sat}$ = 0.1 V.
Use the typical value for V_{UD} = 1.8 V.
Use the typical value for Delay Charge Current I_D = 6.5 μA.

$$t_d = [100\ \text{nF}(1.8 - 0.1\ \text{V})]/6.5\ \mu\text{A} = 26.2\ \text{ms} \quad \text{(eq. 3)}$$

When the output voltage V_Q drops below the reset threshold voltage V_{RT}, the voltage on the delay capacitor V_D starts to drop. The time it takes to drop below the lower threshold voltage of V_{LD} is the reset reaction time, t_{RR}. This time is typically 1.0 μs for a delay capacitor of 0.1 μF. The reset reaction time can be estimated from the following relationship:

$$t_{RR} = 10\ \text{ns/nF} \times C_D \quad \text{(eq. 4)}$$

Sense Input (SI)/Sense Output (SO) Voltage Monitor

An on−chip comparator is available to provide early warning to the microprocessor of a possible reset signal. The reset signal typically turns the microprocessor off instantaneously. This can cause unpredictable results with the microprocessor. The signal received from the SO pin will allow the microprocessor time to complete its present task before shutting down. This function is performed by a comparator referenced to the band gap voltage. The actual trip point can be programmed externally using a resistor divider to the input monitor (SI) (Figures 39 and 40). The typical threshold is 1.35 V on the SI Pin.

Signal Output

Figure 42 shows the SO Monitor waveforms as a result of the circuits depicted in Figures 39 and 40. As the output voltage V_Q falls, the monitor threshold $V_{SI,LOW}$ is crossed. This causes the voltage on the SO output to go low sending a warning signal to the microprocessor that a reset signal may occur in a short period of time. $T_{WARNING}$ is the time the microprocessor has to complete the function it is currently working on and get ready for the reset shutdown signal.

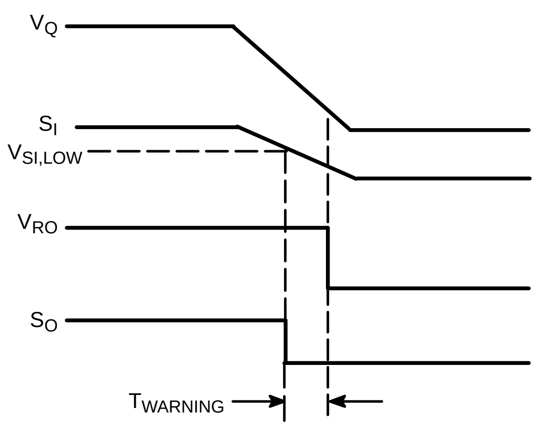


Figure 42. SO Warning Timing Waveform

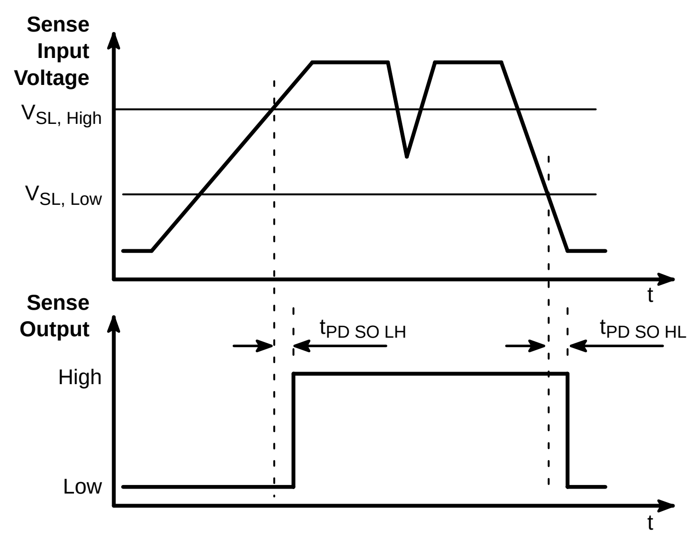


Figure 43. Sense Timing Diagram

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator is:

$$P_{D(max)} = [V_{I(max)} - V_{Q(min)}]\, I_{Q(max)} + V_{I(max)} I_q \quad \text{(eq. 5)}$$

where:

$V_{I(max)}$ is the maximum input voltage,
$V_{Q(min)}$ is the minimum output voltage,
$I_{Q(max)}$ is the maximum output current for the application, and
I_q is the quiescent current the regulator consumes at $I_{Q(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = (150^\circ\text{C} - T_A)/P_D \quad \text{(eq. 6)}$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in Equation 6 will keep the die temperature below 150°C. In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

Heatsinks

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad \text{(eq. 7)}$$

where:

$R_{\theta JC}$ = the junction−to−case thermal resistance,
$R_{\theta CS}$ = the case−to−heatsink thermal resistance, and
$R_{\theta SA}$ = the heatsink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heatsink data sheets of heatsink manufacturers. Thermal, mounting, and heatsinking are discussed in the ON Semiconductor application note AN1040/D, available on the ON Semiconductor website.

SOIC 8 LEAD

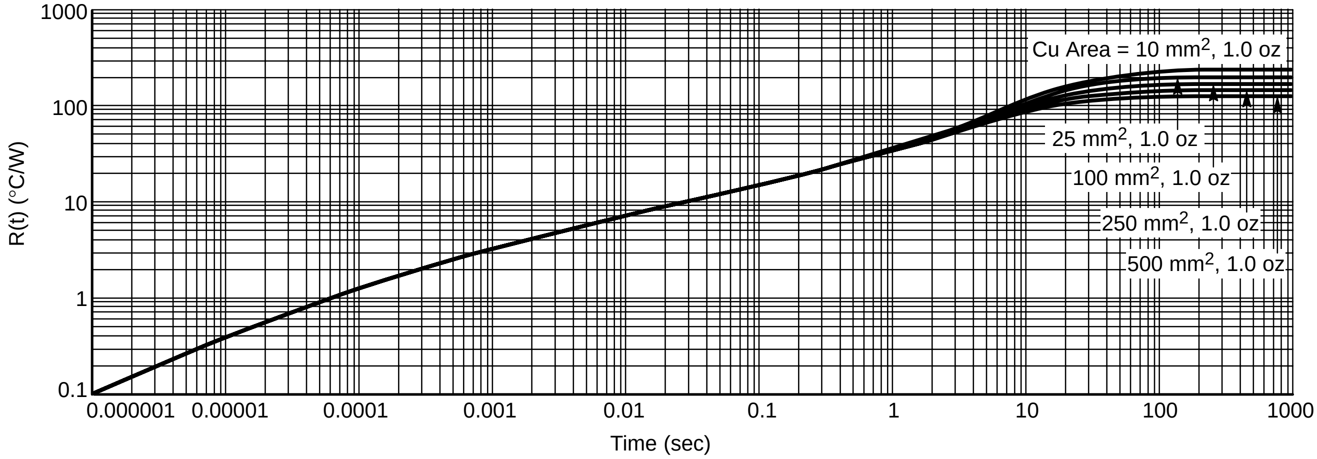


Figure 44. Transient Thermal Response Simulation to a Single Pulse 1 oz (Log−Log)

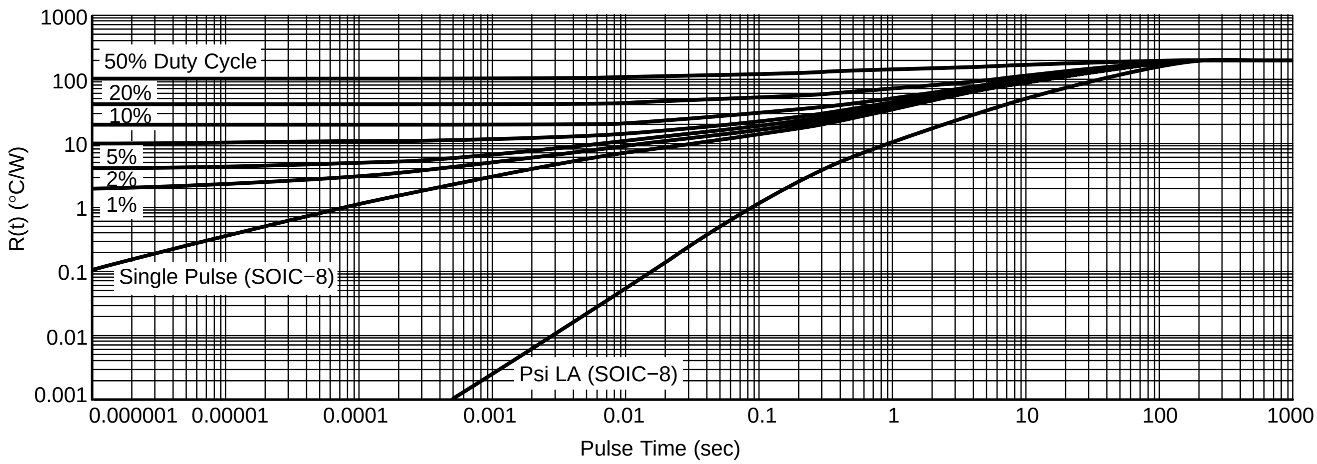


Figure 45. Transient Thermal Response Simulation to a Single Pulse with Duty Cycles Applied (Log−Log) (PCB = 50 mm^2 1 oz)

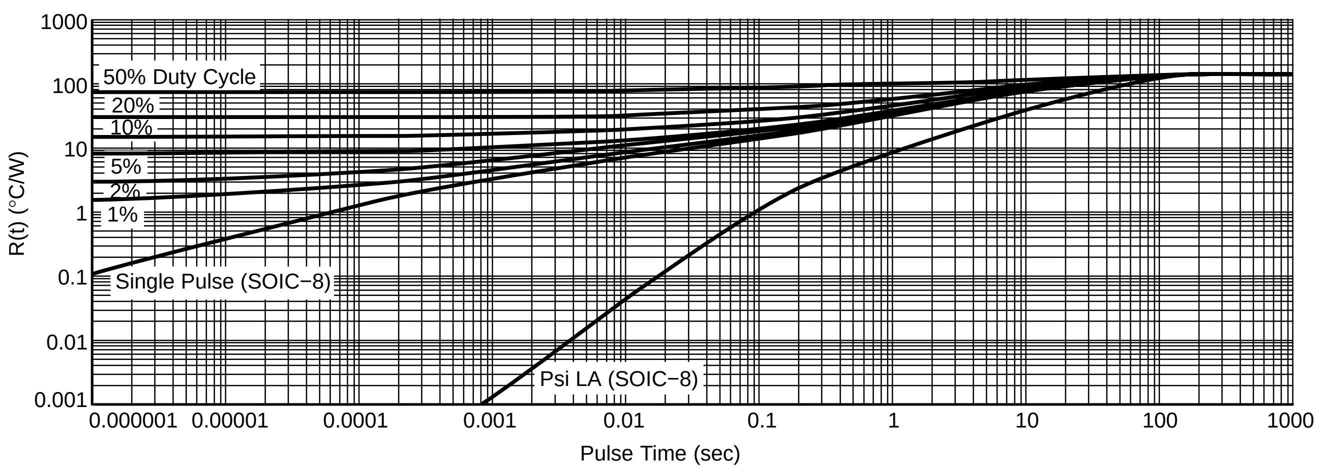


Figure 46. Transient Thermal Response Simulation to a Single Pulse with Duty Cycles Applied (Log−Log) (PCB = 250 mm^2 1 oz)

SOIC 14 LEAD

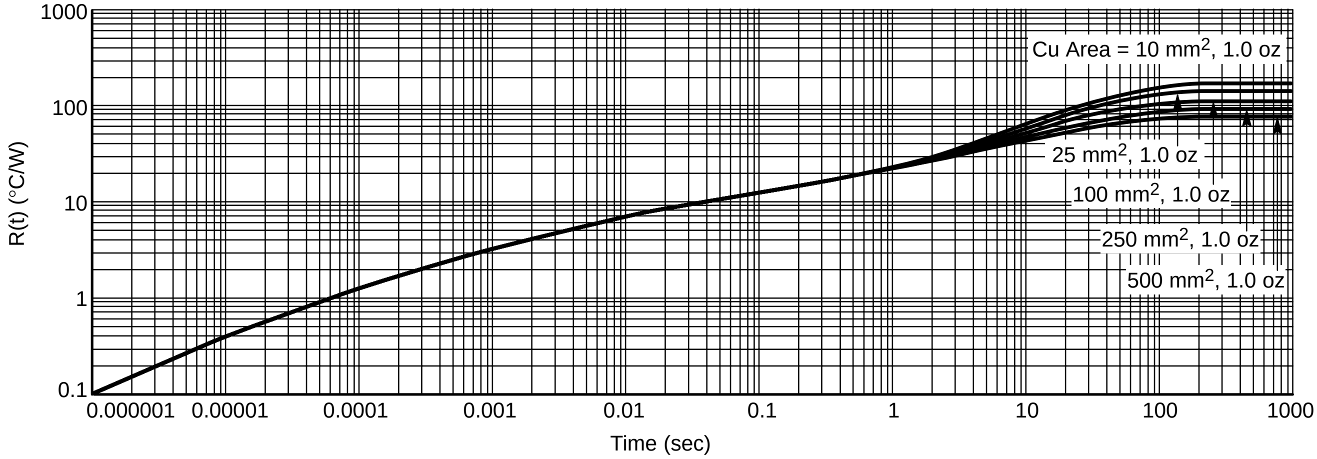


Figure 47. Transient Thermal Response Simulation to a Single Pulse 1 oz (Log−Log)

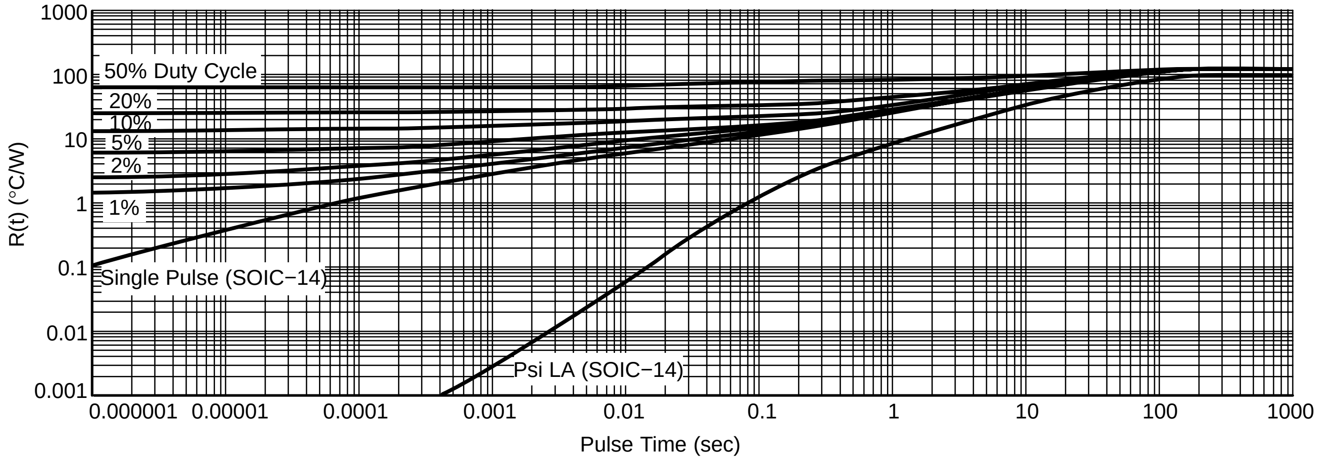


Figure 48. Transient Thermal Response Simulation to a Single Pulse with Duty Cycles Applied (Log−Log) (PCB = 50 mm^2 1 oz)

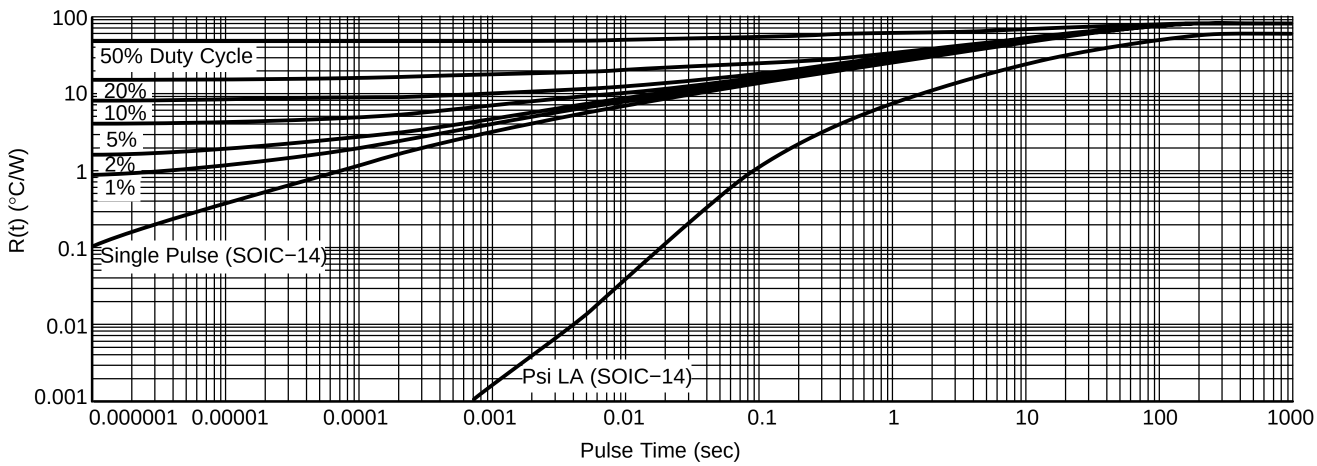


Figure 49. Transient Thermal Response Simulation to a Single Pulse with Duty Cycles Applied (Log−Log) (PCB = 250 mm^2 1 oz)

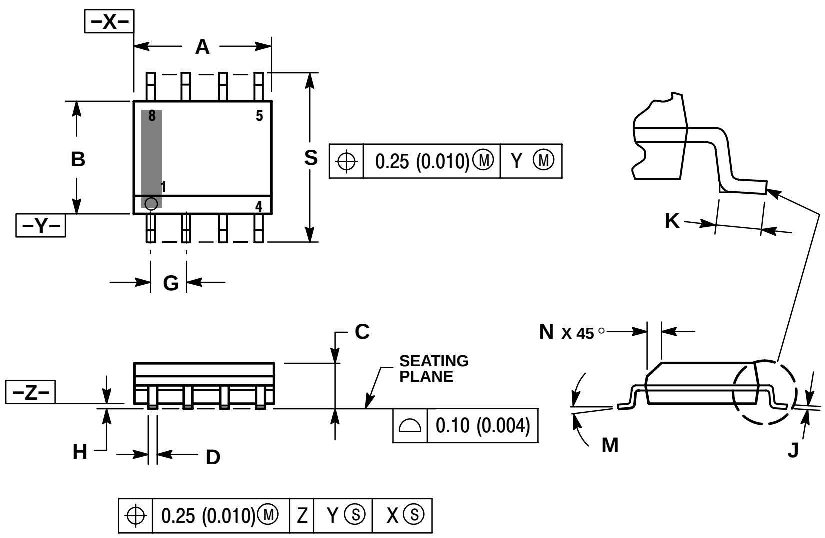
ORDERING INFORMATION

Device	Package	Shipping†
NCV4299D1	SO−8	98 Units/Rail
NCV4299D1G	SO−8 (Pb−Free)	98 Units/Rail
NCV4299D1R2	SO−8	2500 Tape & Reel
NCV4299D1R2G	SO−8 (Pb−Free)	2500 Tape & Reel
NCV4299D2	SO−14	55 Units/Rail
NCV4299D2G	SO−14 (Pb−Free)	55 Units/Rail
NCV4299D2R2	SO−14	2500 Tape & Reel
NCV4299D2R2G	SO−14 (Pb−Free)	2500 Tape & Reel
NCV4299D233G	SO−14 (Pb−Free)	55 Units/Rail
NCV4299D233R2G	SO−14 (Pb−Free)	2500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

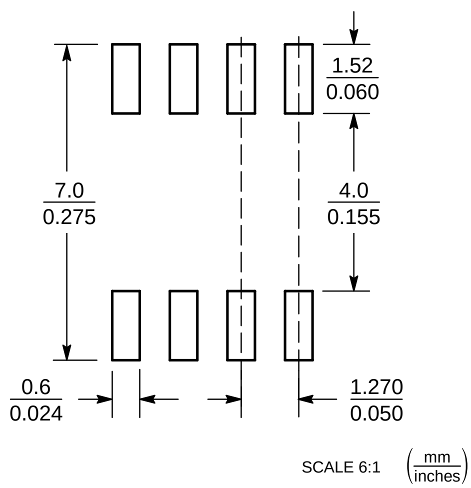
SOIC−8 NB
CASE 751−07
ISSUE AH



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

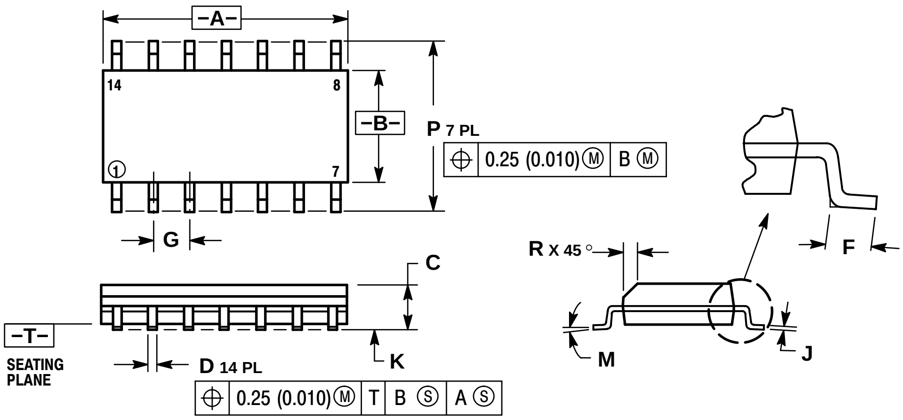
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

SO−14
D SUFFIX
CASE 751A−03
ISSUE G



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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For additional information, please contact your local Sales Representative.