

NCV8402D

Dual Self-Protected Low-Side Driver with Temperature and Current Limit

NCV8402D is a dual protected Low-Side Smart Discrete device. The protection features include overcurrent, overtemperature, ESD and integrated Drain-to-Gate clamping for overvoltage protection. This device offers protection and is suitable for harsh automotive environments.

Features

- Short-Circuit Protection
- Thermal Shutdown with Automatic Restart
- Overvoltage Protection
- Integrated Clamp for Inductive Switching
- ESD Protection
- dV/dt Robustness
- Analog Drive Capability (Logic Level Input)
- AEC-Q101 Qualified
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Control
- These Devices are Pb-Free and are RoHS Compliant

Typical Applications

- Switch a Variety of Resistive, Inductive and Capacitive Loads
- Can Replace Electromechanical Relays and Discrete Circuits
- Automotive / Industrial

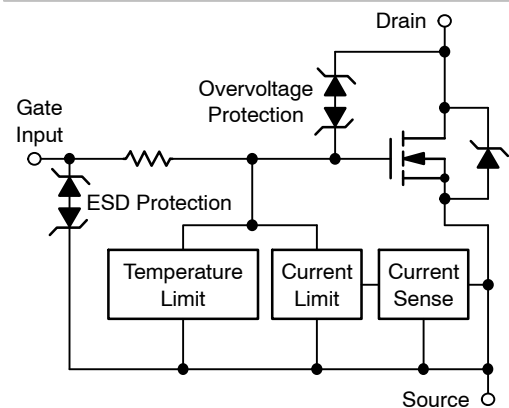


ON Semiconductor®

<http://onsemi.com>

$V_{(BR)DSS}$ (Clamped)	$R_{DS(ON)}$ TYP	I_D MAX
42 V	165 mΩ @ 10 V	2.0 A*

*Max current limit value is dependent on input condition.

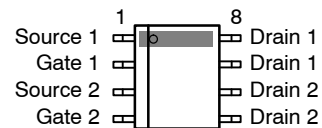


MARKING DIAGRAM



V8402D = Specific Device Code
 A = Assembly Location
 L = Wafer Lot
 Y = Year
 W = Work Week
 ■ = Pb-Free Package

PIN ASSIGNMENT



ORDERING INFORMATION

Device	Package	Shipping†
NCV8402DDR2G	SOIC-8 (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NCV8402D

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage Internally Clamped	V_{DSS}	42	V
Drain-to-Gate Voltage Internally Clamped ($R_G = 1.0\text{ M}\Omega$)	V_{DGR}	42	V
Gate-to-Source Voltage	V_{GS}	± 14	V
Continuous Drain Current	I_D	Internally Limited	
Power Dissipation	P_D	0.8 1.62	W
Thermal Resistance	Junction-to-Ambient Steady State (Note 1)	$R_{\theta JA}$	157
	Junction-to-Ambient Steady State (Note 2)	$R_{\theta JA}$	77
Single Pulse Drain-to-Source Avalanche Energy ($V_{DD} = 32\text{ V}$, $V_G = 5.0\text{ V}$, $I_{PK} = 1.0\text{ A}$, $L = 300\text{ mH}$, $R_{G(ext)} = 25\ \Omega$)	E_{AS}	150	mJ
Load Dump Voltage ($V_{GS} = 0$ and 10 V , $R_I = 2.0\ \Omega$, $R_L = 9.0\ \Omega$, $t_d = 400\text{ ms}$)	V_{LD}	87	V
Operating Junction and Storage Temperature	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface-mounted onto min pad FR4 PCB, (Cu area = 40 sq. mm, 1 oz.).
2. Surface-mounted onto 1" sq. FR4 board (Cu area = 625 sq. mm, 2 oz.).

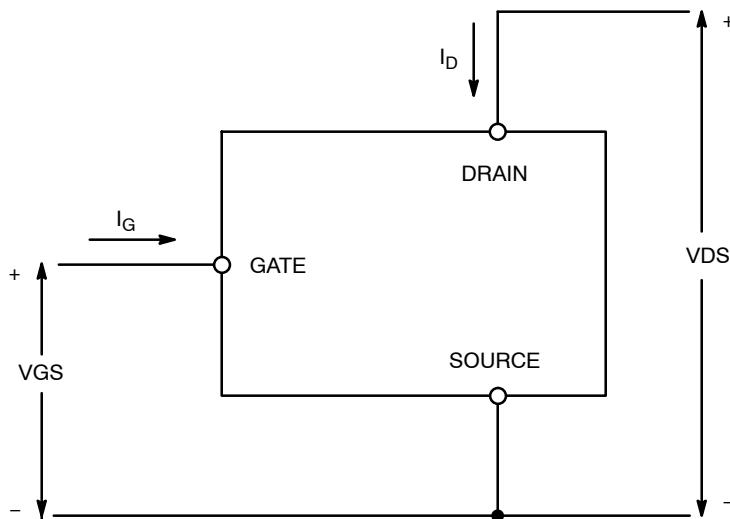


Figure 1. Voltage and Current Convention

NCV8402D

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Test Condition	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage (Note 3)	V _{GS} = 0 V, I _D = 10 mA, T _J = 25°C	V _{(BR)DSS}	42	46	55	V
	V _{GS} = 0 V, I _D = 10 mA, T _J = 150°C (Note 5)		40	45	55	
Zero Gate Voltage Drain Current	V _{GS} = 0 V, V _{DS} = 32 V, T _J = 25°C	I _{DSS}		0.25	4.0	μA
	V _{GS} = 0 V, V _{DS} = 32 V, T _J = 150°C (Note 5)			1.1	20	
Gate Input Current	V _{DS} = 0 V, V _{GS} = 5.0 V	I _{GSSF}		50	100	μA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 150 μA	V _{GS(th)}	1.3	1.8	2.2	V
Gate Threshold Temperature Coefficient		V _{GS(th)} /T _J		4.0	6.0	-mV/°C
Static Drain-to-Source On-Resistance	V _{GS} = 10 V, I _D = 1.7 A, T _J = 25°C	R _{DS(on)}		165	200	mΩ
	V _{GS} = 10 V, I _D = 1.7 A, T _J = 150°C (Note 5)			305	400	
	V _{GS} = 5.0 V, I _D = 1.7 A, T _J = 25°C			195	230	
	V _{GS} = 5.0 V, I _D = 1.7 A, T _J = 150°C (Note 5)			360	460	
	V _{GS} = 5.0 V, I _D = 0.5 A, T _J = 25°C			190	230	
	V _{GS} = 5.0 V, I _D = 0.5 A, T _J = 150°C (Note 5)			350	460	
Source-Drain Forward On Voltage	V _{GS} = 0 V, I _S = 7.0 A	V _{SD}		1.0		V

SWITCHING CHARACTERISTICS (Note 5)

Turn-ON Time (10% V _{IN} to 90% I _D)	V _{GS} = 10 V, V _{DD} = 12 V I _D = 2.5 A, R _L = 4.7 Ω	t _{ON}		25		μs
Turn-OFF Time (90% V _{IN} to 10% I _D)		t _{OFF}		120		
Slew-Rate ON (70% V _{DS} to 50% V _{DS})	V _{GS} = 10 V, V _{DD} = 12 V, R _L = 4.7 Ω	-dV _{DS} /dt _{ON}		0.8		V/μs
Slew-Rate OFF (50% V _{DS} to 70% V _{DS})		dV _{DS} /dt _{OFF}		0.3		

SELF PROTECTION CHARACTERISTICS (T_J = 25°C unless otherwise noted) (Note 4)

Current Limit	V _{DS} = 10 V, V _{GS} = 5.0 V, T _J = 25°C	I _{LIM}	3.7	4.3	5.0	A
	V _{DS} = 10 V, V _{GS} = 5.0 V, T _J = 150°C (Note 5)		2.3	3.0	3.7	
	V _{DS} = 10 V, V _{GS} = 10 V, T _J = 25°C		4.2	4.8	5.4	
	V _{DS} = 10 V, V _{GS} = 10 V, T _J = 150°C (Note 5)		2.7	3.6	4.5	
Temperature Limit (Turn-off)	V _{GS} = 5.0 V (Note 5)	T _{LIM(off)}	150	175	200	°C
Thermal Hysteresis	V _{GS} = 5.0 V	ΔT _{LIM(on)}		15		
Temperature Limit (Turn-off)	V _{GS} = 10 V (Note 5)	T _{LIM(off)}	150	165	185	
Thermal Hysteresis	V _{GS} = 10 V	ΔT _{LIM(on)}		15		

GATE INPUT CHARACTERISTICS (Note 5)

Device ON Gate Input Current	V _{GS} = 5 V, I _D = 1.0 A	I _{GON}		50		μA
	V _{GS} = 10 V, I _D = 1.0 A			400		
Current Limit Gate Input Current	V _{GS} = 5 V, V _{DS} = 10 V	I _{GCL}		0.05		mA
	V _{GS} = 10 V, V _{DS} = 10 V			0.4		
Thermal Limit Fault Gate Input Current	V _{GS} = 5 V, V _{DS} = 10 V	I _{GTL}		0.15		mA
	V _{GS} = 10 V, V _{DS} = 10 V			0.7		

ESD ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (Note 5)

Electro-Static Discharge Capability	Human Body Model (HBM)	ESD	4000			V
	Machine Model (MM)		400			

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Fault conditions are viewed as beyond the normal operating range of the part.
5. Not subject to production testing.

TYPICAL PERFORMANCE CURVES

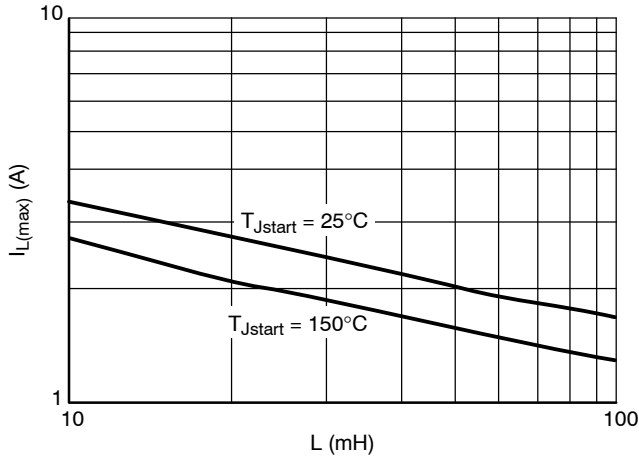


Figure 2. Single Pulse Maximum Switch-off Current vs. Load Inductance

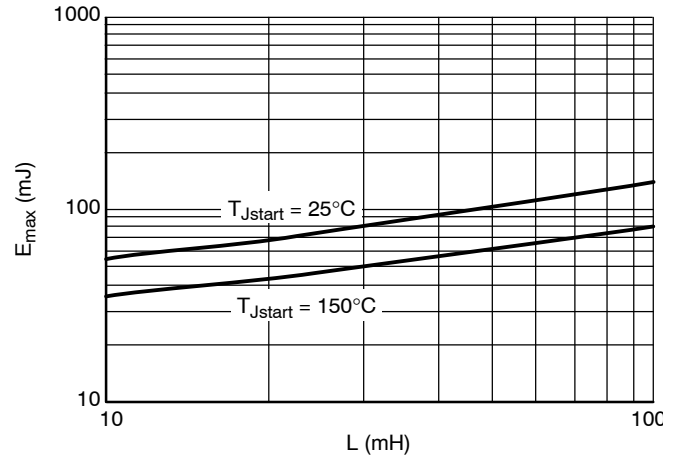


Figure 3. Single Pulse Maximum Switching Energy vs. Load Inductance

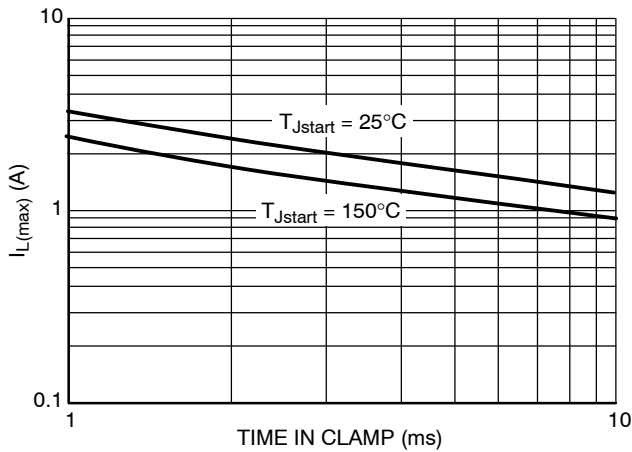


Figure 4. Single Pulse Maximum Inductive Switch-off Current vs. Time in Clamp

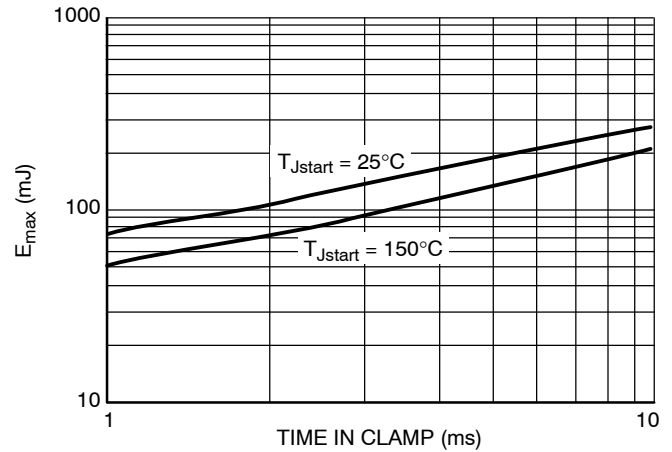


Figure 5. Single Pulse Maximum Inductive Switching Energy vs. Time in Clamp

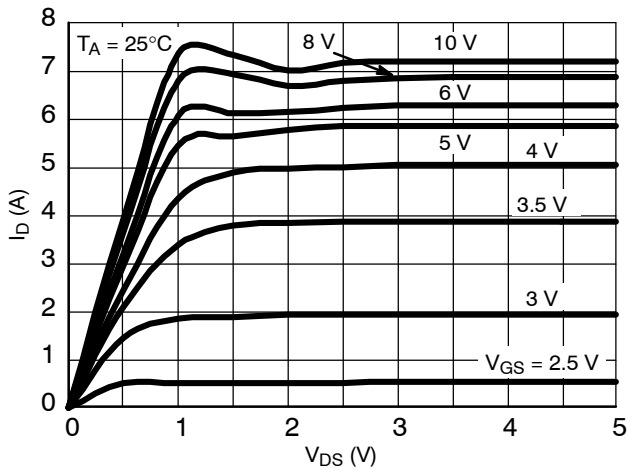


Figure 6. On-state Output Characteristics

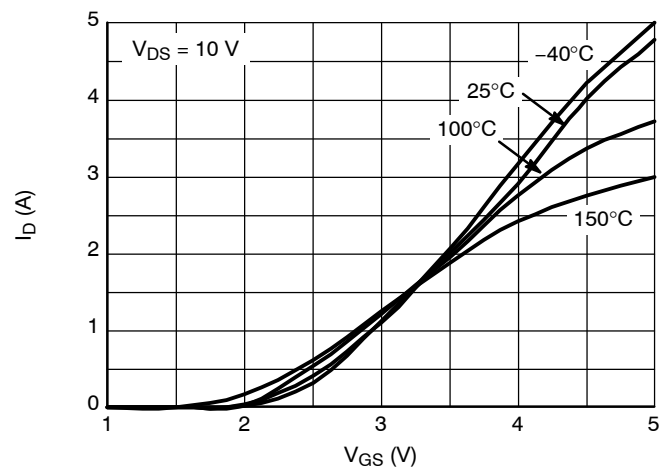


Figure 7. Transfer Characteristics

TYPICAL PERFORMANCE CURVES

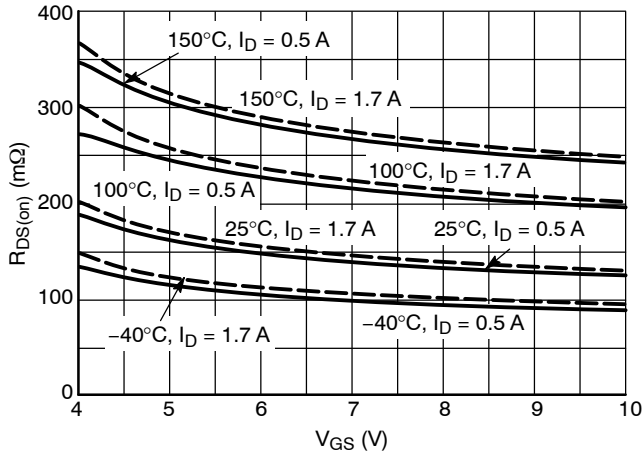


Figure 8. $R_{DS(on)}$ vs. Gate-Source Voltage

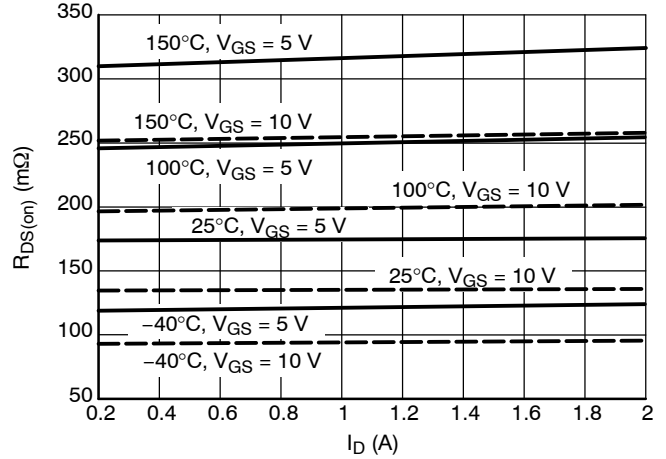


Figure 9. $R_{DS(on)}$ vs. Drain Current

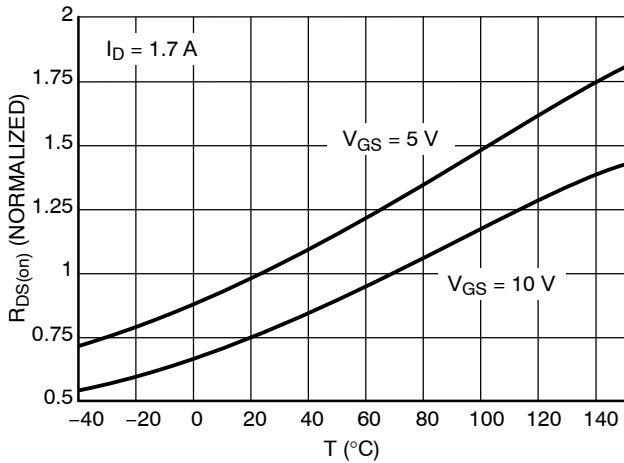


Figure 10. Normalized $R_{DS(on)}$ vs. Temperature

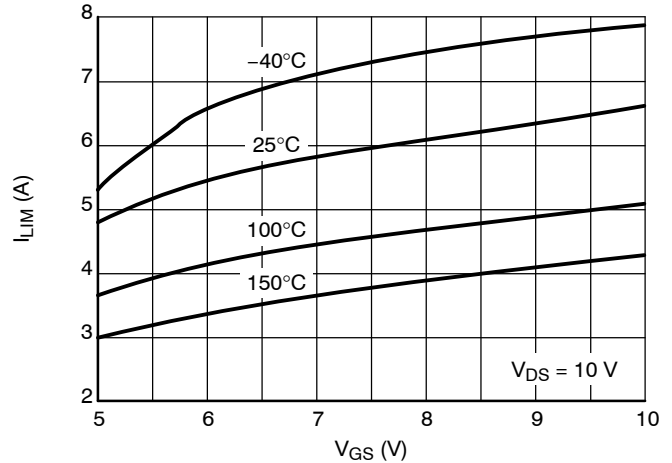


Figure 11. Current Limit vs. Gate-Source Voltage

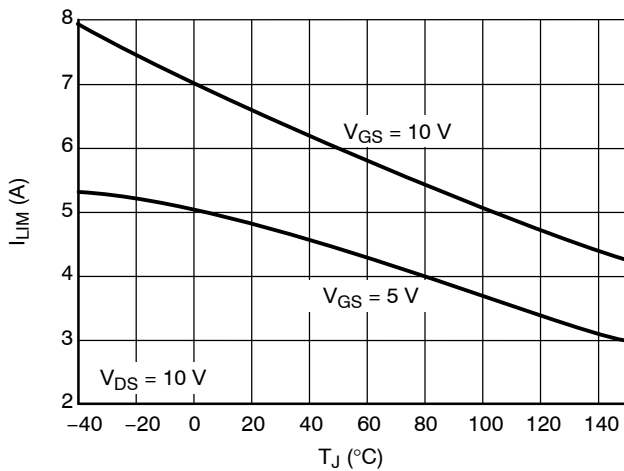


Figure 12. Current Limit vs. Junction Temperature

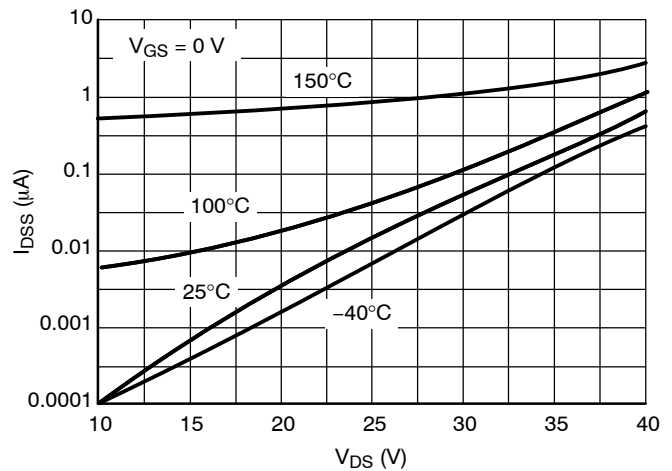


Figure 13. Drain-to-Source Leakage Current

TYPICAL PERFORMANCE CURVES

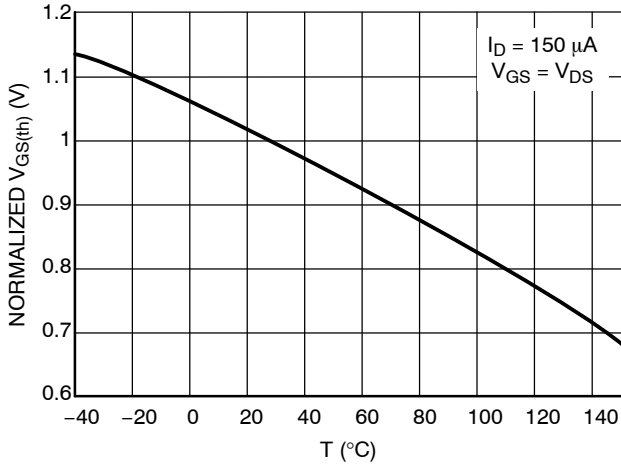


Figure 14. Normalized Threshold Voltage vs. Temperature

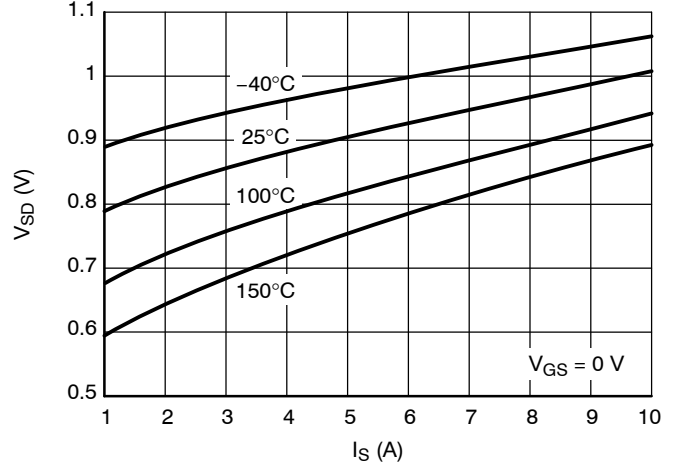


Figure 15. Source-Drain Diode Forward Characteristics

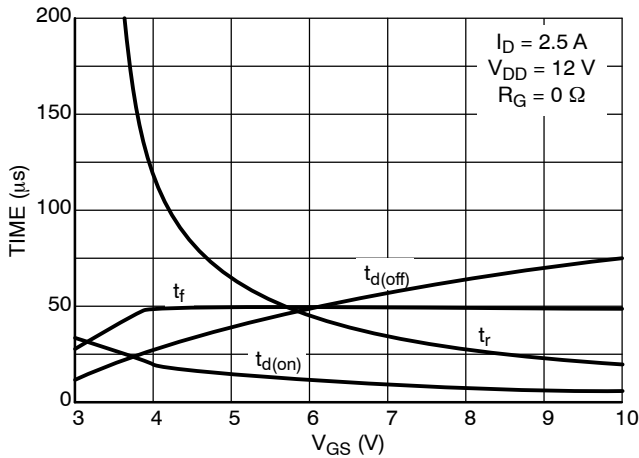


Figure 16. Resistive Load Switching Time vs. Gate-Source Voltage

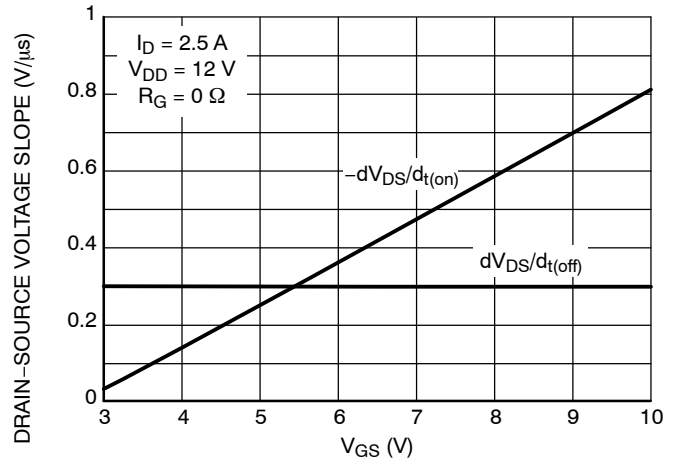


Figure 17. Resistive Load Switching Drain-Source Voltage Slope vs. Gate-Source Voltage

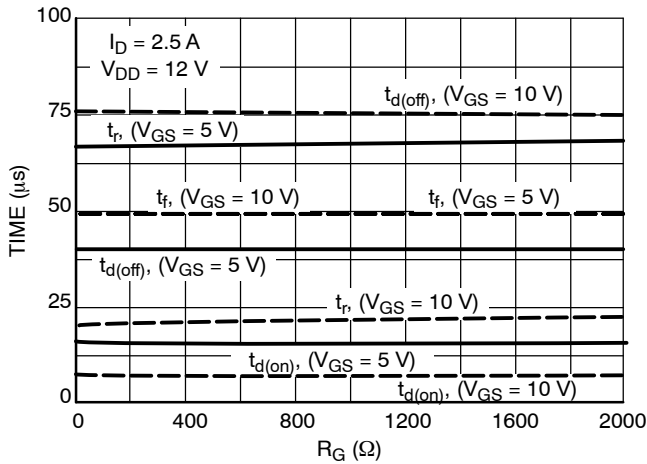


Figure 18. Resistive Load Switching Time vs. Gate Resistance

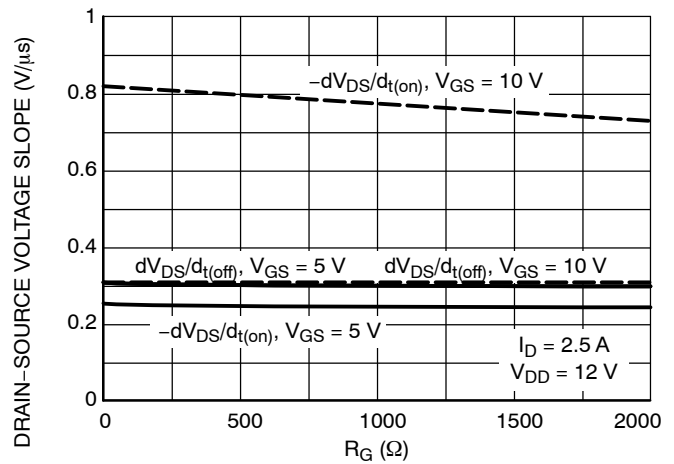


Figure 19. Drain-Source Voltage Slope during Turn On and Turn Off vs. Gate Resistance

NCV8402D

TYPICAL PERFORMANCE CURVES

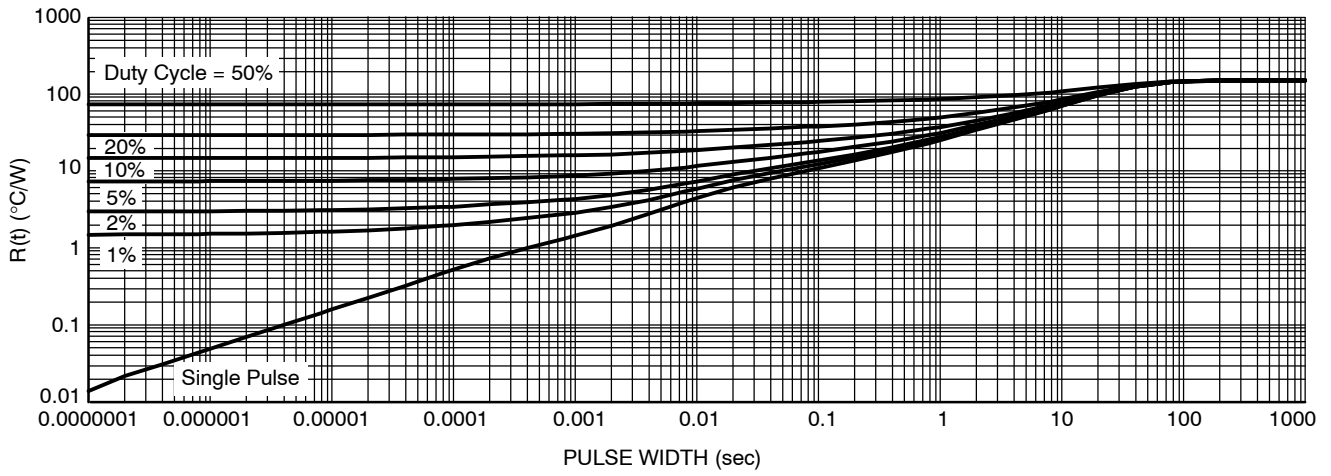


Figure 20. Transient Thermal Resistance

NCV8402D

TEST CIRCUITS AND WAVEFORMS

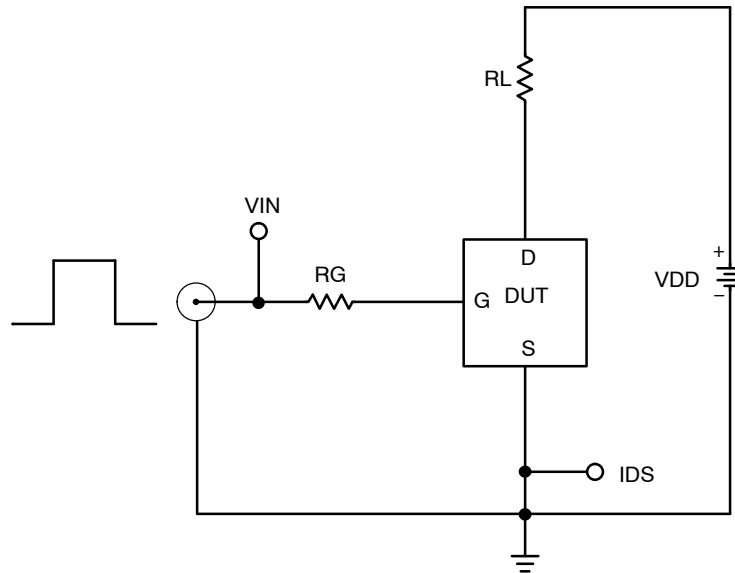


Figure 21. Resistive Load Switching Test Circuit

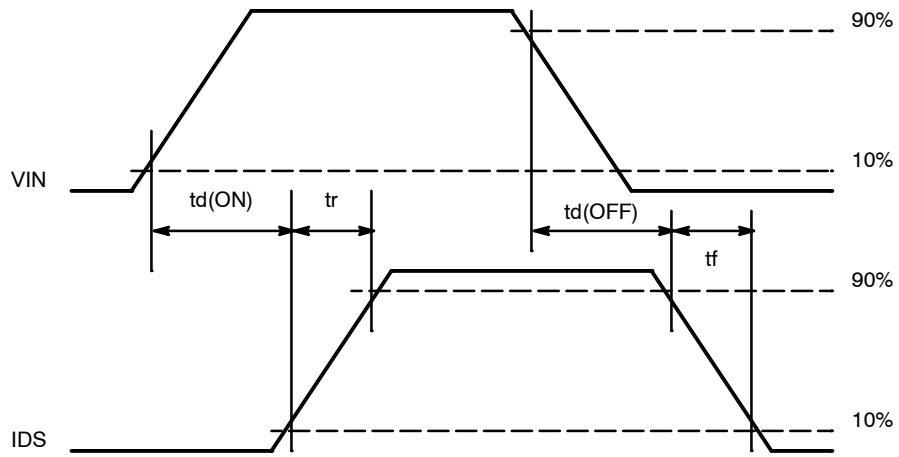


Figure 22. Resistive Load Switching Waveforms

NCV8402D

TEST CIRCUITS AND WAVEFORMS

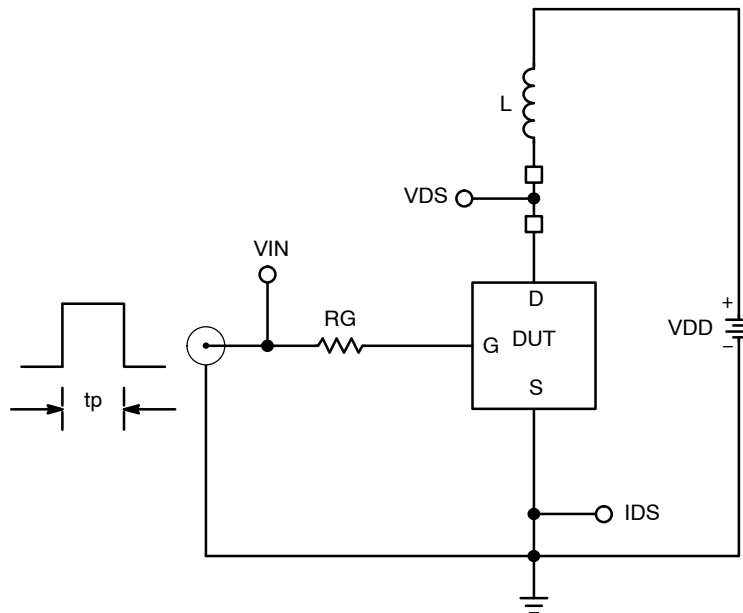


Figure 23. Inductive Load Switching Test Circuit

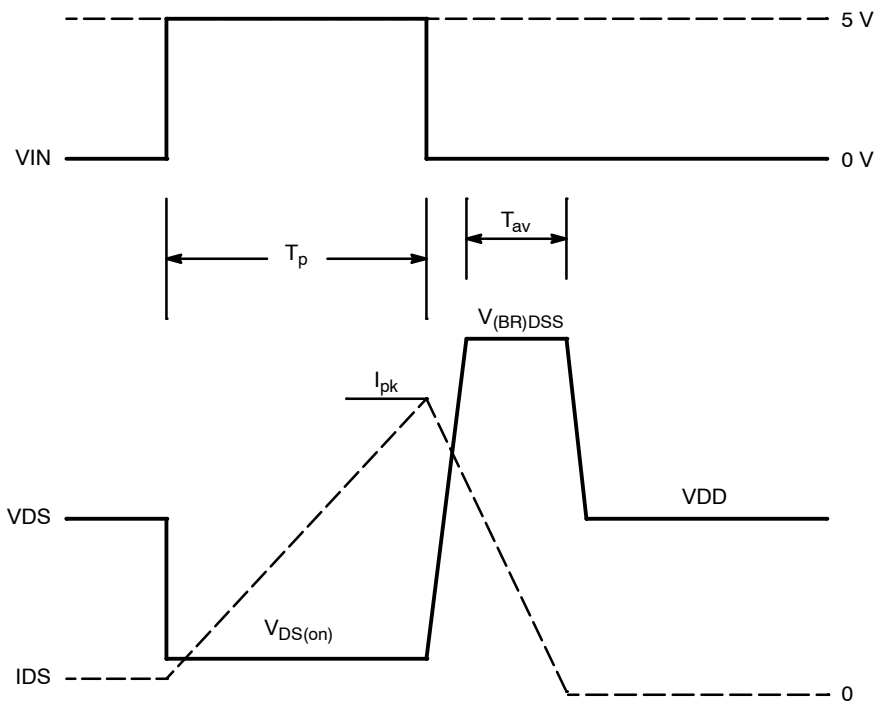
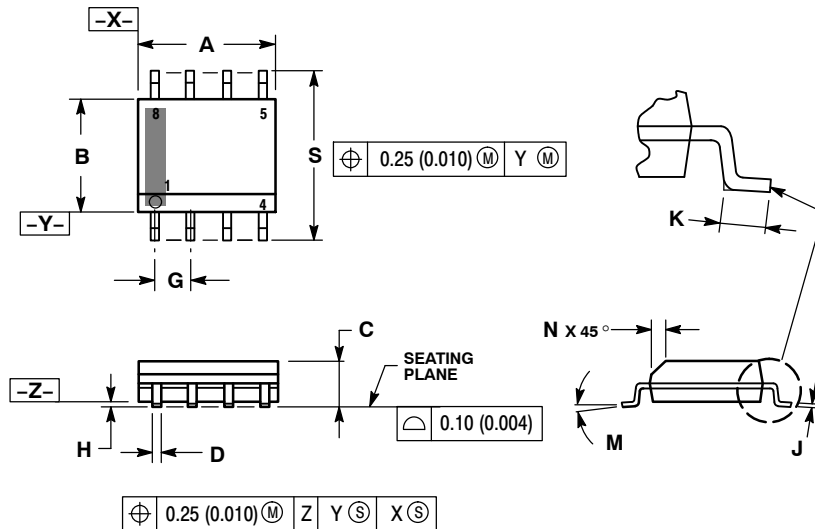


Figure 24. Inductive Load Switching Waveforms

NCV8402D

PACKAGE DIMENSIONS

SOIC-8
CASE 751-07
ISSUE AJ

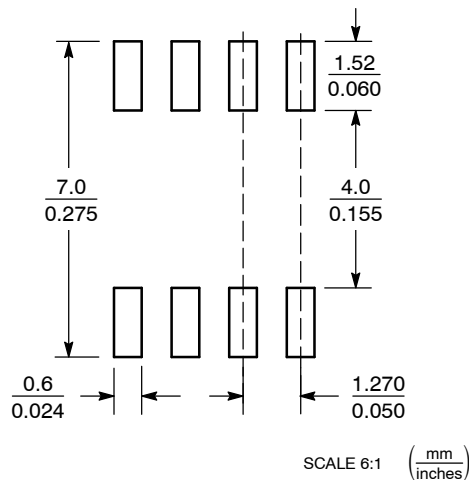


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



STYLE 11:

- PIN 1. SOURCE 1
- GATE 1
- SOURCE 2
- GATE 2
- DRAIN 2
- DRAIN 2
- DRAIN 1
- DRAIN 1

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative