

# HETERO JUNCTION FIELDEFFECT TRANSISTOR NE321000

### C to Ka BAND SUPER LOW NOISE AMPLIFIER N-CHANNEL HJ-FET CHIP

#### DESCRIPTION

The NE321000 is Hetero Junction FET that utilizes the hetero junction to create high mobility electrons. Its excellent low noise and associated gain make it suitable for DBS and another commercial systems, industrial and space applications.

#### FEATURES

- Super Low Noise Figure & High Associated Gain  
NF = 0.35 dB TYP.  $G_a = 13.5$  dB TYP. @  $f = 12$  GHz
- Gate Length:  $L_g \leq 0.20 \mu\text{m}$
- Gate Width :  $W_g = 160 \mu\text{m}$

#### ORDERING INFORMATION (PLAN)

Part Number	Quality Grade
NE321000	Standard (Grade D)

**Remark** To order evaluation samples, please contact your local NEC sales office. (Part number for sample order: NE321000)

#### ABSOLUTE MAXIMUM RATINGS ( $T_A = +25^\circ\text{C}$ )

Parameter	Symbol	Ratings	Unit
Drain to Source Voltage	$V_{DS}$	4.0	V
Gate to Source Voltage	$V_{GS}$	-3.0	V
Drain Current	$I_D$	$I_{DSS}$	mA
Gate Current	$I_G$	100	$\mu\text{A}$
Total Power Dissipation	$P_{tot}^{\text{Note}}$	200	mW
Channel Temperature	$T_{ch}$	175	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-65 to +175	$^\circ\text{C}$

**Note** Chip mounted on an Alumina heatsink (size:  $3 \times 3 \times 0.6$  t)

The information in this document is subject to change without notice. Before using this document, please confirm that this is the latest version.  
Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

**RECOMMENDED OPERATING CONDITIONS (T<sub>A</sub> = +25 °C)**

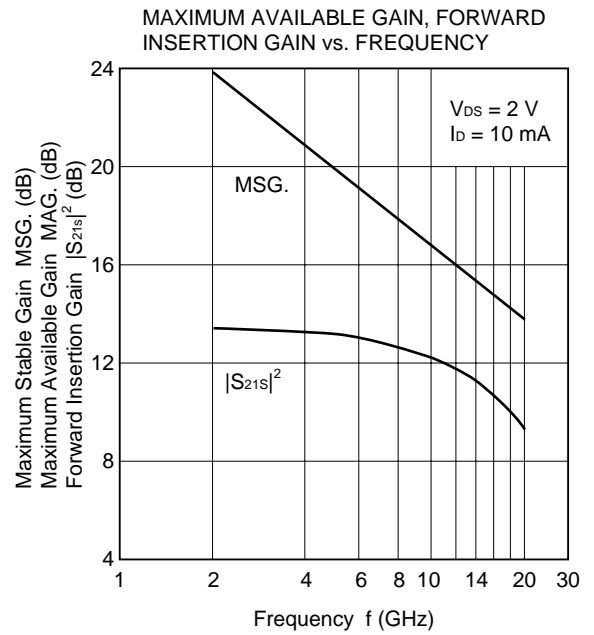
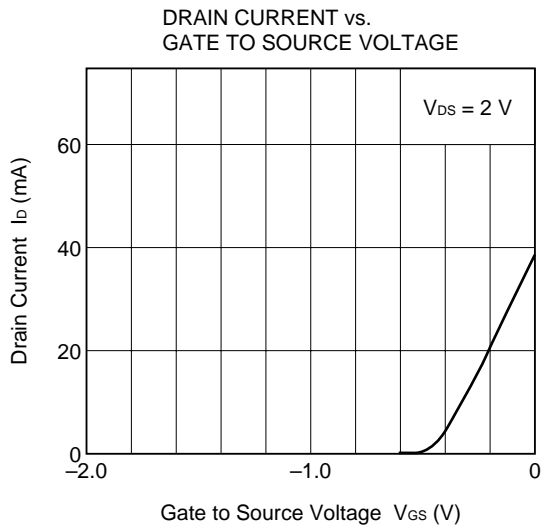
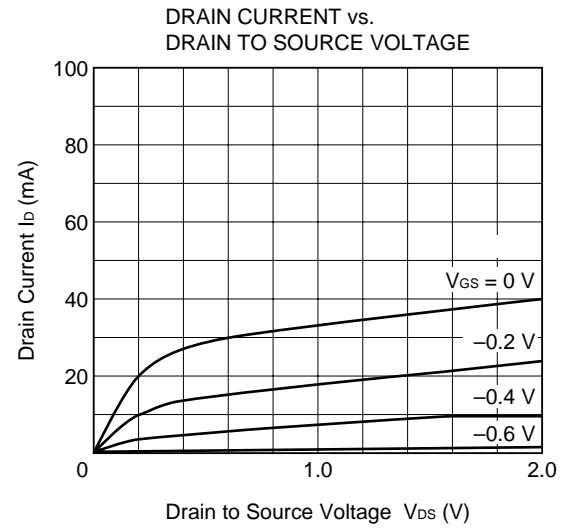
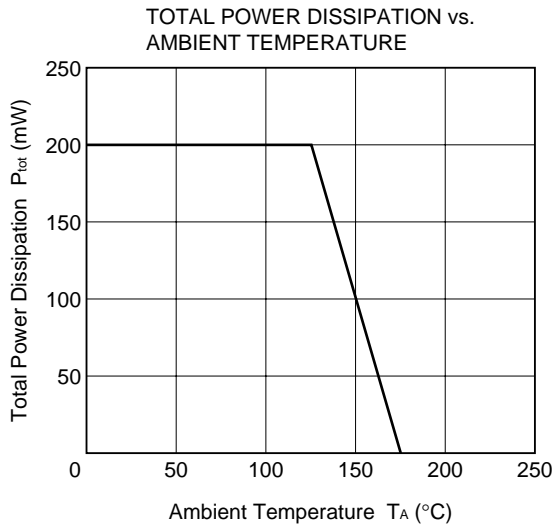
Parameter	Symbol	MIN.	TYP.	MAX.	Unit
★ Drain to Source Voltage	V <sub>DS</sub>	1	2	3	V
★ Drain Current	I <sub>D</sub>	5	10	15	mA
Input Power	P <sub>in</sub>	–	–	0	dBm

**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = +25 °C)**

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Gate to Source Leak Current	I <sub>GSO</sub>	V <sub>GS</sub> = –3 V	–	0.5	10	μA
Saturated Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 2 V, V <sub>GS</sub> = 0 V	15	40	70	mA
Gate to Source Cut Off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = 2 V, I <sub>DS</sub> = 100 μA	–0.2	–0.7	–2.0	V
Transconductance	g <sub>m</sub>	V <sub>DS</sub> = 2 V, I <sub>DS</sub> = 10 mA	40	55	–	mS
Noise Figure	NF	V <sub>DS</sub> = 2 V, I <sub>DS</sub> = 10 mA	–	0.35	0.45	dB
NF Associated Gain	G <sub>a</sub>	f = 12 GHz	12.0	13.5	–	dB

**Remark** RF performance is determined by packaging and testing 10 chips per wafer.  
 Wafer rejection criteria for standard devices is 2 rejects per 10 samples.

TYPICAL CHARACTERISTICS ( $T_A = +25\text{ }^\circ\text{C}$ )

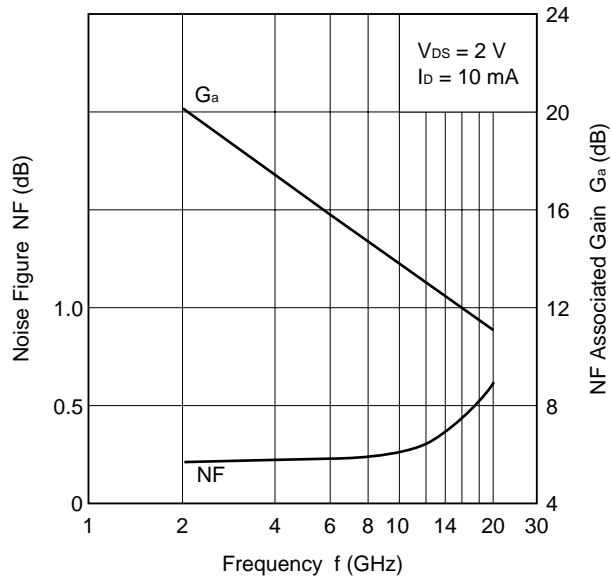


GAIN CALCULATIONS

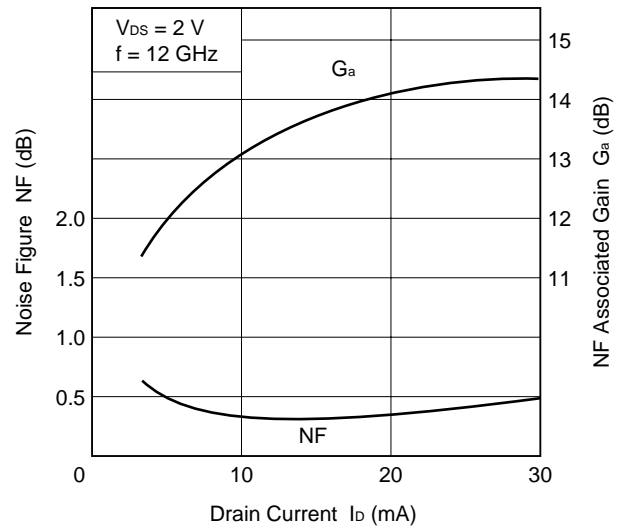
$$MSG. = \left| \frac{S_{21}}{S_{12}} \right| \quad K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2 |S_{12}| |S_{21}|}$$

$$MAG. = \left| \frac{S_{21}}{S_{12}} \right| (k \pm \sqrt{k^2 - 1}) \quad \Delta = S_{11} \cdot S_{22} - S_{21} \cdot S_{12}$$

NOISE FIGURE, NF ASSOCIATED GAIN vs. FREQUENCY



NOISE FIGURE, NF ASSOCIATED GAIN vs. DRAIN CURRENT



**S-PARAMETERS**

MAG. AND ANG.

$V_{DS} = 2\text{ V}$ ,  $I_D = 10\text{ mA}$

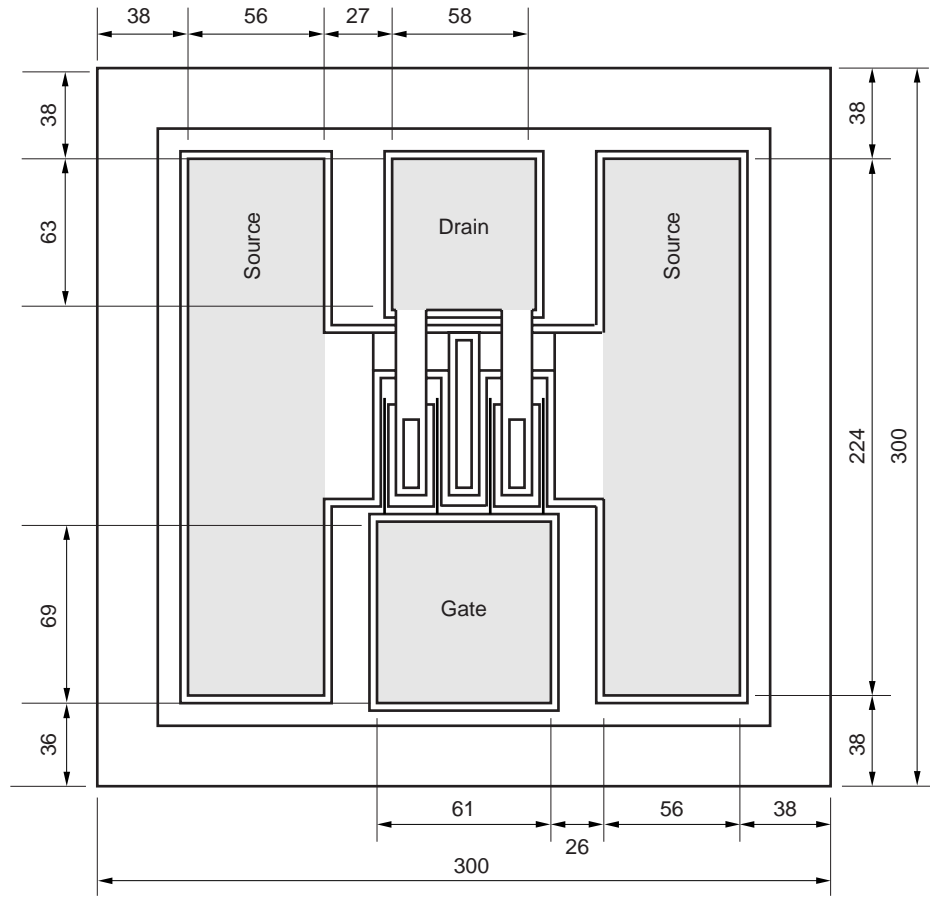
FREQUENCY GHz	S <sub>11</sub>		S <sub>21</sub>		S <sub>12</sub>		S <sub>22</sub>	
	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.	MAG.	ANG.
2.0	0.998	-13.2	4.72	170.2	0.020	81.3	0.602	-10.0
3.0	0.987	-19.3	4.70	165.6	0.030	77.3	0.599	-14.8
4.0	0.981	-25.7	4.62	160.5	0.040	73.2	0.593	-19.9
5.0	0.970	-32.7	4.50	155.7	0.050	69.4	0.588	-25.6
6.0	0.962	-38.6	4.45	151.6	0.059	65.3	0.583	-30.1
7.0	0.952	-44.4	4.37	147.4	0.067	62.2	0.574	-34.4
8.0	0.941	-50.1	4.28	143.5	0.074	58.6	0.567	-39.1
9.0	0.927	-55.6	4.17	139.7	0.081	55.2	0.564	-43.1
10.0	0.912	-61.5	4.03	135.6	0.087	51.5	0.552	-47.2
11.0	0.898	-66.9	3.90	131.5	0.094	48.0	0.541	-52.0
12.0	0.882	-71.6	3.79	128.0	0.100	44.9	0.536	-55.5
13.0	0.868	-75.9	3.66	124.9	0.104	42.0	0.526	-58.6
14.0	0.855	-80.2	3.54	121.9	0.108	39.0	0.518	-62.1
15.0	0.843	-84.2	3.42	119.0	0.111	36.2	0.509	-65.0
16.0	0.827	-88.5	3.30	115.8	0.115	33.5	0.501	-68.3
17.0	0.807	-92.6	3.16	112.9	0.116	30.5	0.494	-71.2
18.0	0.796	-95.3	3.05	110.8	0.117	28.5	0.488	-73.2
19.0	0.793	-98.0	2.97	108.7	0.120	27.9	0.489	-75.2
20.0	0.788	-101.2	2.89	106.2	0.123	26.5	0.487	-77.4
21.0	0.782	-103.8	2.79	104.1	0.125	24.9	0.484	-80.9
22.0	0.783	-106.4	2.70	101.9	0.128	23.3	0.486	-82.7
23.0	0.785	-109.9	2.62	99.5	0.132	20.7	0.477	-84.1
24.0	0.778	-113.4	2.53	97.4	0.135	18.8	0.474	-87.9
25.0	0.766	-116.0	2.46	95.8	0.135	16.8	0.481	-88.3
26.0	0.757	-118.1	2.40	93.8	0.135	15.3	0.469	-89.2
27.0	0.753	-119.9	2.33	92.5	0.133	14.3	0.463	-91.6
28.0	0.755	-121.6	2.29	90.6	0.136	14.0	0.484	-93.5
29.0	0.748	-124.2	2.23	88.4	0.135	12.6	0.481	-95.2
30.0	0.743	-126.2	2.16	86.8	0.136	11.3	0.475	-97.5

**NOISE PARAMETERS**

$V_{DS} = 2\text{ V}$ ,  $I_D = 10\text{ mA}$

Freq. (GHz)	NF <sub>min.</sub> (dB)	G <sub>a</sub> (dB)	Γ <sub>opt</sub>		Rn/50
			MAG.	ANG. (deg.)	
2.0	0.21	19.5	0.94	3.7	0.31
4.0	0.22	17.6	0.87	8.2	0.31
6.0	0.24	15.9	0.82	13.3	0.32
8.0	0.26	14.6	0.77	18.8	0.32
10.0	0.28	13.5	0.73	24.8	0.32
12.0	0.31	12.7	0.69	31.4	0.31
14.0	0.38	12.1	0.67	38.4	0.31
16.0	0.45	11.6	0.64	45.9	0.30
18.0	0.52	11.3	0.63	53.9	0.29
20.0	0.59	11.2	0.62	62.4	0.28
22.0	0.66	11.1	0.61	71.4	0.27
24.0	0.72	11.2	0.62	80.8	0.25
26.0	0.79	11.2	0.63	90.8	0.23

CHIP DIMENSIONS (Unit:  $\mu\text{m}$ )



Thickness = 140  $\mu\text{m}$   
[Shaded Box] : BONDING AREA

## CHIP HANDLING

### DIE ATTACHMENT

Die attach operation can be accomplished with Au-Sn (within a 300 °C – 10 s) performs in a forming gas environment.

Epoxy die attach is not recommend.

### BONDING

Bonding wires should be minimum length, semi hard gold wire (3 to 8 % elongation) 20 microns in diameter.

Bonding should be performed with a wedge tip that has a taper of approximately 15 %. Bonding time should be kept to minimum.

As a general rule, the bonding operation should be kept within a 280 °C, 2 minutes for all bonding wires.

If longer periods are required, the temperature should be lowered.

### PRECAUTION

The user must operate in a clean, dry environment. The chip channel is glassivated for mechanical protection only and does not preclude the necessity of a clean environment.

The bonding equipment should be periodically checked for sources of surge voltage and should be properly grounded at all times. In fact, all test and handling equipment should be grounded to minimize the possibilities of static discharge.

Avoid high static voltage and electric fields, because this device is Hetero Junction field effect transistor with shottky barrier gate.



[MEMO]

[MEMO]

[MEMO]

## CAUTION

**The Great Care must be taken in dealing with the devices in this guide.**

**The reason is that the material of the devices is GaAs (Gallium Arsenide), which is designated as harmful substance according to the law concerned.**

**Keep the law concerned and so on, especially in case of removal.**

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