150MHz phase-locked loop NE/SA568A

DESCRIPTION

The NE568A is a monolithic phase-locked loop (PLL) which operates from 1Hz to frequencies in excess of 150MHz and features an extended supply voltage range and a lower temperature coefficient of the V_{CO} center frequency in comparison with its predecessor, the NE 568. The NE568A is function and pin-compatible with the NE568, requiring only minor changes in peripheral circuitry (see Figure 3). Temperature compensation network is different, no resistor on Pin 12, needs to be grounded and Pin 13 has a 3.9kΩ resistor to ground. Timing cap, C_2, is different and for 70MHz operation with temperature compensation network should be 16pF, not 34pF as was used in the NE568. The NE568A has the following improvements: ESD protected; extended V_{CC} range from 4.5V to 5.5V; operating temperature range -55 to 125°C (see Signetics Military 568A data sheet); less layout sensitivity; and lower T_C of VCO (center frequency). The integrated circuit consists of a limiting amplifier, a current-controlled oscillator (ICO), a phase detector, a level shift circuit, V/I and I/V converters, an output buffer, and bias circuitry with temperature and frequency compensating characteristics. The design of the NE568A is particularly well-suited for demodulation of FM signals with extremely large deviation in systems which require a highly linear output. In satellite receiver applications with a 70MHz IF, the NE568A will demodulate ±20% deviations with less than 1.0% typical non-linearity. In addition to high linearity, the circuit has a loop filter which can be configured with series or shunt elements to optimize loop dynamic performance. The NE568A is available in 20-pin dual in-line and 20-pin SO (surface mounted) plastic packages.

FEATURES

- Operation to 150MHz
- High linearity buffered output

PIN CONFIGURATION

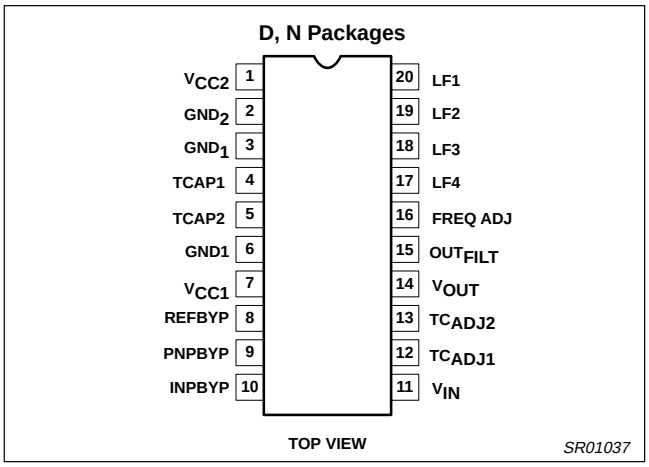


Figure 1. Pin Configuration

- Series or shunt loop filter component capability
- External loop gain control
- Temperature compensated
- ESD protected[1]

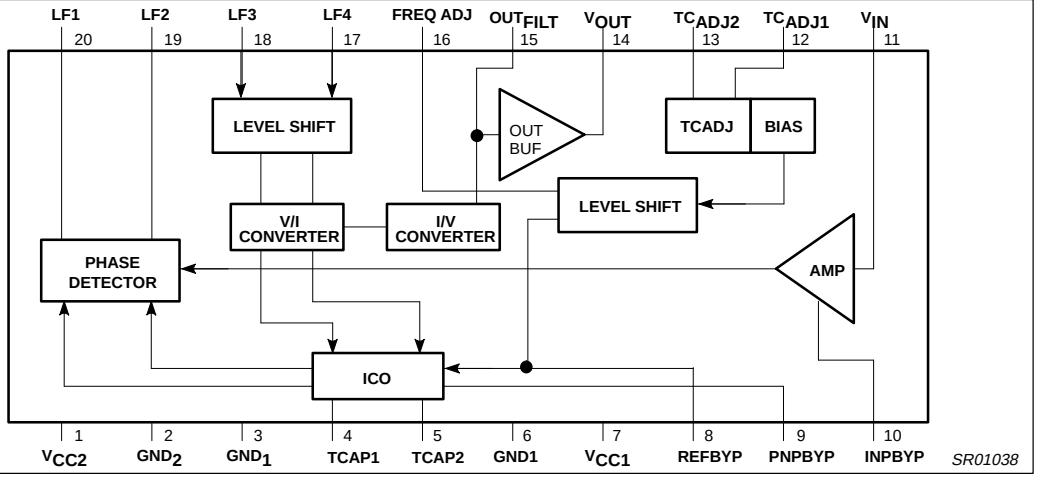
APPLICATIONS

- Satellite receivers
- Fiber optic video links
- VHF FSK demodulators
- Clock Recovery

ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
20-Pin Plastic Small Outline Large (SOL) Package	0 to +70°C	NE568AD	SOT163-1
20-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE568AN	SOT146-1
20-Pin Plastic Small Outline Large (SOL) Package	-40 to +85°C	SA568AD	SOT163-1
20-Pin Plastic Dual In-Line Package (DIP)	-40 to +85°C	SA568AN	SOT146-1

BLOCK DIAGRAM



NOTE:
Pins 4 and 5 can tolerate 1000V only, and all other pins, greater than 2000V for ESD (human body model).

Figure 2. Block Diagram

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Supply voltage	6	V
T_J	Junction temperature	+150	°C
T_{STG}	Storage temperature range	-65 to +150	°C
P_{DMAX}	Maximum power dissipation	400	mW
θ_{JA}	Thermal resistance	80	°C/W

ELECTRICAL CHARACTERISTICS

The elctrical characteristics listed below are actual tests (unless otherwise stated) performed on each device with an automatic IC tester prior to shipment. Performance of the device in automated test set-up is not necessarily optimum. The NE568A is layout-sensitive. Evaluation of performance for correlation to the data sheet should be done with the circuit and layout of Figures 3, 4, and 5 with the evaluation unit soldered in place. (Do not use a socket!)

DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5V; T_A = 25°C; f_O = 70MHz, Test Circuit Figure 3, f_{IN} = -20dBm, R_4 = 3.9kΩ, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA568A			
			MIN	TYP	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	V
I_{CC}	Supply current			54	70	mA

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			NE/SA568A			
			MIN	TYP	MAX	
f_{OSC}	Maximum oscillator operating frequency[3]		150			MHz
	Input signal level		50 –20[1]		2000 +10	mV_{P-P} dBm
BW	Demodulated bandwidth			$f_O/7$		MHz
	Non-linearity[5]	Dev = ±20%, Input = -20dBm		1.0	4.0	%
	Lock range[2]	Input = -20dBm	±25	±35		% of f_O
	Capture range[2]	Input = -20dBm	±20	±30		% of f_O
	TC of f_O	Figure 3		100		ppm/°C
R_{IN}	Input resistance[4]		1			kΩ
	Output impedance			6		Ω
	Demodulated V_{OUT}	Dev = ±20% of f_O measured at Pin 14	0.40	0.52		V_{P-P}
	AM rejection	V_{IN} = -20dBm (30% AM) referred to ±20% deviation		50		dB
f_O	Distribution[6]	Centered at 70MHz, R_2 = 1.2kΩ, C_2 = 16pF, R_4 = 3.9kΩ (C_2 + C_{STRAY} = 20pF)	-15	0	+15	%
f_O	Drift with supply	4.5V to 5.5V		2		%/V

NOTE:

1. Signal level to assure all published parameters. Device will continue to function at lower levels with varying performance.
2. Limits are set symmetrical to f_O. Actual characteristics may have asymmetry beyond the specified limits.
3. Not 100% tested, but guaranteed by design.
4. Input impedance depends on package and layout capacitances. See Figures 6 and 5.
5. Linearity is tested with incremental changes in inupt frequency and measurement of the DC output voltage at Pin 14 (V_{OUT}). Non-linearity is then calculated from a straight line over the deviation range specified.
6. Free-running frequency is measured as feedthrough to Pin 14 (V_{OUT}) with no input signal applied.

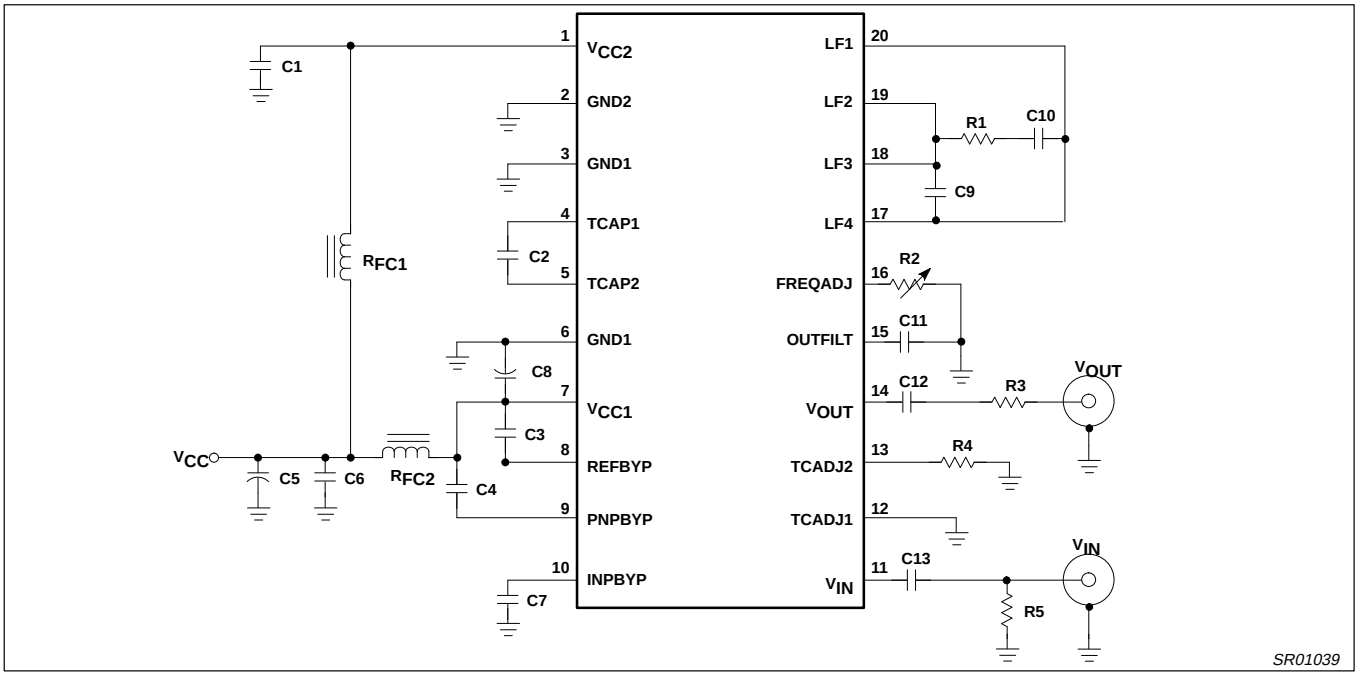


Figure 3. Test Circuit for AC Parameters

FUNCTIONAL DESCRIPTION

The NE568A is a high-performance phase-locked loop (PLL). The circuit consists of conventional PLL elements, with special circuitry for linearized demodulated output, and high-frequency performance. The process used has NPN transistors with f_T > 6GHz. The high gain and bandwidth of these transistors make careful attention to layout and bypass critical for optimum performance. The performance of the PLL cannot be evaluated independent of the layout. The use of the application layout in this data sheet and surface-mount capacitors are highly recommended as a starting point.

The input to the PLL is through a limiting amplifier with a gain of 200. The input of this amplifier is differential (Pins 10 and 11). For single-ended applications, the input must be coupled through a DC-blocking capacitor with low impedance at the frequency of interest. The single-ended input is normally applied to Pin 11 with Pin 10 AC-bypassed with a low-impedance capacitor. The input impedance is characteristically slightly above 500Ω. Impedance match is not necessary, but loading the signal source should be avoided. When the source is 50 or 75Ω, a DC-blocking capacitor is usually all that is needed.

Input amplification is low enough to assure reasonable response time in the case of large signals, but high enough for good AM rejection. After amplification, the input signal drives one port of a multiplier-cell phase detector. The other port is driven by the current-controlled oscillator (ICO). The output of the phase comparator is a voltage proportional to the phase difference of the input and ICO signals. The error signal is filtered with a low-pass filter to provide a DC-correction voltage, and this voltage is converted to a current which is applied to the ICO, shifting the frequency in the direction which causes the input and ICO to have a 90° phase relationship.

The oscillator is a current-controlled multivibrator. The current control affects the charge/discharge rate of the timing capacitor. It is common for this type of oscillator to be referred to as a voltage-controlled oscillator (VCO), because the output of the phase comparator and the loop filter is a voltage. To control the frequency of an integrated ICO multivibrator, the control signal must be conditioned by a voltage-to-current converter. In the NE568A, special circuitry predistorts the control signal to make the change in frequency a linear function over a large control-current range.

The free-running frequency of the oscillator depends on the value of the timing capacitor connected between Pins 4 and 5. The value of the timing capacitor depends on internal resistive components and current sources. When R_2 = 1.2kΩ and R_4 = 0Ω, a very close approximation of the correct capacitor value is:

$$C^* = \frac{0.0014}{f_O} \text{ F}$$

where

$$C^* = C_2 + C_{STRAY}$$

The temperature-compensation resistor, R_4, affects the actual value of capacitance. This equation is normalized to 70MHz. See 10 for correction factors.

The loop filter determines the dynamic characteristics of the loop. In most PLLs, the phase detector outputs are internally connected to the ICO inputs. The NE568A was designed with filter output to input connections from Pins 20 (ϕ DET) to 17 (ICO), and Pins 19 (ϕ DET) to 18 (ICO) external. This allows the use of both series and shunt loop-filter elements. The loop constratints are:

K_O = 0.12V/Radian (Phase Detector Constant)

$$K_O = 4.2 \cdot 10^9 \frac{\text{Radians}}{V_{-sec}} \text{ (ICO Constant) at 70MHz}$$

The loop filter determines the general characteristics of the loop. Capacitors C_9, C_{10}, and resistor R_1, control the transient output of the phase detector. Capacitor C_9 suppresses 70MHz feedthrough by interaction with 100Ω load resistors internal to the phase detector.

$$C_9 = \frac{1}{2\pi\ (50)\ (f_O)}\ F$$

At 70MHz, the calculated value is 45pF. Empirical results with the test and application board were improved when a 47pF capacitor was used.

The natural frequency for the loop filter is set by C_{10} and R_1. If the center frequency of the loop is 70MHz and the full demodulated bandwidth is desired, i.e., $f_{BW} = f_O/7 = 10MHz$, and a value for R_1 is chosen, the value of C_{10} can be calculated.

$$C_{10} = \frac{1}{2\pi\ R_1\ f_{BW}}\ F$$

Also,

$$C_{11} = \frac{1}{2\pi 350\Omega f_{BW(Hz)}}$$

This capacitance determines the signal bandwidth of the output buffer amplifier. (For further inofrmation see Philips application note AN1881 “The NE568A Phase Locked Loop as a Wideband Video Demodulator”.

Parts List and Layout 40MHz Application NE568AD

C_1	100nF	±10%	Ceramic chip	1206
C_2[1]	18pF	±2%	Ceramic chip	0805
C_2[2]	16pF	±2%	Ceramic ORChip	
C_3	100nF	±10%	Ceramic chip	1206
C_4	100nF	±10%	Ceramic chip	1206
C_5	6.8µF	±10%	Tantalum	35V
C_6	100nF	±10%	Ceramic chip	1206
C_7	100nF	±10%	Ceramic chip	1206
C_8	100nF	±10%	Ceramic chip	1206
C_9	47pF	±2%	Ceramic chip	0805 or 1206
C_{10}	560pF	±2%	Ceramic chip	0805 or 1206
C_{11}	47pF	±2%	Ceramic chip	0805 or 1206
C_{12}	100nF	±10%	Ceramic chip	1206
C_{13}	100nF	±10%	Ceramic chip	1206
R_1	27Ω	±10%	Chip CR32	1/4W
R_2	1.2kΩ		Trim pot	
R_3[3]	43Ω	±10%	Chip CR32	1/4W
R_4[4]	3.9kΩ	±10%	Chip CR32	1/4W
R_5[3]	50Ω	±10%	Chip CR32	1/4W
RFC_1[5]	10µH	±10%	Surface mount	
RFC_2[5]	10µH	±10%	Surface mount	

NOTES:
1. 18pF with Pin 12 ground and Pin 13 no connect (open).
2. $C_2 + C_{STRAY} = 16pF$ for temperature-compensated configuration with $R_4 = 3.9k\Omega$.
3. For 50Ω setup. $R_1 = 62\Omega$, $R_3 = 75\Omega$ for 75Ω application.
4. For test configuration $R_4 = 0\Omega$ (GND) and $C_2 = 18pF$.
5. 0Ω chip resistors (jumpers) may be substituted with minor degradation of performance.

Parts List and Layout 70MHz Application NE568AN

C_1	100nF	±10%	Ceramic chip	50V
C_2[1]	18pF	±2%	Ceramic chip	50V
C_2[2]	16pF	±2%	Ceramic chip	0805
C_3	100nF	±10%	Ceramic chip	50V
C_4	100nF	±10%	Ceramic chip	50V
C_5	6.8µF	±10%	Tantalum	35V
C_6	100nF	±10%	Ceramic chip	50V
C_7	100nF	±10%	Ceramic chip	50V
C_8	100nF	±10%	Ceramic chip	50V
C_9	47pF	±2%	Ceramic chip	50V
C_{10}	560pF	±2%	Ceramic chip	50V
C_{11}	47pF	±2%	Ceramic chip	50V
C_{12}	100nF	±10%	Ceramic chip	50V
C_{13}	100nF	±10%	Ceramic chip	50V
R_1	27Ω	±10%	Ceramic chip CR32	1/4W
R_2	1.2kΩ		Trim pot	
R_3[3]	43Ω	±10%	Ceramic chip CR32	1/4W
R_4[4]	3.9kΩ	±10%	Ceramic chip CR32	1/4W
R_5[3]	50Ω	±10%	Ceramic chip CR32	1/4W
RFC_1	10µH	±10%	Surface mount	
RFC_2	10µH	±10%	Surface mount	

NOTES:
1. 18pF with Pin 12 ground and Pin 13 no connect (open).
2. $C_2 + C_{STRAY} = 16pF$ for temperature-compensated configuration with $R_4 = 3.9k\Omega$.
3. For 50Ω setup. $R_1 = 62\Omega$, $R_3 = 75\Omega$ for 75Ω application.
4. For test configuration $R_4 = 0\Omega$ (GND) and $C_2 = 18pF$.

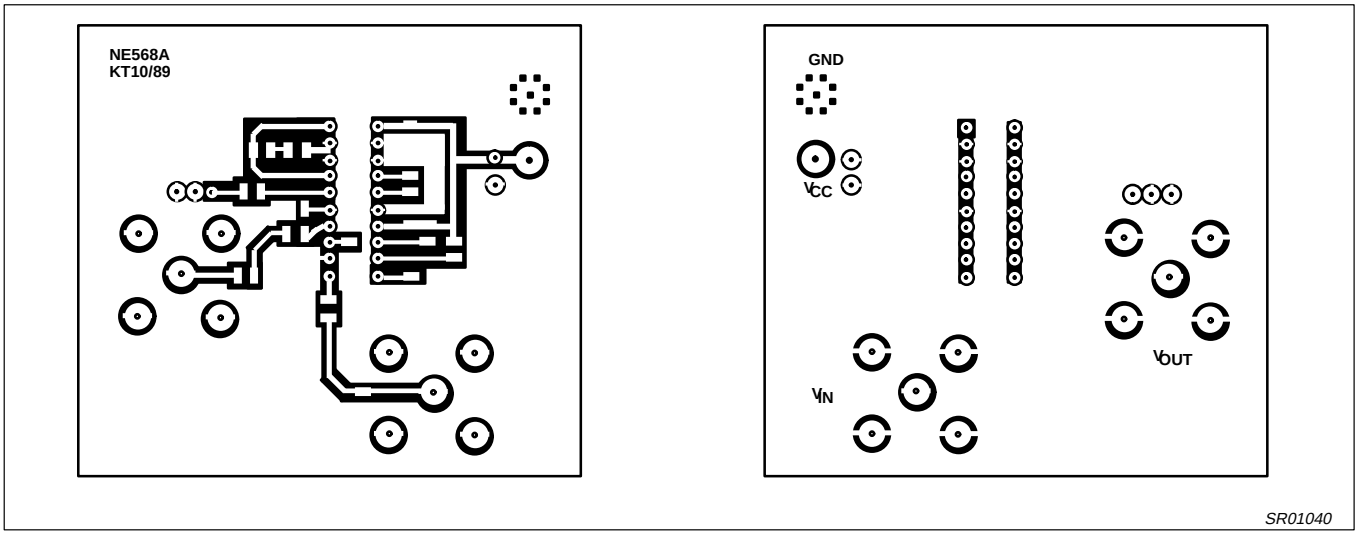


Figure 4. N Package Layout (Not Actual Size)

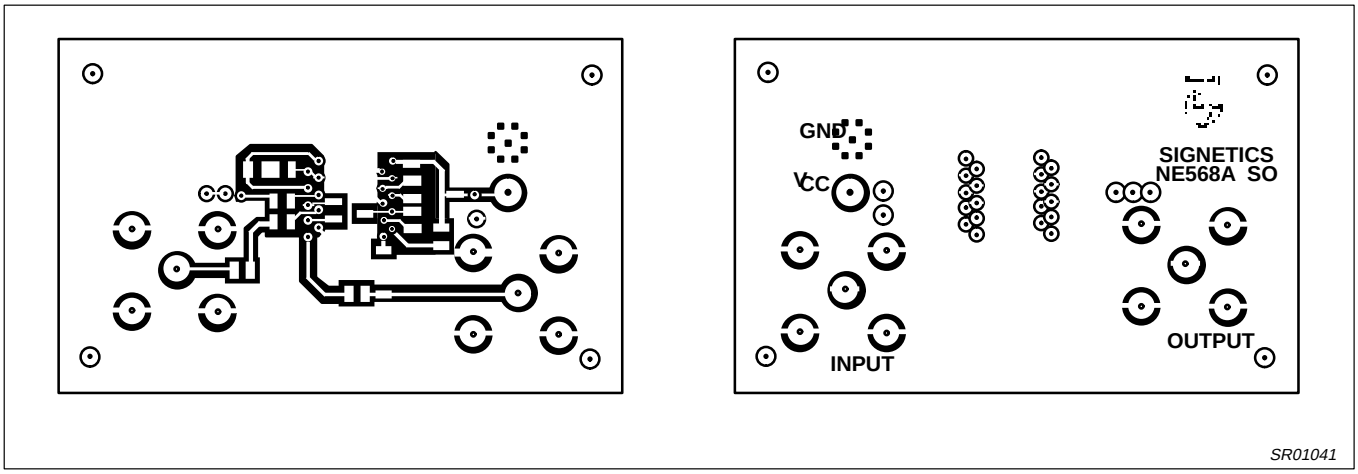


Figure 5. D Package Layout (Not Actual Size)

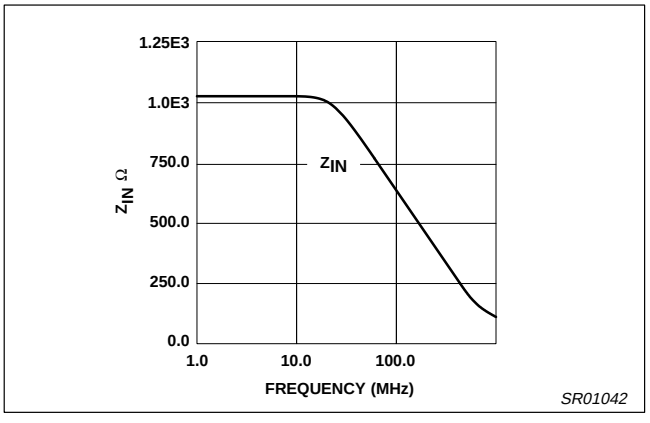


Figure 6. NE568A Input Impedance With CP = 0.5pF 20-Pin SO Package

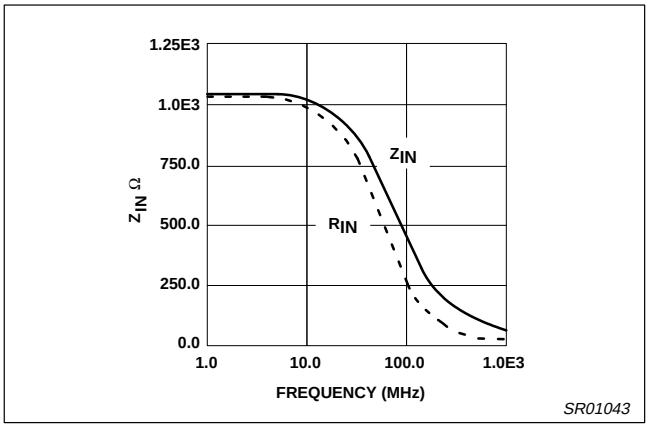


Figure 7. NE568A Input Impedance WithCP = 1.49pF 20-Pin Dual In-Line Plastic Package

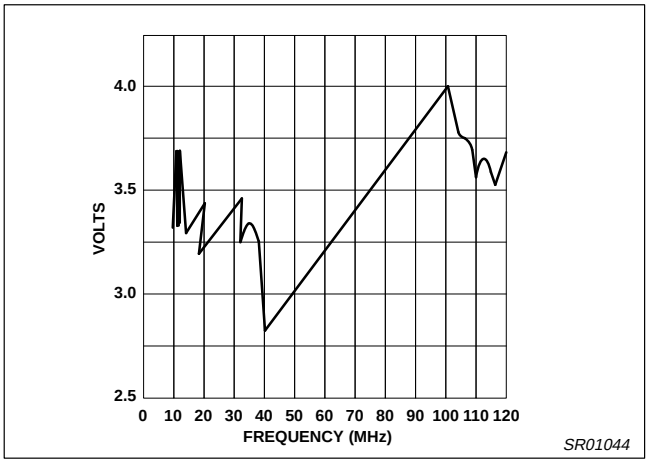


Figure 8. Typical Output Linearity

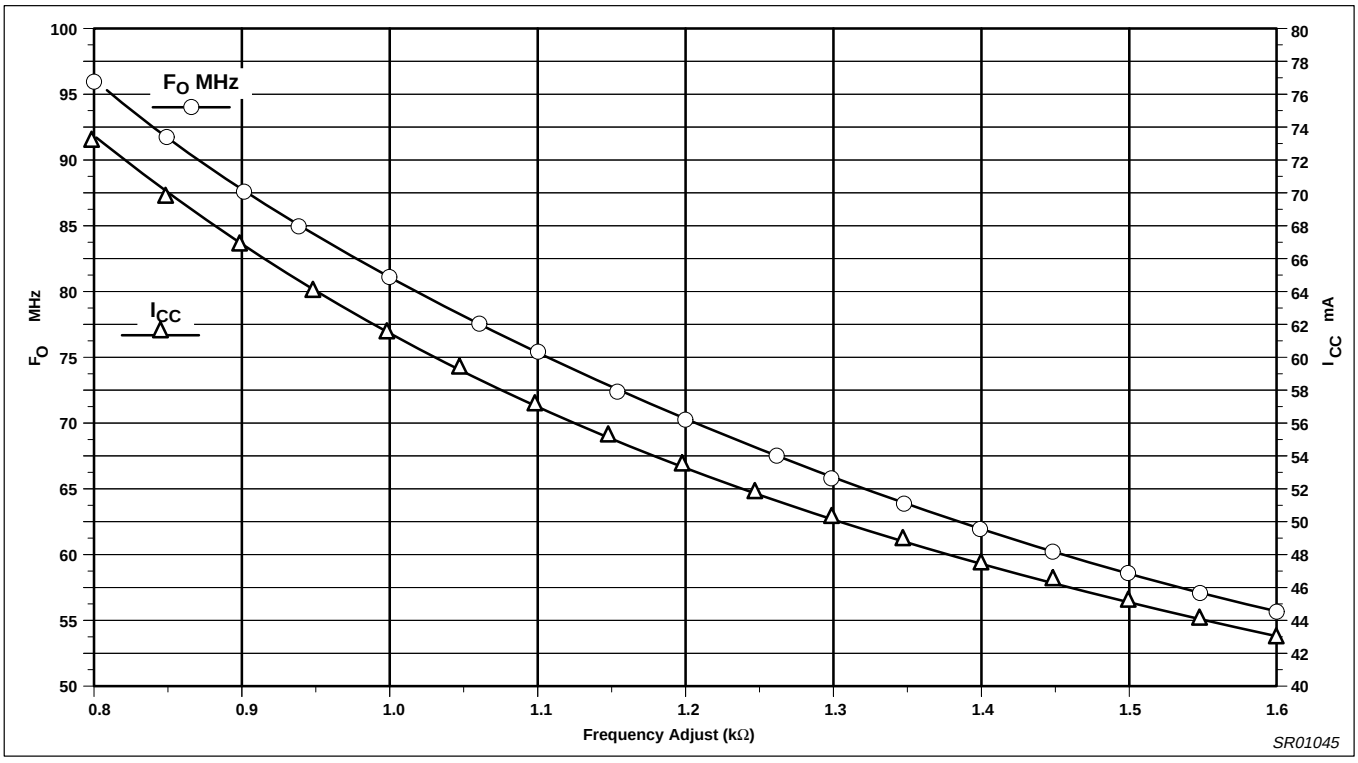


Figure 9. NE568: Frequency Adjust vs F_O and I_{CC}

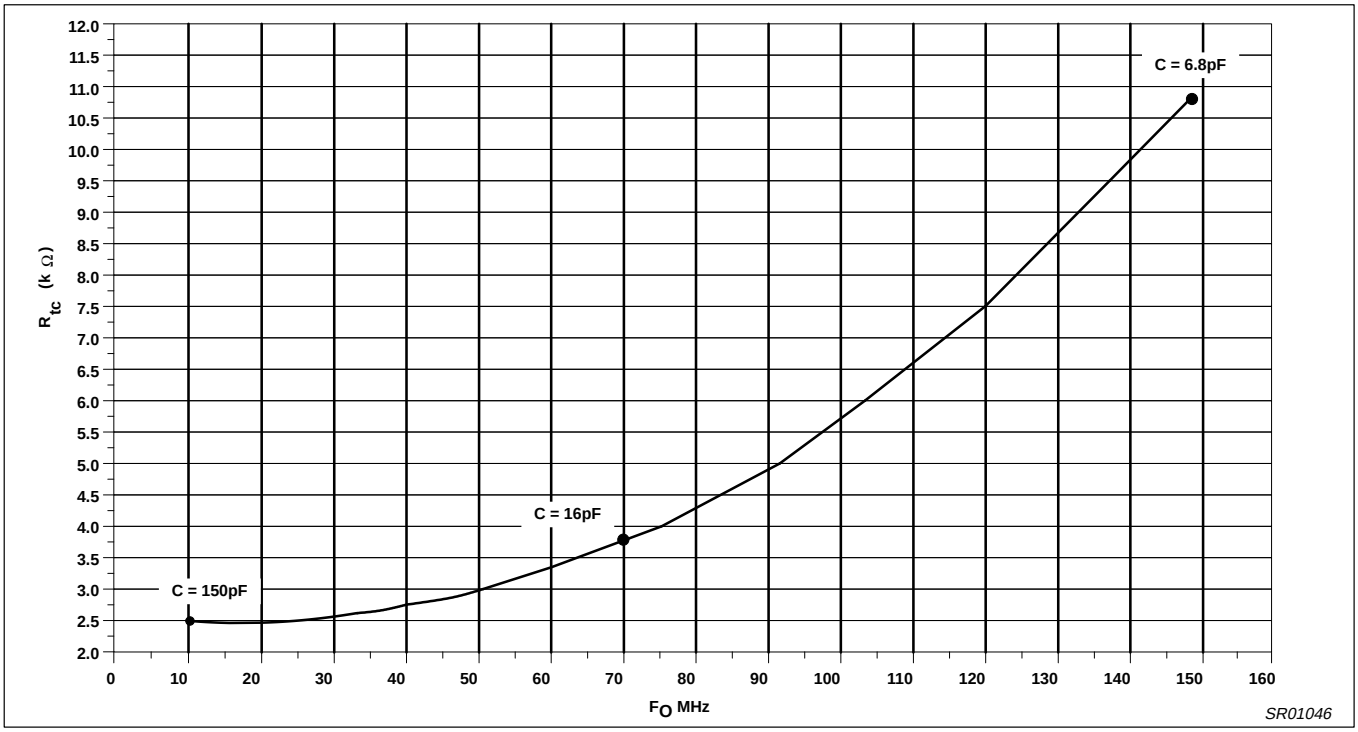


Figure 10. NE568A: R_{tc} (Pin 13) vs F_O; Choosing the Optimum Temperature Compensation Resistor

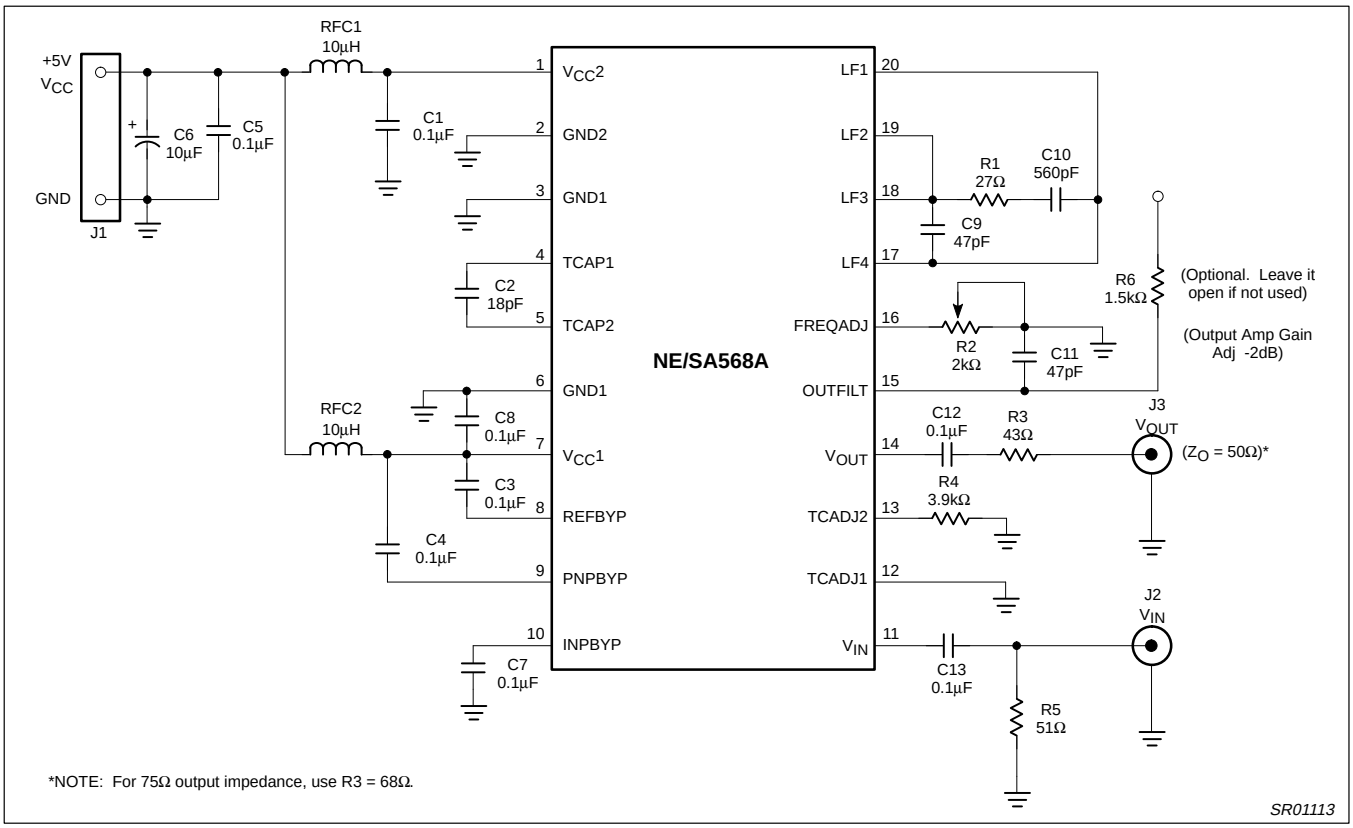
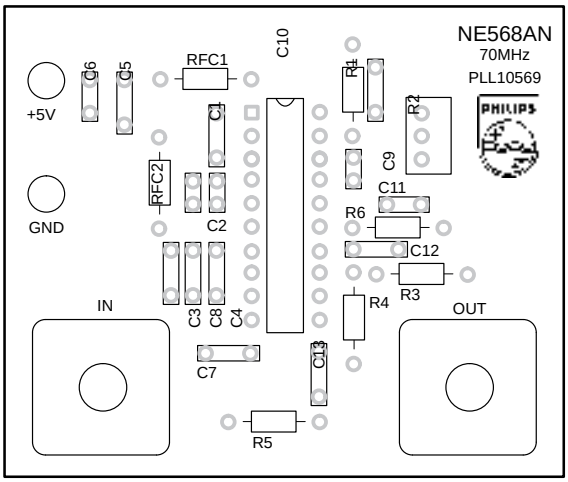
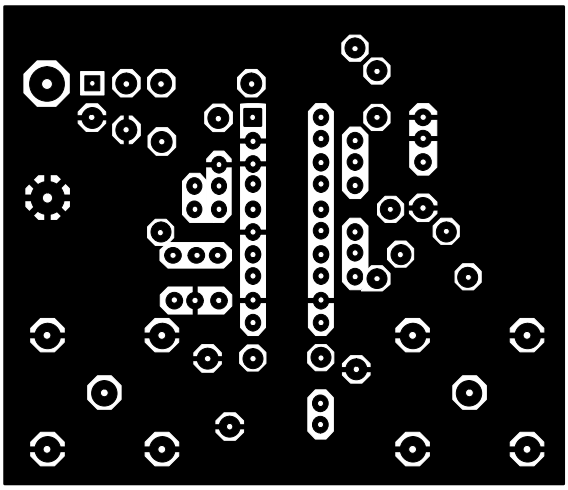


Figure 11. Phase Locked Loop NE/SA568A

COMPONENTS LAYOUT



TOP



BOTTOM

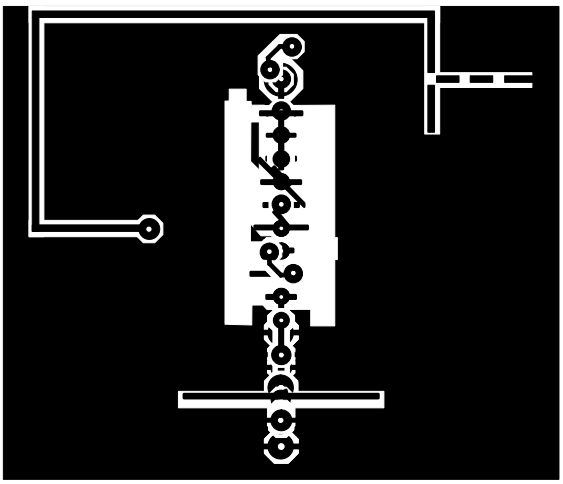


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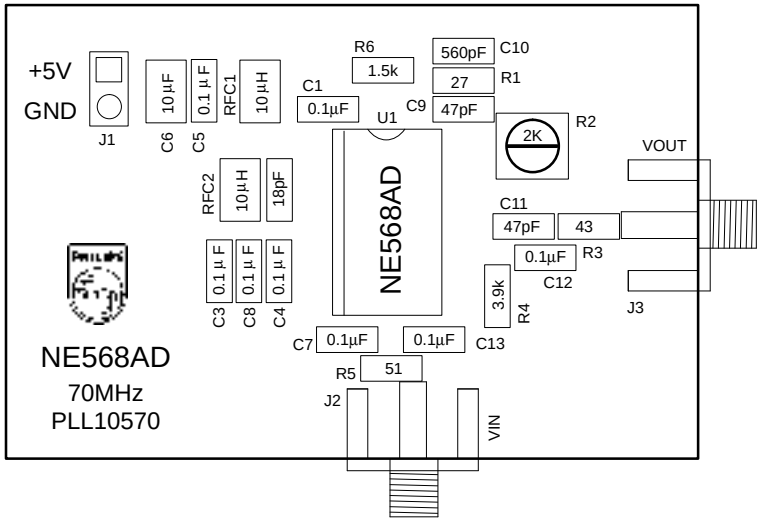
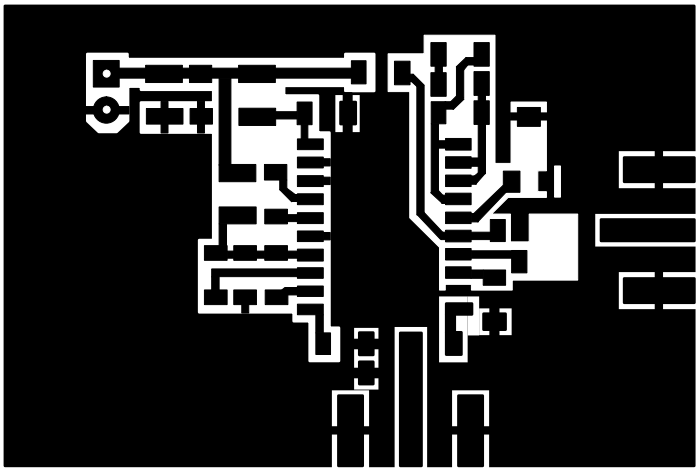
Figure 12. NE568AN Board Layout (Not Actual Size)





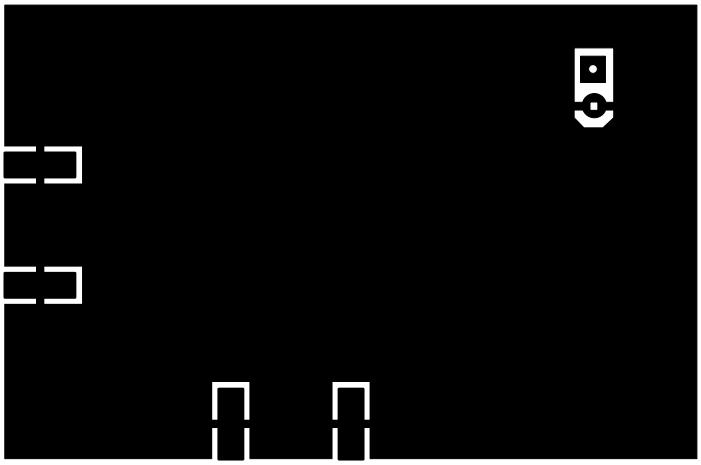


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Figure 13. NE568AD Board Layout (Not Actual Size)