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GEC PLESSEY
SEMICONDUCTORS

DS3281-1.1

NJ88C30

VHF SYNTHESISER

The NJ88C30 contains all the logic needed for a VHF PLL synthesiser and is fabricated on the GPS high performance, small geometry CMOS process. The circuit contains a reference oscillator and divider, a two-modulus prescaler and 4-bit control register, a 12-bit programmable divider, a phase comparator and the necessary data input and control logic.

FEATURES

- Low Power CMOS
- Easy to Use
- Low Cost
- Single Chip Synthesiser to VHF
- Lock Detect Output

APPLICATIONS

- Mobile Radios
- Hand Held Portable Radios
- Sonobuoys

ORDERING INFORMATION

NJ88C30 KA DP Plastic DIL Package
NJ88C30 KA MP Miniature Plastic DIL Package

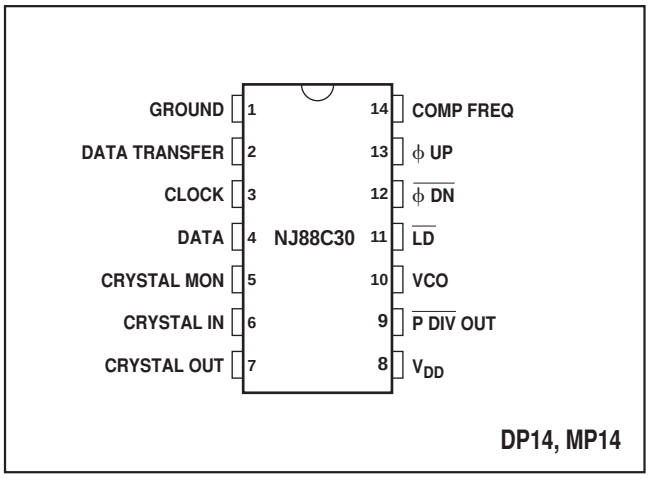


Fig.1 Pin connections - top view

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}	−0·3V to 6V
Voltage on any pin	−0·3V to V_{DD}+0·3V
Operating temperature	−30°C to +70°C
Storage temperature	−55°C to +125°C

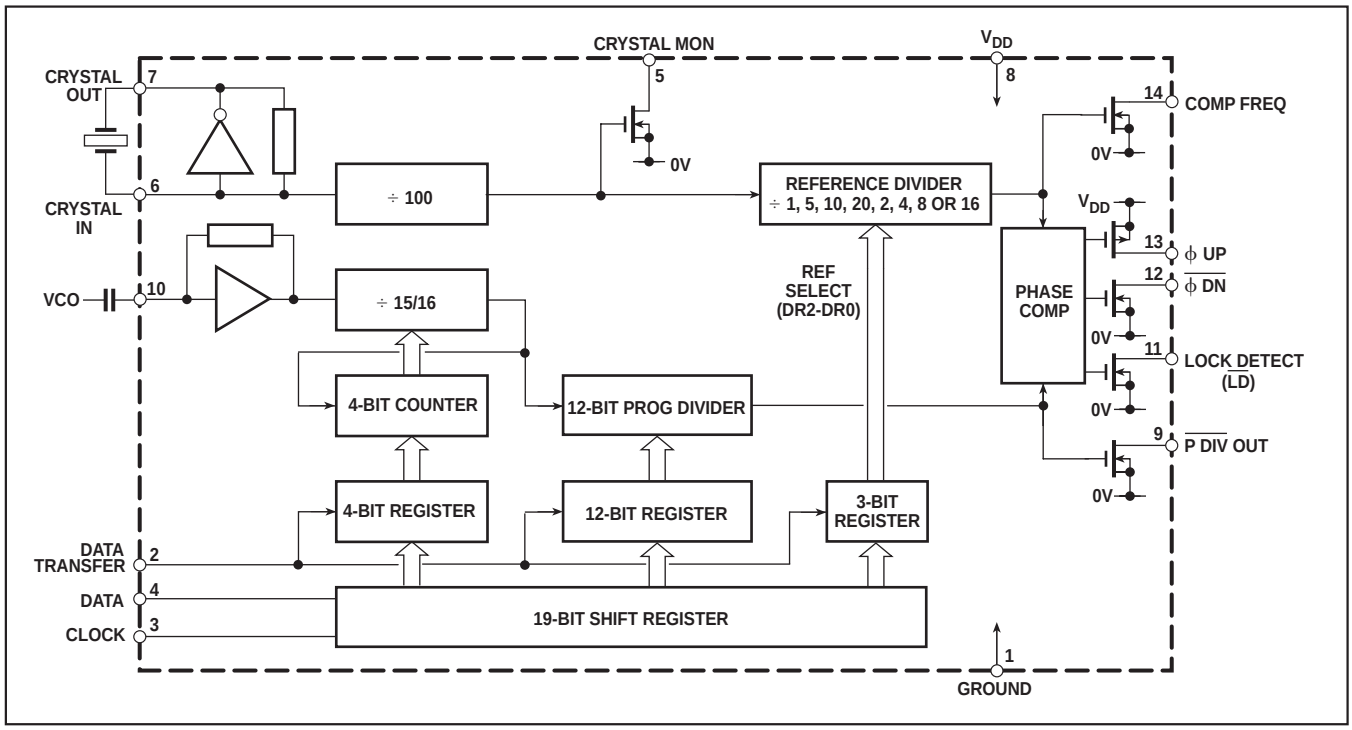


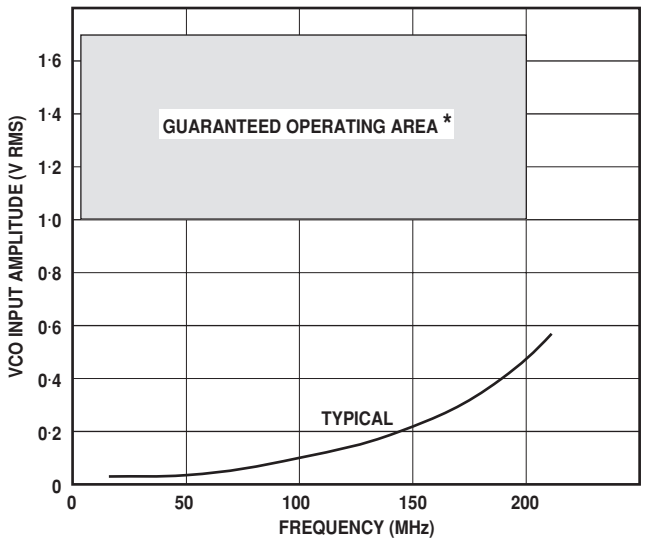
Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

T_{AMB} = –30°C to +70°C, V_{DD} = 5V ±0·5V

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	8		4	7	mA	1VRMS VCO input at 200MHz and f_{XTAL} = 10MHz
Crystal Oscillator						
Frequency	6, 7		10	15	MHz	Parallel resonant, fundamental crystal
External input level	6	1			Vrms	AC coupled
High level	6	$V_{DD}-1$			V	DC coupled
Low level	6			1	V	DC coupled
VCO Input						
Input sensitivity	10	1			Vrms	At 200MHz, see Fig. 3
Slew rate	10	4			V/µs	
Input impedance	10		5pF// 10k			
DATA, DATA TRANSFER and CLOCK Inputs						
High level	2, 3, 4	$V_{DD}-1$			V	
Low level	2. 3, 4			1	V	
Rise, fall time	2, 3			200	ns	
Data set-up time	3, 4	200			ns	See Fig. 4
Clock frequency	3			2	MHz	
Transfer pulse width	2	500			ns	
CRYSTAL MONITOR Output						
Current sink	5	0·8			mA	V_{OUT} = 0·5V
COMP FREQ, $\overline{\text{LD}}$, $\overline{\text{P DIV}}$						
Current sink	9, 11, 14	1·6			mA	V_{OUT} = 0·5V
ϕ UP / $\overline{\phi}$ DN						
Current sink	12	0·8			mA	V_{OUT} = 0·5V
Current source	13	0·8			mA	$V_{OUT} = V_{DD}-0·5V$



* Tested as specified in Table of Electrical Characteristics

Fig. 3 Input sensitivity

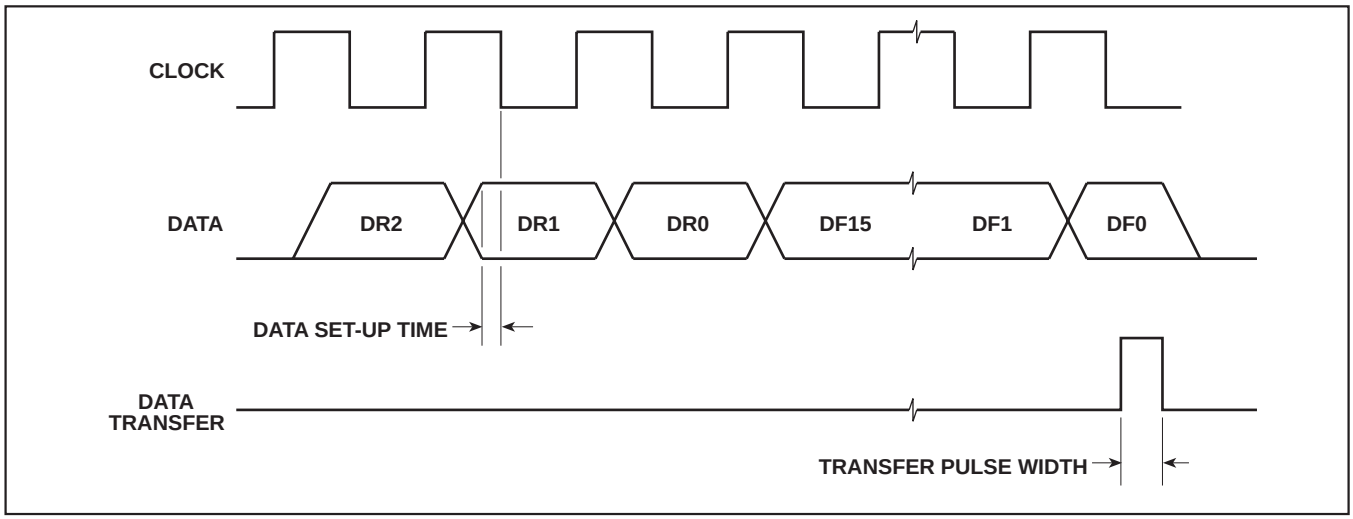


Fig. 4 Input data timing diagram

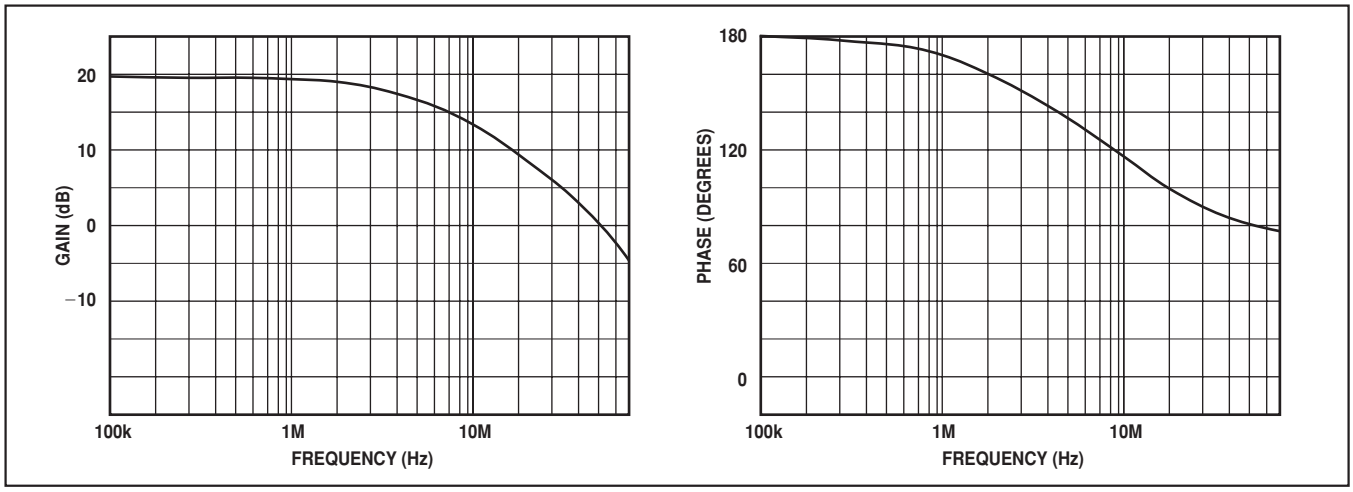


Fig. 5 Gain and phase characteristics of reference oscillator inverter

CIRCUIT DESCRIPTION

Crystal Oscillator and Reference Divider

The Reference oscillator consists of a Pierce type oscillator intended for use with a parallel resonant fundamental crystal. Typical gain and phase characteristics for the oscillator inverter are shown in Fig 5. An external reference oscillator may be used by either capacitively coupling a 1V RMS sinewave into CRYSTAL IN (pin 6) or, if CMOS levels are available, by direct connection to CRYSTAL IN.

The reference oscillator drives a ÷100 prescaler followed by a reference divider to provide a range of comparison frequencies which are selected by decoding the first three bits (DR2, DR1, DR0) of the input data. The possible division ratios and the comparison frequencies (channel spacing) if a 10MHz crystal is used are shown in Table 1.

DR2	DR1	DR0	Total division ratio	Comparison frequency for 10MHz Ref. Osc.
0	0	0	1600	6·25kHz
0	0	1	800	12·5kHz
0	1	0	400	25kHz
0	1	1	200	50kHz
1	0	0	2000	5kHz
1	0	1	1000	10kHz
1	1	0	500	20kHz
1	1	1	100	100kHz

Table 1 Reference divider division ratios

To assist in trimming the crystal, an open drain output at one hundredth of the reference oscillator frequency is provided on CRYSTAL MONITOR pin 5

Programmable Divider

The programmable divider consists of a ÷15/16 two modulus prescaler with a 4-bit control register, followed by a 12-bit programmable divider. A 1V RMS sinewave should be capacitively coupled from the VCO to the divider input VCO pin (pin 10).

The overall division ratio is selected by a single 16-bit word (DF15 to DF0), loaded through the serial data bus. A lower limit of 240 ensures correct prescaler operation; the upper limit is 65535. The VCO frequency in a locked system will be this division ratio multiplied by the comparison frequency.

Phase Comparator

The phase comparator consists of a digital type phase comparator with open drain ϕ UP and ϕ DN outputs and an open drain LOCK DETECT ($\overline{LD}$) output. Open drain outputs from the reference divider and programmable divider are provided for monitoring purposes or for use with an external phase comparator. Waveforms for all these outputs are shown in Fig.6. The duty cycle of ϕ UP and ϕ DN versus phase difference are shown in Fig. 7. The phase comparator is linear over a $\pm 2\pi$ range and if the phase gains or slips by more than 2π, the phase comparator outputs repeat with a 2π period.

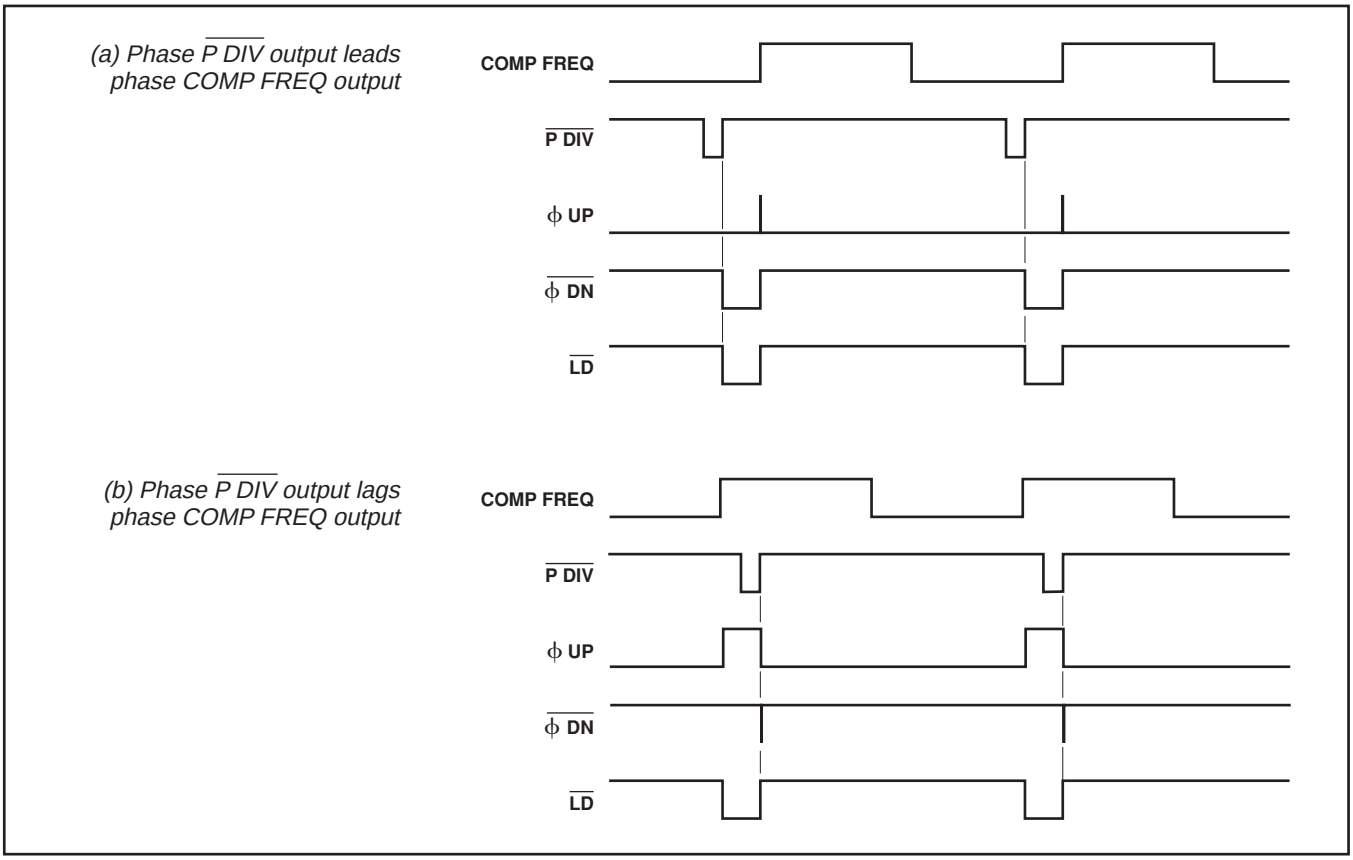


Fig. 6 Phase comparator waveforms

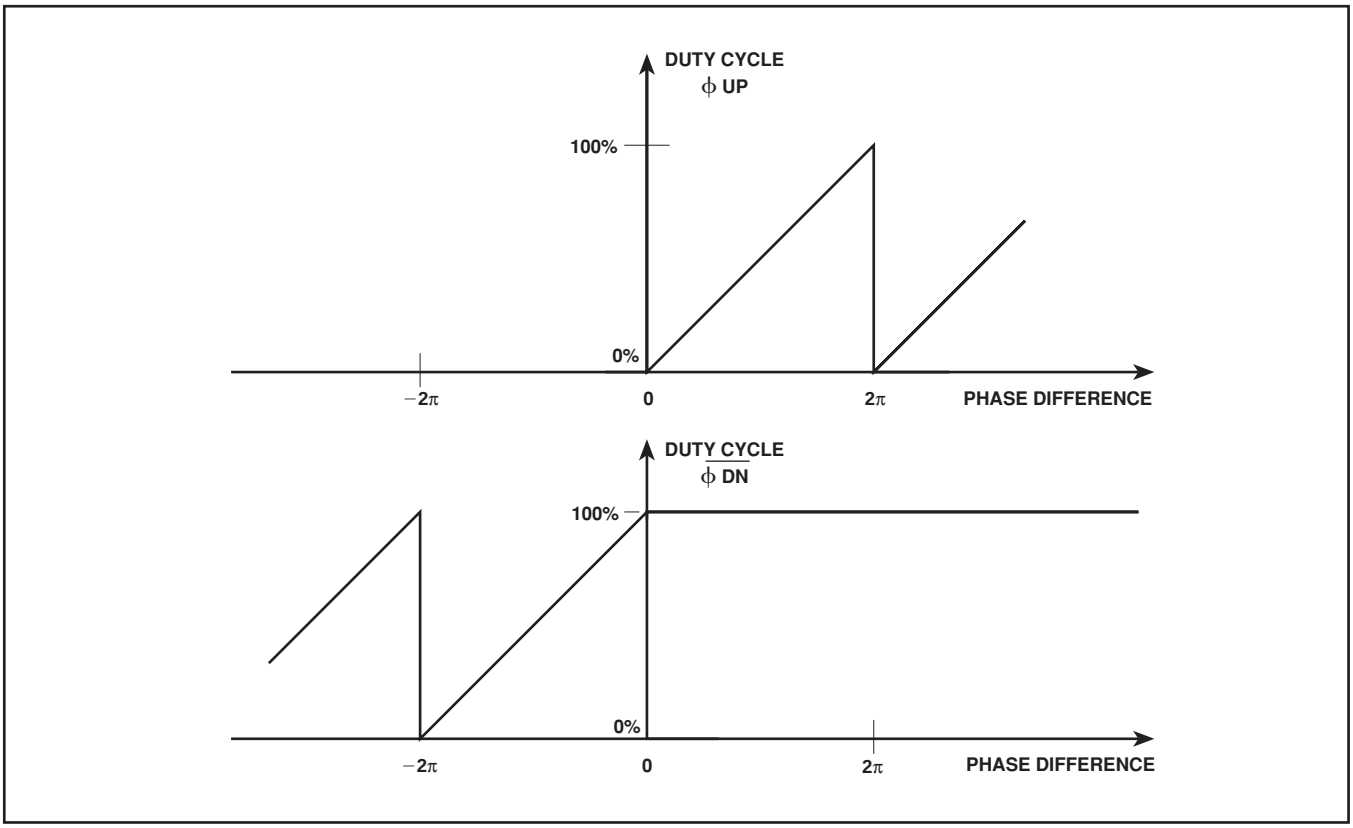


Fig. 7 Phase comparator output characteristics

Once the phase difference exceeds 2π, the comparator will gain or slip one cycle and then try to lock on to the new zero phase difference. Note that very narrow pulses may be seen on the inactive phase comparator output at the end of the pulse on the active output, as shown in Fig. 6.

Data Input and Control Register

To control the synthesiser a simple three-line serial input is used with DATA, CLOCK and DATA TRANSFER signals. The data consists of 19 bits; the first three, DR2, DR1 and DR0, control the reference divider while the following sixteen, DF15 to DF0, control the prescaler and programmable divider. Until the synthesiser receives the DATA TRANSFER pulse, it will use the previously loaded data; on receiving the pulse it will switch rapidly to the new data.

APPLICATIONS

A simplified circuit for a synthesiser intended for VHF broadcast receiver applications is shown in Fig. 8. When the varicap line drive voltage necessary to tune the required band is greater than 5V, some form of level shifter such as the operational amplifier shown in Fig. 8 is required.

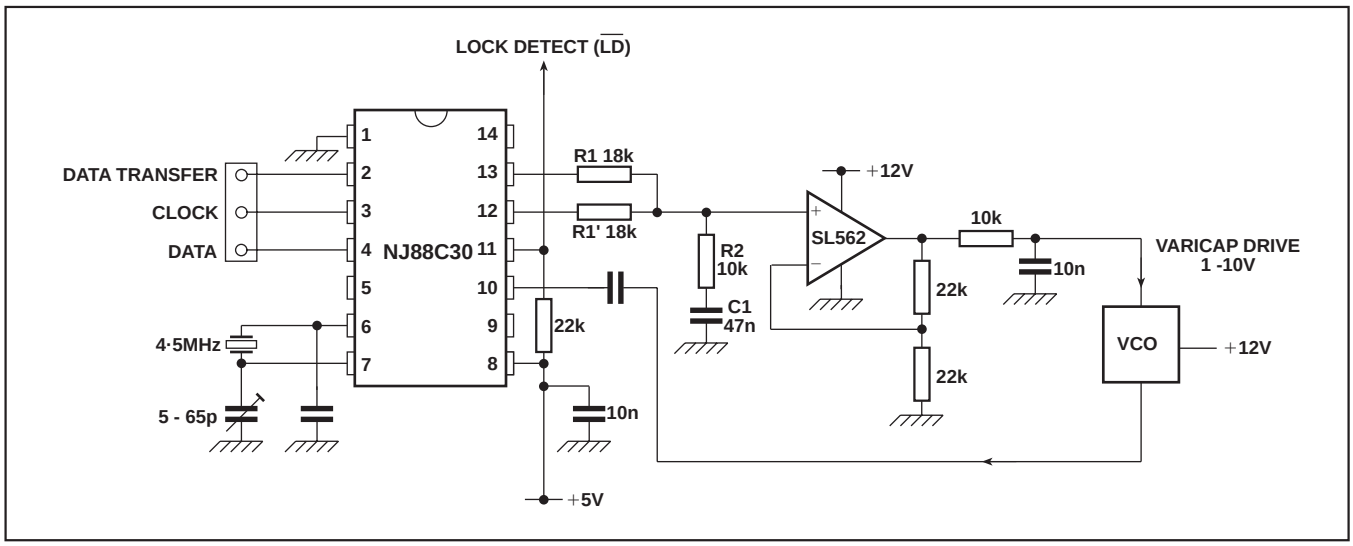


Fig.8. Typical application

PROGRAMMING EXAMPLE

1.Maximum Frequency

For a channel spacing (comparison frequency, f_{comp}) of 5kHz when using a 10MHz crystal oscillator, the reference divider ratio will need to be 2000 (seeTable 1) This is programmed as binary 100 (= 4_{HEX}) in the most significant three of the 19 bits (MSB programmed first).

To obtain the maximum VCO frequency of 200MHz the programmable divider ratio would be:

$$\frac{200\times10^6}{5\times10^3} = 40\times10^3 \text{ which is } 9C40_{HEX}$$

The program word would then be as shown in Table 2.

	DR			DF															
	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary	1	0	0	1	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0
Hex	4			9				C				4				0			

Table 2 Maximum VCO frequency programming (f_{XTAL} = 10MHz, f_{comp} = 5kHz)

2. Minimum Frequency

Using the same crystal frequency and channel spacing (10MHz, 5kHz), the lower limit of programmable divider ratio of 240 = $F0_{HEX}$ gives a minimum programmable VCO frequency of $240\times5\times10^3$ = 1·2MHz. The program word for this frequency is therefore as shown in Table 3.

	DR			DF															
	2	1	0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0
Hex	4			0				0				F				0			

Table 3 MinimumVCO frequency programming (f_{XTAL} = 10MHz, f_{comp} = 5kHz)

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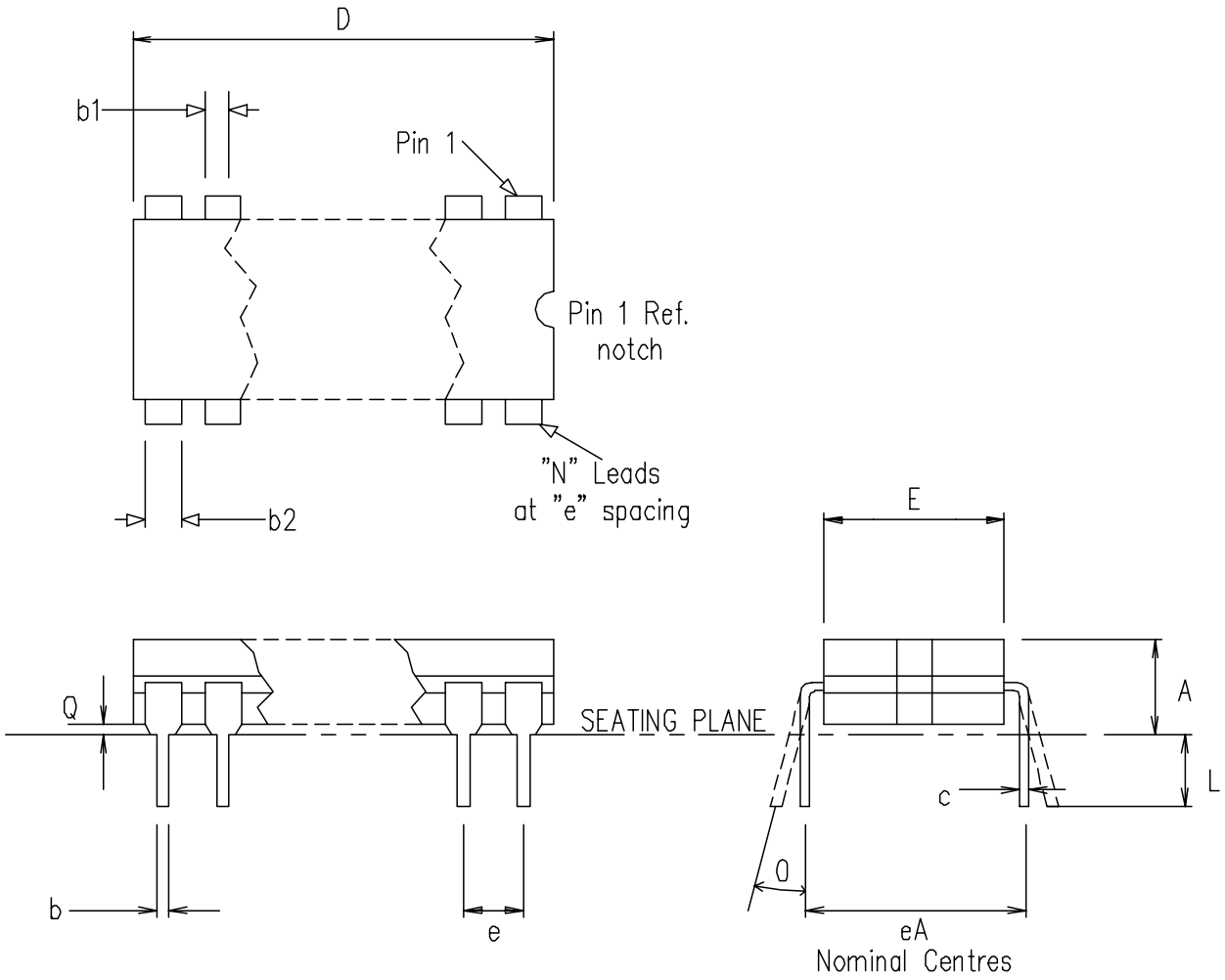

Symbol	Altern. Dimensions in millimetres				Control Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
L	3.18		4.06		0.125		0.160
A			5.08				0.200
Q	0.51				0.020		
E	5.59		7.87		0.220		0.310
eA		7.62				0.300	
c	0.20		0.36		0.008		0.014
D			20.32				0.800
e	2.54 BSC.				0.100 BSC.		
b1	1.14		1.65		0.045		0.065
b	0.36		0.58		0.014		0.023
b2	0.73		1.12		0.029		0.044
0			15°				15°
	Pin features						
N	14						
ND	7						
NE	0						
NOTE	RECTANGULAR						

This drawing supersedes 418/ED/39501/002 (Swindon)

ORIGINATING SITE: SWINDON

ISSUE	1					MITEL SEMICONDUCTOR
ACN	201729					
DATE	20.NOV.96					
APPROVED						

Title: Outline drawing for 14 Lead Cerdip (DG)

Drawing Number
GPD00271

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