NJ88C33

Frequency Synthesiser (I^2C BUS Programmable)

Advance Information

DS2429 - 3.2 September 1994

The NJ88C33 is a synthesiser circuit fabricated on Zarlink Semiconductor's 1.4 micron CMOS process, assuring very high performance. It is I^2C compatible and can also be programmed at up to 5MHz. It contains a 16-bit R counter, a 12-bit N counter and a 7-bit A counter.

A digital phase comparator gives improved loop stability with current source outputs to reduce loop components. A voltage doubler is provided for the loop driver to improve control voltage range to the VCO when operating at low supply voltages.

FEATURES

- Easy to Use
- Low Power Consumption (15mW)
- Single Supply 2.5V to 5.5V
- Digital Phase Comparator with Current Source Outputs
- Serial (I^2C Compatible) Programming, 5MHz max
- Channel Loading in 8µs
- 150MHz Input Frequency Without Prescaler at 4.5V (52MHz at 2.7V)
- Standby Modes
- Use of Two-Modulus Prescaler is Possible

APPLICATIONS

- Cordless Telephones (CT2, DECT)
- Cellular Telephones (GSM, PCN, ETACS)
- Hand Held Marine Radios
- Sonarbuoys
- Video Clock generators

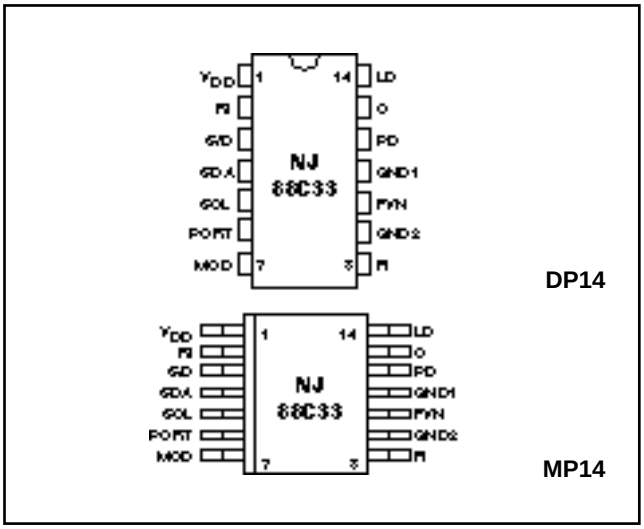


Fig.1 Pin connections (not to scale) - top views

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{DD}	-0.3V to 7V
Input voltage, V_{IM1}	-0.3 to V_{DD} +0.3V
Output voltage on pin 13, V_{IM2}	$-V_{DD}$ to 0V
Storage temperature, T_{stg}	-55°C to +125°C

ORDERING INFORMATION

NJ88C33 MA DP (Industrial - Plastic DIL package)
NJ88C33 MA MP (Industrial - Miniature Plastic DIL package)

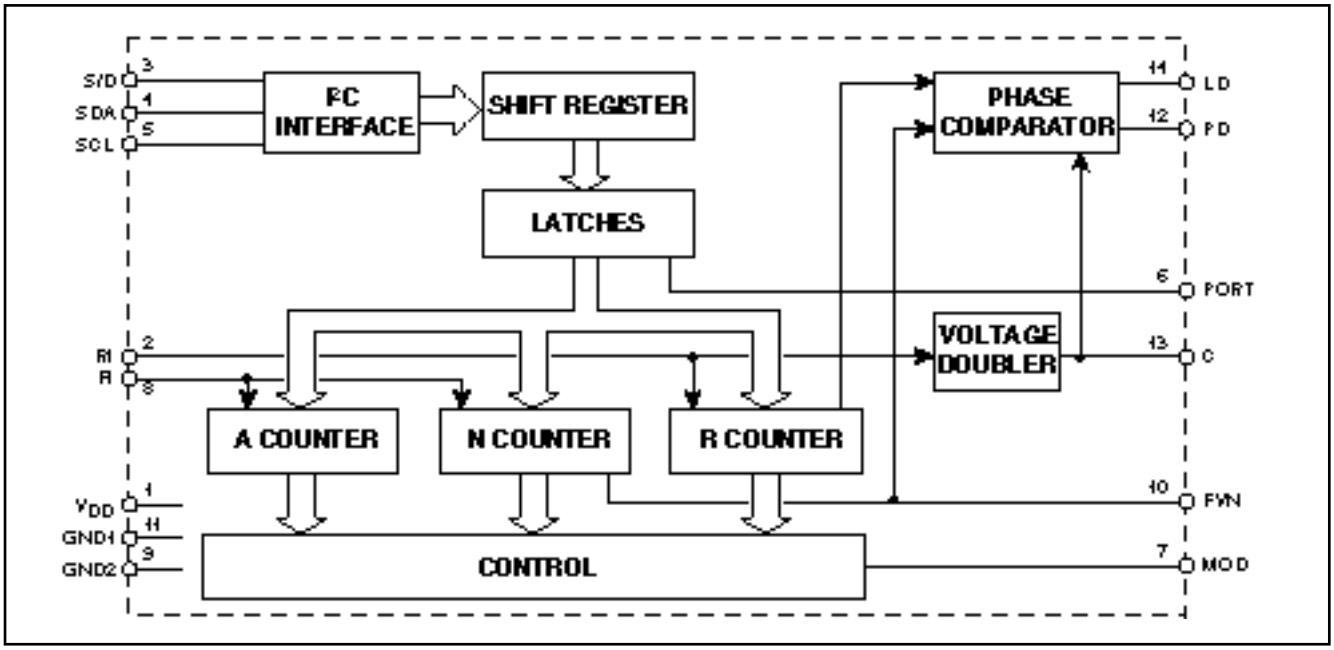


Fig.2 Simplified block diagram of NJ88C33

PIN DESIGNATIONS

Pin No.	Pin Name	Description
1	V_{DD}	Supply voltage (normally 5V or 3V).
2	RI	Reference frequency input from an accurate source, normally a crystal oscillator. The input is normally an AC coupled sinewave but may be a DC coupled square wave.
3	S/D	Single/dual modulus operating mode selection input. Single modulus operation is selected by driving the pin low. 'High' selects dual modulus mode.
4	SDA	I^2C bus data input pin. It is also an open-drain output for generating I^2C bus acknowledge pulses.
5	SCL	I^2C bus clock input. It can be clocked at up to 5MHz.
6	PORT	Output control pin, which can be programmed via the I^2C bus. It can be connected to the S/D pin to select single or dual modulus mode under bus control.
7	MOD	Modulus control pin. It is high in single modulus mode but switches in dual modulus operation. In dual modulus mode, MOD remains low during operation of the A counter until A=0; MOD then remains high until N=0, when both counters are reloaded. It can be programmed via the I^2C bus as an open-drain or push-pull output.
8	FI	Frequency input from a VCO or prescaler. The input is normally an AC coupled sinewave but may be a DC coupled square wave.
9	GND2	Dedicated ground for the FI input buffer. It should be connected to the VCO ground or the prescaler ground, if used. Any noise on this pin will affect the performance of the VCO loop.
10	FVN	Open-drain output from the N counter.
11	GND1	Ground supply pin (global).
12	PD	Tristate current output from the phase detector. The polarity of the output can be programmed via the I^2C bus.
13	C	Voltage doubler output. The operation of the doubler can be controlled via the I2C bus. In applications where the voltage doubler is switched off, this pin should be connected to GND1; a reservior capacitor should be connected from this pin to GND1 for applications where it is switched on.
14	LD	Open-drain lock detect output - requires integration if used.

OPERATING RANGE

Test conditions (unless otherwise stated):

PLL locked, RI = 10MHz

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	2.5	5	5.5	V	
Ambient temperature	T_{amb}	-40		+85	°C	
Supply current						
Single modulus	I_{DD}		2.1	3.0	mA	FI = 50MHz, V_{FI} = 150mVrms, N,R > 1000 without voltage doubler, V_{DD} = 5V, T_{amb} = 25°C
Dual modulus	I_{DD}		2	3.0	mA	FI = 10MHz, V_{FI} = 500mVrms, N,R > 1000 without voltage doubler, V_{DD} = 5V, T_{amb} = 25°C
Standby mode	I_{DD}			1	µA	FI = 50MHz, V_{FI} = 150mVrms, preamp off, divider off, V_{DD} = 5V, T_{amb} = 25°C
Standby mode	I_{DD}		1.0	1.5	mA	FI = 50MHz, V_{FI} = 150mVrms, preamp on, divider off, V_{DD} = 5V, T_{amb} = 25°C

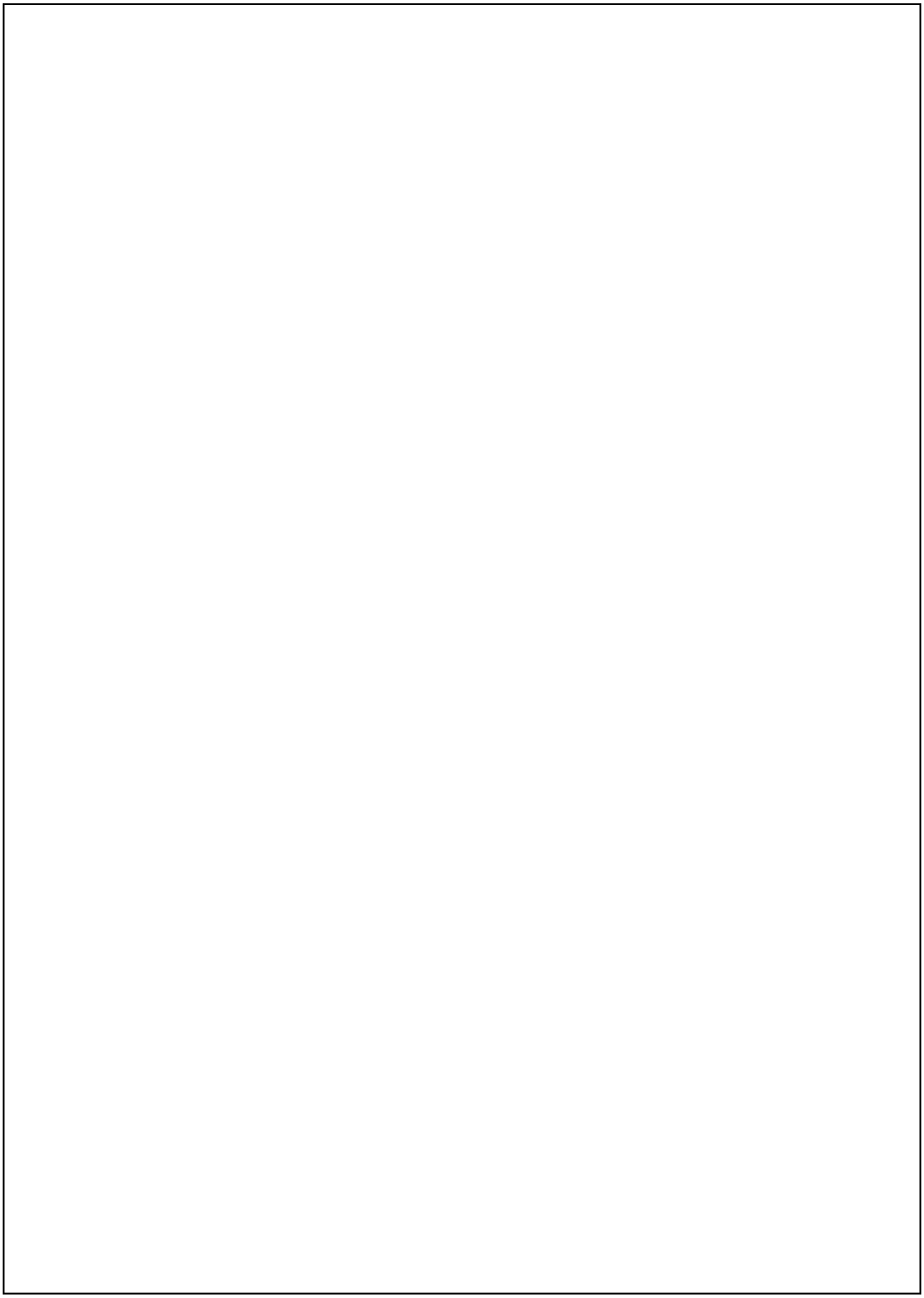


Fig.3 Functional block diagram

ELECTRICAL CHARACTERISTICS

These characteristics are guaranteed over the following conditions (unless otherwise stated):

V_{DD} = 4.5V to 5.5V, T_{amb} = -40°C to +85°C

INPUT SIGNALS

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Input Signals SDA, SCL, S/D						
Input voltage high	V_{IH}	0.7V_{DD}		V_{DD}	V	
Input voltage low	V_{IL}	0		0.3V_{DD}	V	
Input capacitance	C_I			10	pF	
Input current	I_{IN}			10	µA	V_{IN} = V_{DD} = 5.5V
Input signal RI						
Input frequency	f_{max}			52	MHz	Sinewave input
Input voltage	V_{Irms}	100			mV	Note 1, 2
Input capacitance	C_I			10	pF	
Input current	I_{IN}			10	µA	V_{IN} = V_{DD} = 5.5V
Input signal FI						Dual modulus operation
Input frequency	f_{max}			52	MHz	Sinewave input
Input voltage	V_{Irms}	50			mV	Note 1, 2
Input capacitance	C_I			10	pF	
Input current	I_{IN}			10	µA	V_{IN} = V_{DD} = 5.5V
Input signal FI						Single modulus operation
Input frequency	f_{max}			150	MHz	Sinewave input
Input voltage	V_{Irms}	30			mV	FI = 0-70MHz Note 1, 2
	V_{Irms}	100			mV	FI = 70-120MHz Note 1, 2
	V_{Irms}	200			mV	FI = 120-150MHz Note 1, 2
Input capacitance	C_I			10	pF	
Input current	I_{IN}			10	µA	V_{IN} = V_{DD} = 5.5V

Note.1Lowest noise floor achieved at 10dB above this level with I^2C bus operating. The source impedance should be less than 2kΩ.

Note.2DC coupled input amplitude V_{IRMS} > 0.8V_{DD}.

OUTPUT SIGNALS

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Output Signals SDA, LD						
Output voltage low	V_{OL}			0.4	V	Open drain, I_{OL} = 3mA
Output Signal PD						C_L = 400pF, tristate output
High current mode (see Fig.4)	I_{HU}	1.9	2.5	3.1	mA	0 < V_{PD} < 4.5, V_{DD} = 5V, T = 25°C Note 1
	I_{HD}	-1.9	-2.5	-3.1	mA	0.4 < V_{PD} < 5, V_{DD} = 5V, T = 25°C Note 1
Low current mode	I_{LU}	0.475	0.625	0.775	mA	0 < V_{PD} < 4.6, V_{DD} = 5V, T = 25°C Note 1
	I_{LD}	-0.475	-0.625	-0.775	mA	0.4 < V_{PD} < 5, V_{DD} = 5V, T = 25°C Note 1
Tristate	I_Z		50		nA	T_{amb} = -25°C to +60°C
Output Signal FVN						Open drain output
Output voltage low	V_{OL}			0.4	V	I_{OL} = 1mA
Output low pulse width	t_{WL}			1/FI		C_L = 30pF
Output Signals MOD, PORT						Push-pull output
Output voltage high	V_{OH}	V_{DD}-0.4			V	IOH = 0.5mA
Output voltage low	V_{OL}			0.4	V	I_{OL} = 0.5mA
Output Signal LD						Open drain output
Output voltage low	V_{OL}			0.4	V	I_{OL} = 3mA, C_L = 30pF
Output low pulse width	t_{WL}		10	1/FVN	ns	Loop locked
				$1/f_C$		Loop not locked
						FVN = FI/N
						f_C = RI/R

Note.1Temperature coefficient for current is typically -0.7%/°C

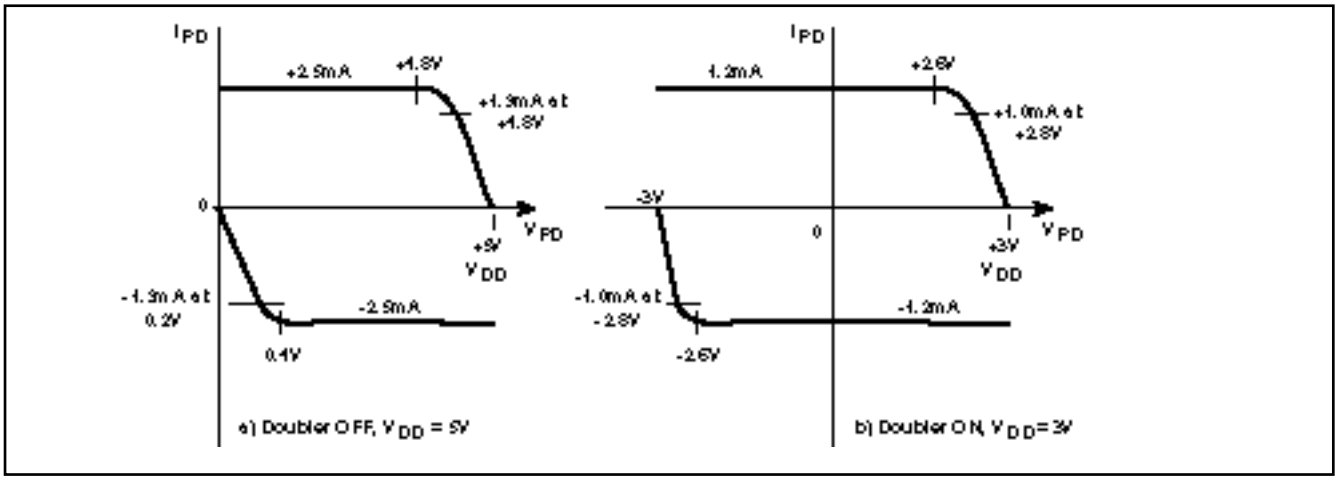


Fig. 4 Typical output signal PD, high current mode

VOLTAGE DOUBLER $V_{DD} \leq 3V$

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Output Pin C						
Output voltage	V_C	$-V_{DD}$		$-V_{DD}$ + 0.8V	V	f_{VD} = 2MHz, I_{OC} = 0µA, V_{DD} = 3V
	V_C	$-V_{DD}$		$-V_{DD}$ + 1.5V	V	f_{VD} = 2MHz, I_{OC} = 100µA, V_{DD} = 3V
Current Consumption	I_D			100	µA	f_{VD} = 2MHz, I_{OC} = 0µA, V_{DD} = 3V

TIMING INFORMATION

Characteristic	Symbol	Value			Unit	Conditions
		Min.	Typ.	Max.		
Input Signal RI						
Input frequency	f_{max}	0		52	MHz	
Input frequency	f_{max}	0		10	MHz	V_{DD} = 2.7V
Rise time	t_R			1.5	µs	
Fall time	t_F			1.5	µs	
Slew rate		3			V/µs	
Input Signal FI						Dual modulus
Input frequency	f_{max}	0		52	MHz	
Input frequency	f_{max}	0		20	MHz	V_{DD} = 2.7V
Rise time	t_R			1.5	µs	
Fall time	t_F			1.5	µs	
Slew rate		3			V/µs	
Input Signal FI						Single modulus
Input frequency	f_{max}			150	MHz	
Input frequency	f_{max}	0		52	MHz	V_{DD} = 2.7V
Rise time	t_R	0		1.5	µs	
Fall time	t_F			1.5	µs	
Slew rate		3			V/µs	
Output Signal PORT						
Rise time	t_R			1	µs	C_L = 30pF
Fall time	t_F			1	µs	C_L = 30pF
Output Signal FVN						
Fall time	t_F		20		ns	C_L = 30pF
Output Signal MOD						
Rise time	t_R			10	ns	C_L = 30pF
Fall time	t_F			10	ns	C_L = 30pF
Delay time (L→H)	t_{DLH}			15	ns	C_L = 30pF Measured from +Ve edge of FI
Delay time (H→L)	t_{DHL}			15	ns	C_L = 30pF Measured from +Ve edge of FI

PHASE COMPARATOR

The phase comparator produces current pulses of duration equal to the difference in phase between the comparison frequency (fc=RI/R), and f_{VN}, the divided-down VCO frequency (FI/N).

When status bit 4 is set high the positive polarity mode of the output PD is selected. When fc leads f_{VN} the PD output goes high; when f_{VN} ieads fc it goes low. Similarly, selecting the negative polarity mode of PD by programming bit 4 of the status register low causes PD to have the inverse polarity. The loop filter integrates the current pulses to produce a voltage drive to the VCO.

No pulses are produced when locked. The lock detect output, LD, produces a logic '0' pulse equal to the phase difference between f_C and f_{VN}.

When the phase difference between fc and f_{VN} is too small to be resolved by the phase detector then no current pulses are produced. In this region the loop does not reduce the close-in noise on the VCO output. This can be overcome using a very high value resistor to leak a few nanoAms of current from the filter and keep the loop on the edge of the region.

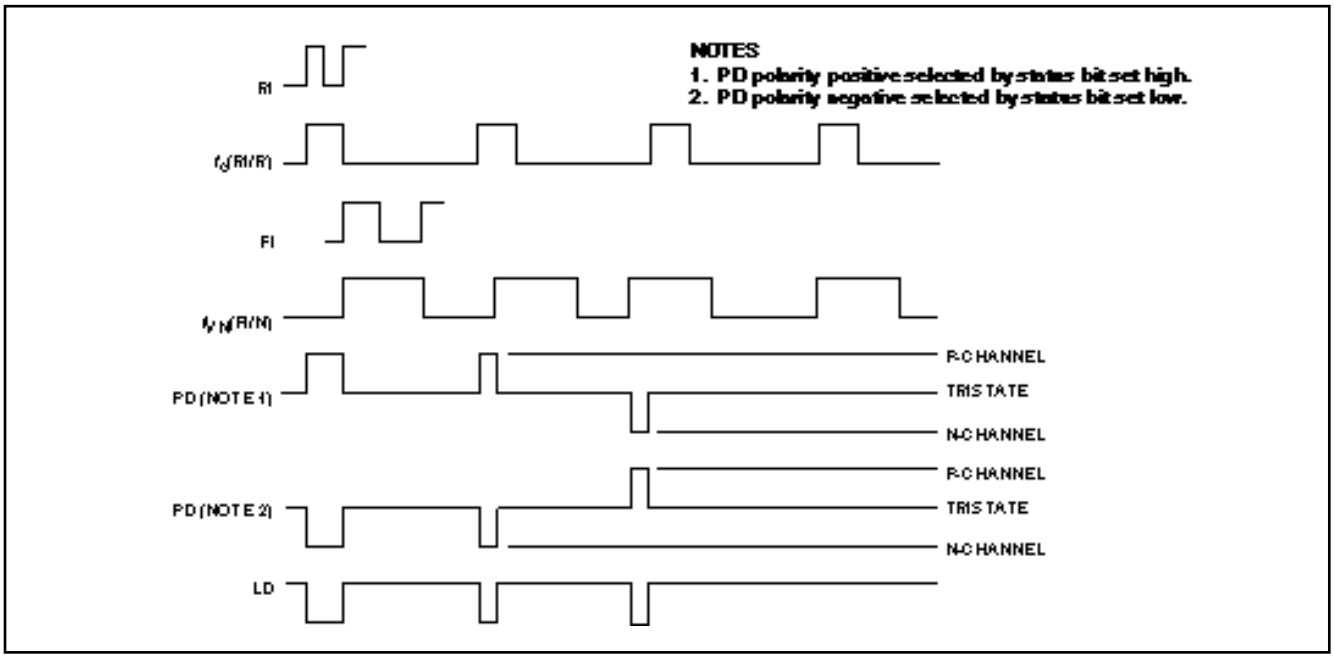


Fig. 5 Phase comparator phase diagram

PROGRAMMING

Transmission Protocol

I^2C programming messages consist of an address byte followed by a sub-address byte followed by 1, 2 or 3 bytes of data. Bit 7 of the address byte must match the setting of the S/D pin for the address to be recognised. This allows for separate addressing of two NJ88C33 synthesisers on the same bus. The sub-address should be set to select the correct registers to be programmed and should be followed by the appropriate number of data bytes. Registers are not programmed until the complete message protocol has been checked.

Each message should commence with a START condition and end with a STOP condition unless followed immediately by another transfer, when the STOP condition may be omitted.

Data is transferred from the shift register to the latches on a STOP condition or by a second START condition.

A START condition is indicated by a falling edge on the Serial Data line, SDA, when the Serial Clock line. SCL, is high.

A rising edge on SDA when SCL is high indicates a STOP condition as shown in Fig.6.

Data on SDA is clocked into the NJ88C33 on the rising edge of SCL. The NJ88C33 acknowledges each byte transferred to it by pulling the SDA line low for one cycle of SCL after the last bit has been received.

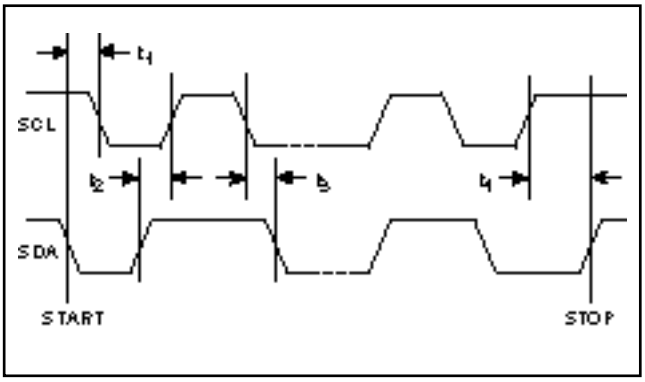


Fig. 6 I^2C timing diagram

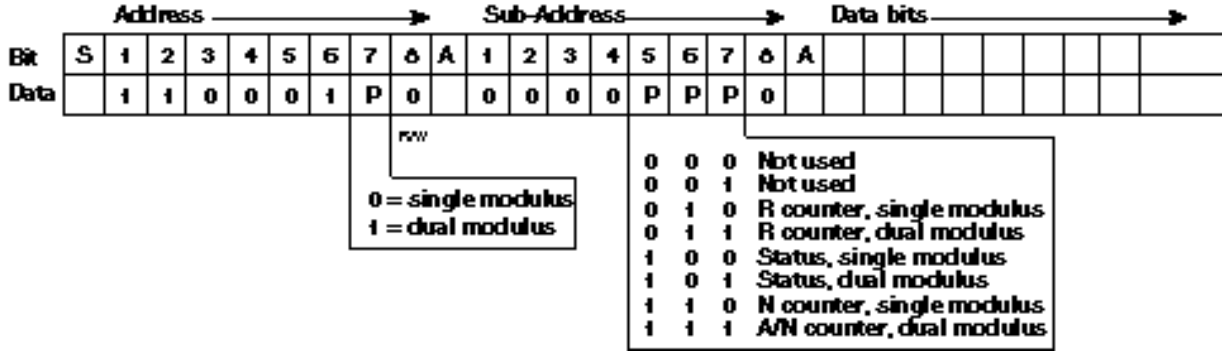
I2C TIMING INFORMATION

VDD = 4.5V to 5.5V, Tamb = -40°C to +85°C

Parameter	Symbol	Value		Unit
		Min.	Max.	
Serial clock frequency	f_{SCL}		5	MHz
SCL hold after START	t_1	200		ns
Data set-up time	t_2	20		ns
Data hold after SCL low	t_3	0		ns
SCL set-up before STOP	t_4	20		ns

Address and Sub-Address Formats

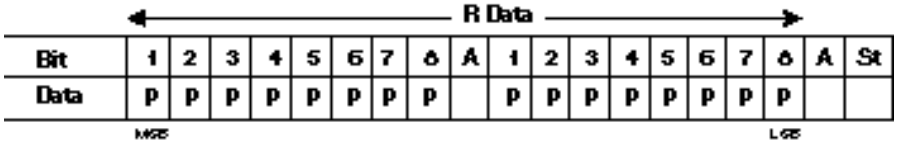
The correct addressing sequence for the NJ88C33 is shown below. The START condition is followed by the address byte, the acknowledge from the NJ88C33, the sub-address byte, another acknowledge then the associated data. The correct values for each address and sub-address are listed, together with the message selection options.



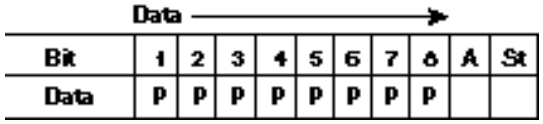
Data Formats

Each of the data formats should be preceded contiguously by the addressing sequence given above.

R counter : single or dual modulus



Status : single or dual modulus

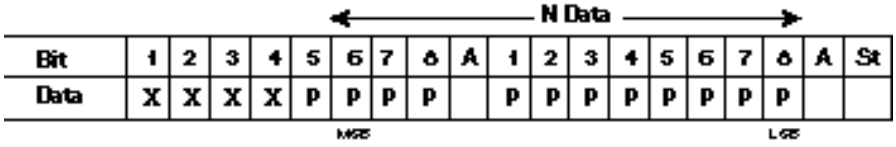


Status Byte		
Bit	**0**	**1**
1	PORT = low	PORT = high
2	Counters off (1)	Counters on
3	FI and RI off (2)	FI and RI on
4	PD = polarity negative	PD = polarity positive
5	PD bias = 0.625mA	PD bias = 2.5mA
6	f_{VD} = RI/2	f_{VD} = RI/4
7	Doubler off	Doubler on (3)
8	MOD = push-pull	MOD = open drain

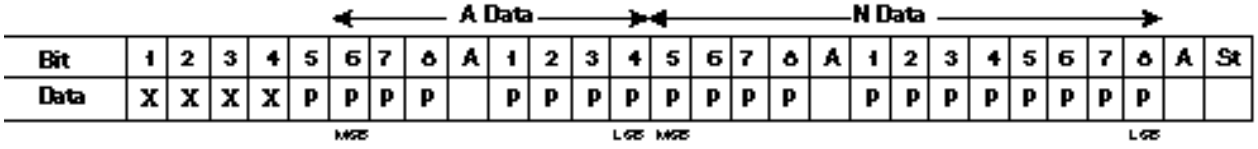
NOTES

1. In this standby mode the counters are disabled but the voltage doubler and I²C interface can both function.
2. In this standby mode the FI and RI preamplifiers are disabled, which stops the counters and the voltage doubler. The I²C interface still operates.
3. The voltage doubler should only be used when $V_{DD} \leq 3.0V$

N counter : single modulus



A/N counters : dual modulus



APPLICATION CIRCUITS

Single Modulus

In this mode, the NJ88C33 synthesiser can be used with or without a fixed modulus prescaler. The R counter is programmed with a value to produce a comparison frequency fc. When the N counter is changed by 1 the loop is no longer in lock and the phase detector output produces current pulses to bring the loop back into lock. These pulses are integrated by the loop fiiter to produce the VCO voltage drive. When the VCO loop is locked, Fl/N=f_C i.e., the VCO frequency is N x f_C.

Using a prescaler with a division ratio P, the smallest VCO output frequency step is Pf_C and the VCO frequency is PNf_C.

If a low pass filter is connected to the lock detect output as shown and sampled by the microprocessor, the proximity of the synthesiser loop to lock can be evaluated.

The A counter is not used in this mode.

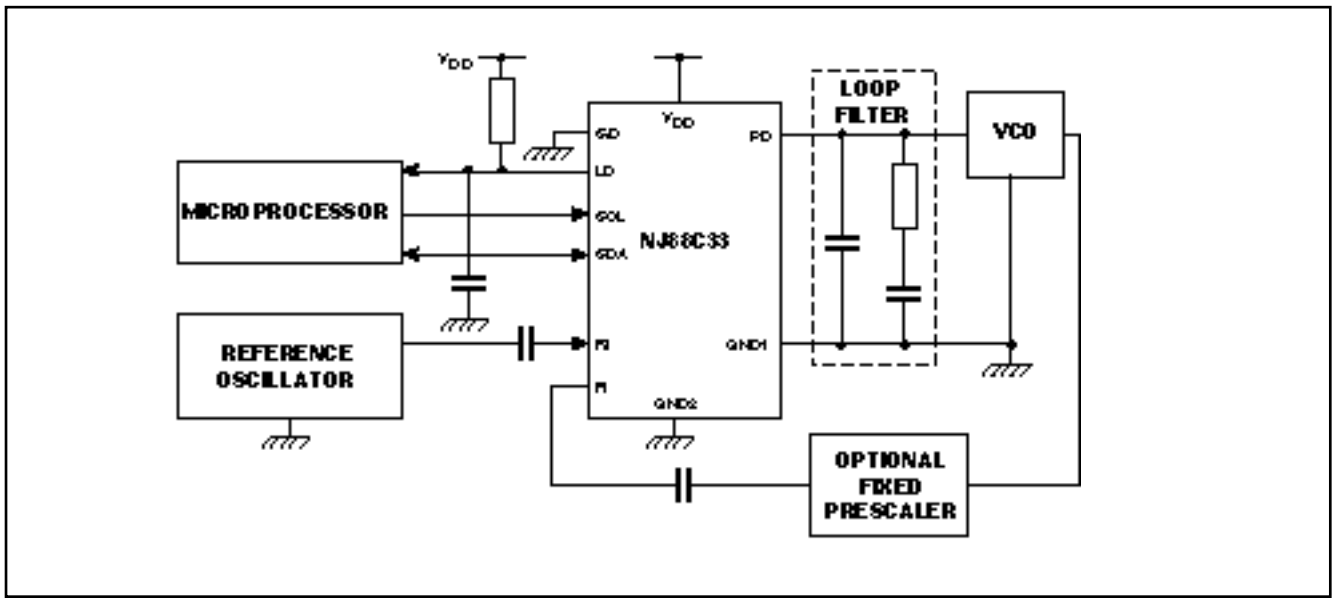


Fig. 7 Single modulus application

Dual Modulus

This mode allows much higher frequencies to be used in conjunction with a prescaler but maintains the step size, fc. In this mode, a dual modulus prescaler (with ratios P and P + 1) must be used with the NJ88C33. The A counter controls the MOD output, which is used to select the division ratio of the prescaler.

When the A counter is non-zero, the MOD output is low and goes high when the A counter has counted down to zero. MOD remains high until the N counter reaches zero, when both counters are re-loaded. Thus, the prescaler divides by P for N-A cycles and by P + 1 for A cycles of Fl. The VCO frequency is given by $PNf_C + Af_C$.

Note that programming A = 0 produces a count of 128 cycles.

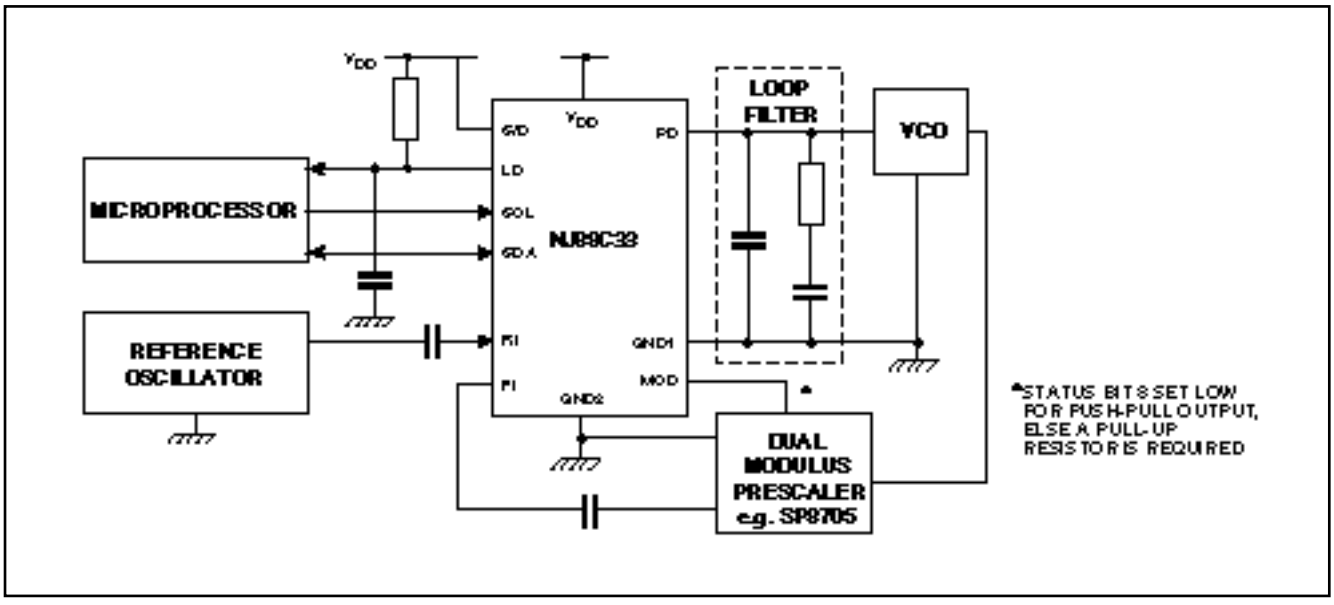


Fig. 8 Dual modulus application

VCO Driving Without Voltage Doubler

To switch off the voltage doubler, bit 7 of the status register is programmed low. This will reduce current consumption and minimise noise. The voltage doubler output C should be connected to GND1 as connection to GND2 would induce noise in the VCO loop.

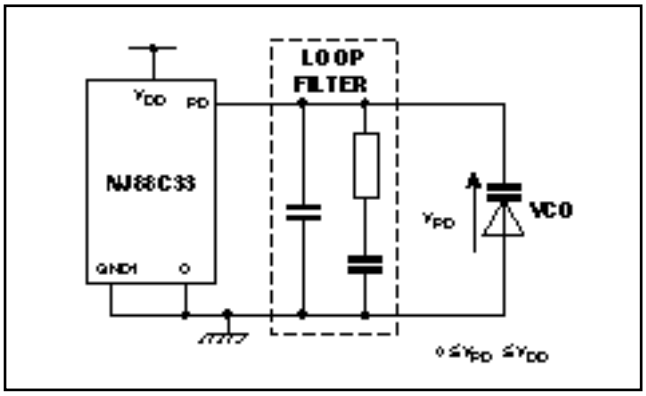


Fig. 9 Driving a VCO without voltage doubler

VCO Driving With Voltage Doubler

The voltage doubler is switched on by setting bit 7 of the status register high. It is recommended that a reservoir capacitor of at least 1µF be connected from C to GND1.

The voltage doubler is designed to boost VCO drive in low voltage applications.

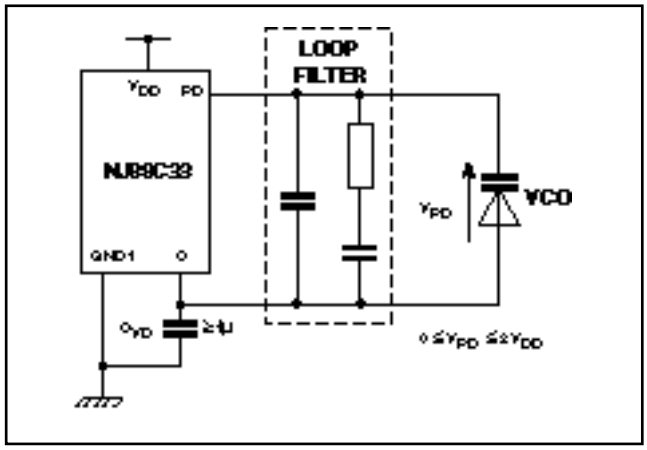


Fig. 10 Driving a VCO using the voltage doubler

Further Applications Information

A stand-alone programmer card and an evaluation board are available for evaluating the NJ88C33. The programmer card allows two sets of variables to be programmed into both the divider and status registers during alternate programming cycles, at either the standard I^2C bus rate of 100kHz or at 2MHz.

Initialisation is with either a manual push-button or by an external logic level pulse; a synchronisation output is provided to allow a quick assessment of 'step' and 'settle' responses to be made.

The NJ88C33 evaluation board (Fig. 11) dernonstrates the preferred layout technique - providing a reference oscillator, a 60 to 80MHz VCO and a simple loop filter to complete a minimal frequency synthesiser loop. The two units allow analysis of different loop variables as well as the selection of comparison frequencies for fast frequency-hopping loops.

Application Note: AN94, *'Using* the NJ88C33 *PLL Synthesiser'* explains the design equations and demonstrates the use of the device, and is available from your local Zarlink Semiconductor customer service centre.

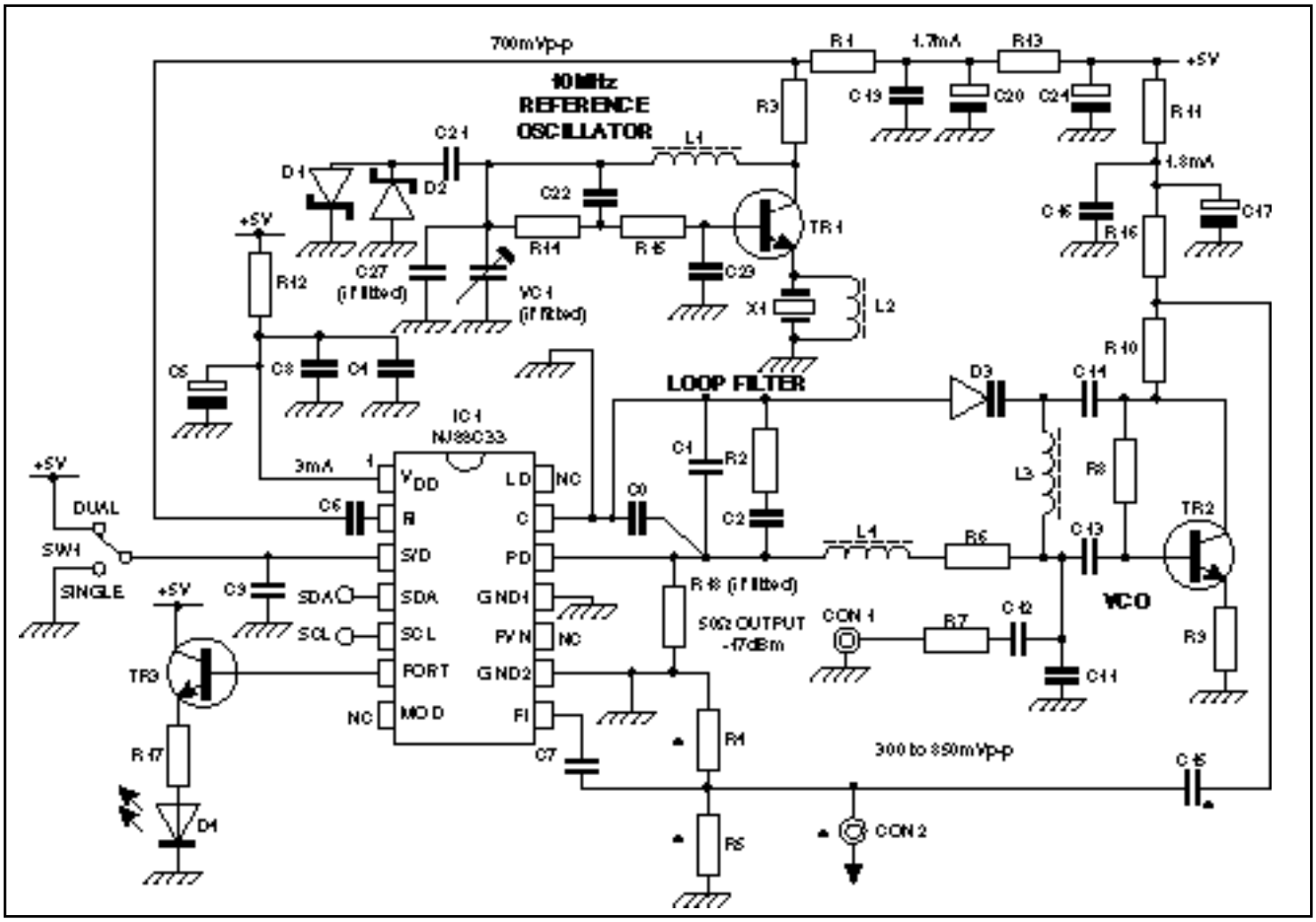


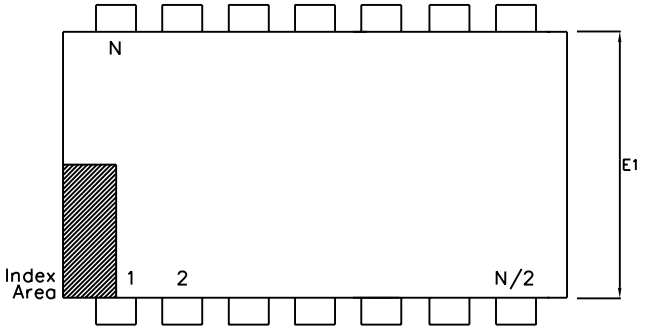
Fig. 11 Typical applications circuit

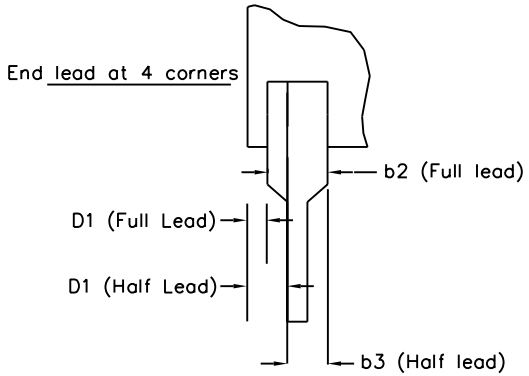
* Insert C15, delete R4 and R5 if CON2 is to be used to monitor the VCO. Delete C15 insert R4 and R5 if CON is to provide an external source, otherwise short C15 and delete R4, R5 and CON2.

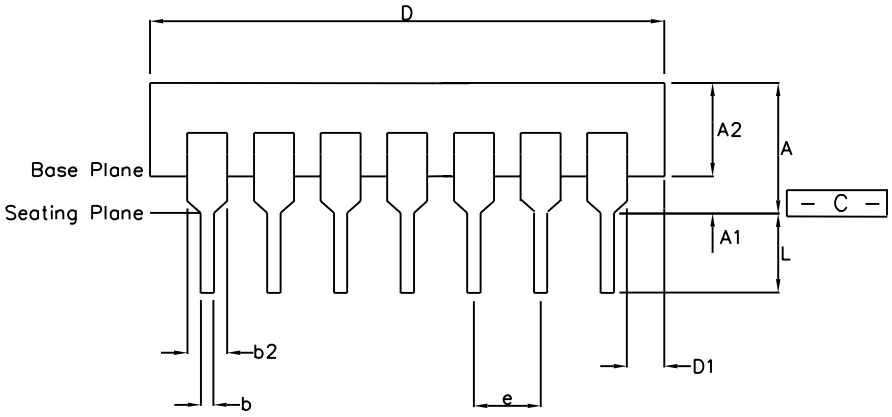
COMPONENT LIST FOR FIG. 11

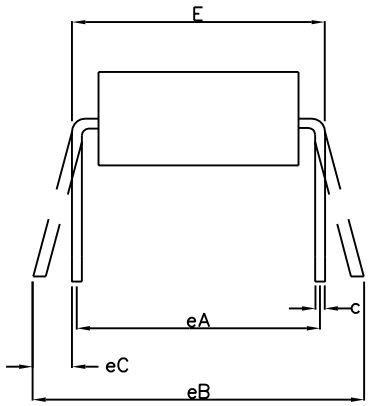
Capacitors				Resistors		Inductors		Miscellaneous	
C0	1nF 10%	C17	22µF/35V Elect.	R1	270Ω	L1	15µH 10%	IC1	NJ88C33
C1	100nF 10%	C19	10nF 10%	R2	470Ω	L2	220µH 10%	X1	10.00MHz 5ppm series
C2	1µF Tant.	C20	22µF/35V Elect.	R3	330Ω	L3	180nH 20%	SW1	Miniature slide switch
C4	10nF 10%	C21	10nF 10%	R4	100Ω	L4	470µH 10%	CON1	SMC socket
C5	22µF/35V Elect.	C22	10nF 10%	R5	100Ω			CON2	SMC socket
C6	10nF 10%	C23	22pF 5% NPO	R6	1kΩ	**Diodes**		PCB	C33ISS2
C7	1nF 10%	C24	22µF/35V Elect.	R7	120Ω				
C8	1nF 10%	C27	22pF 5% NPO	R8	27kΩ	D1	1N6263 Schottky		
C9	1nF 10%	VC1	3p5-22p	R9	Link	D2	1N6263 Schottky		
C11	150pF 5% NPO			R10	1kΩ	D3	BBY40 varicap		
C12	1nF 10%			R11	10Ω	D4	5mm red LED		
C13	1nF 10%			R12	10Ω				
C14	2p7 ± 0.5pF NPO			R13	10Ω	**Transistors**			
C15	10nF 10%			R14	22kΩ				
C16	10nF 10%			R15	2.7kΩ	TR1	BFS17 RF NPN		
				R16	330R	TR2	BFS17 RF NPN		
				R17	100Ω	TR3	2N3904 Switching		
				R18	33MΩ				

NOTES
1. With the exception of electrolytics, all capacitors are surface mount types.
2. All resistors are 0.25W, ±2%.
3. C0, C1, C2, C11, C12, C13 and C14 must be low leakage types.
4. R18 may be required to optimise VCO close in noise performance.









	Min mm	Max mm	Min Inches	Max Inches
A		5.33		0.210
A1	0.38		0.015	
A2	2.92	4.95	0.115	0.195
b	0.36	0.56	0.014	0.022
b2	1.14	1.78	0.045	0.070
b3	n/a	n/a	n/a	n/a
c	0.20	0.36	0.008	0.014
D	18.67	19.69	0.735	0.775
D1	0.13		0.005	
E	7.62	8.26	0.300	0.325
E1	6.10	7.11	0.240	0.280
e	2.54 BSC		0.100 BSC	
eA	7.62 BSC		0.300 BSC	
eB		10.92		0.430
eC	0.00	1.52	0.000	0.060
L	2.92	3.81	0.115	0.150
N	14		14	
Conforms to Jedec MS-001AA Issue D				

This drawing supersedes: –
Plymouth/Swindon drawing # 418/ED/39502/002

Notes:
1. Dimensions D, D1 & E1 do not include mould flash or protrusions.
2. Dimensions E & eA are measured with leads constrained to be perpendicular to datum – C –
3. Dimensions eB & eC are measured with the leads unconstrained
4. Controlling dimensions are Inches. Millimeter conversions are not necessarily exact.
5. N is the maximum of terminal positions.

ISSUE	1	2		
ACN	202539	212482		
DATE	23May97	5Apr02		
APPRD.				

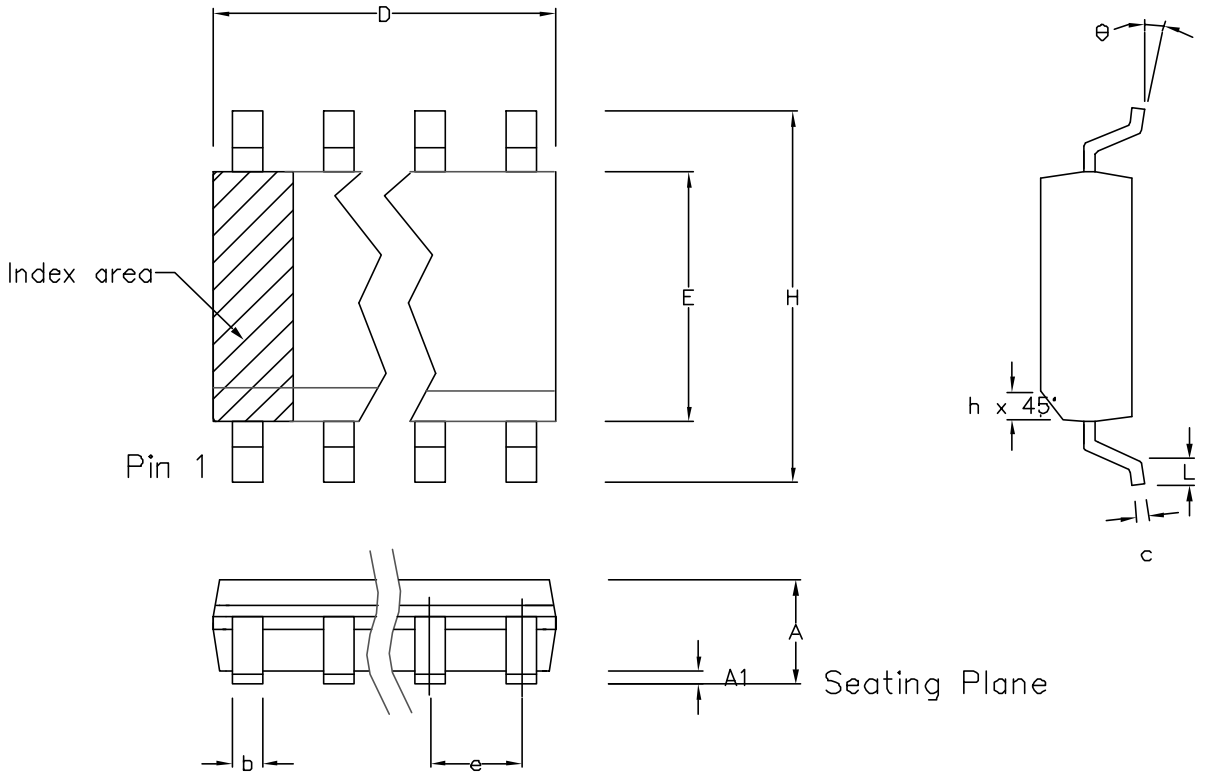
ZARLINK SEMICONDUCTOR

Previous package codes
DP / E

Package Code DA

Package Outline for
14 lead PDIP

GPD00344



	Min mm	Max mm	Min inch	Max inch
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	8.55	8.75	0.337	0.344
H	5.80	6.20	0.228	0.244
E	3.80	4.00	0.150	0.157
L	0.40	1.27	0.016	0.050
e	1.27 BSC		0.050 BSC	
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
θ	0°	8°	0°	8°
h	0.25	0.50	0.010	0.020
	Pin Features			
N	14		14	
Conforms to JEDEC MS-012AB Iss. C				

Notes:

1. The chamfer on the body is optional. If not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimensions are in inches.
3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protusion / intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

ISSUE	6	2	3	4	5
ACN	214220	201937	202596	203707	212430
DATE	7Apr03	27Feb97	12Jun97	9Dec97	25Mar02
APPRD.					

ZARLINK SEMICONDUCTOR

Previous package codes

MP / S

Package Code DC

Package Outline for 14 lead SOIC (0.150" Body Width)

GPD00011

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www.zarlink.com

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