TWO OUTPUT HIGH VOLTAGE SWITCHING REGULATOR

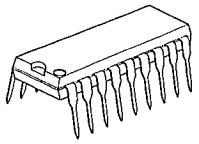
■ GENERAL DESCRIPTION

New JRC's high voltage switching regulator, NJM2355, is a monolithic high voltage (50V max) operation integrated circuit consisting of two channel PWM controlers.

The NJM2355 contains an internal 5V refernce, free running oscillator, low supply voltage detector, two comparators and three error amplifiers. The error amp 2 or amp 3 is for current limiting in channel B output circuit.

The NJM2355 is suited for DC to DC converter application; step up, step down, positive to negative.

■ PACKAGE OUTLINE

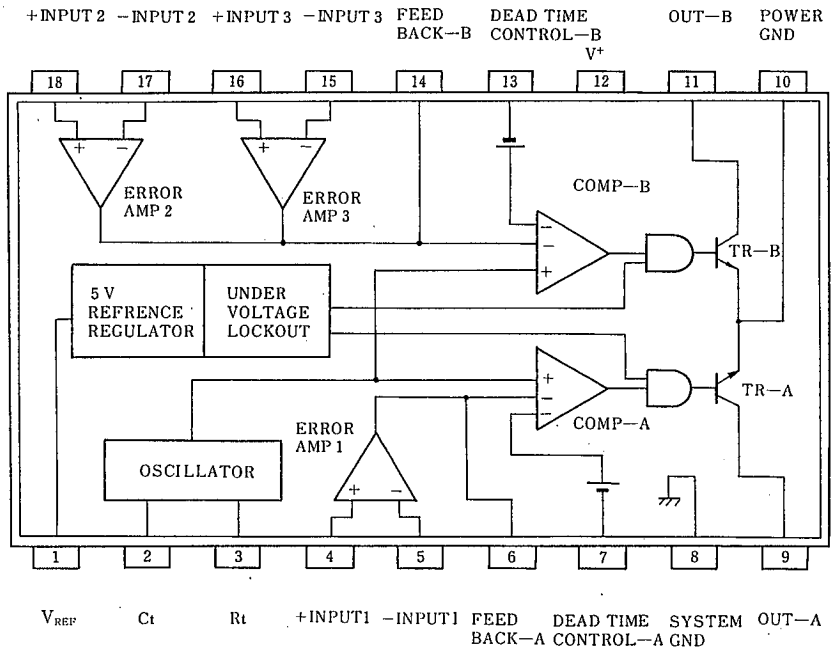


NJM2355D

■ FEATURES

- Operating Voltage (7.5V～50V)
- Complete PWM Power Control Circuit
- Uncommitted Outputs fov 200-mA Sink or Source
- Output control Selects Single-Ended or Pull Operation
- Internal Cicuitry Prohibits Double Pulse at Either Output
- Variable Dead-Time Provides Control Over Total Range
- Package Outline DIP18
- Bipolar Technology

■ BLOCK DIAGRAM & PIN CONFIGURATION



NJM2355D

■ ABSOLUTE MAXIMUM RATINGS

(Ta=25℃)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V^+	50	V
Output Current 1	I_{O1}	200	mA
Output Current 2	I_{O2}	200	mA
Power Dissipation	P_D	700	mW
Operating Temperature Range	T_{opr}	−20~+75	℃
Storage Temperature Range	T_{stg}	−40~+125	℃

■ ELECTRICAL CHARACTERISTICS

(Ta=25℃, V^+=15V)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Current (1)	I_{CC} (1)	V^+=15V	—	5.7	7.5	mA
Operating Current (2)	I_{CC} (2)	V^+=50V	—	5.9	8.0	mA

< Reference Section >

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Voltage	V_{REF}	I_{REF}=0mA	4.8	5.0	5.2	V
Line Regulation	REGin	V^+=7.5V~50V, I_{REF}=0mA	—	12	35	mV
Load Regulation	REG1	I_{REF}=0mA~10mA	—	6	15	mV
Output Short Current			—	30	—	mA
Output disable Voltage	V_{nop}	OUT=High Level	—	4.3	4.6	V
Output disable hysterisis Voltage	ΔV_{nop}		—	0.3	—	V

< Oscillator Section >

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Frequency	F_O	C_t=0.01μF, R_t=4.3kΩ	25	28	31	kHz

6

< Dead Interval Adjustment Section >

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.		UNIT
Input Bias Current	Ibdt	DT=0V	—	—	−10	μA
Maximum Duty (On-time)	ΔTon/T	C_t=0.01μF, R_t=4.3kΩ	90	—	—	%
Input Threshold Voltage	V_{th}	Duty Cycle: 0%	2.0	2.5	3.0	V

< PWM Comparator Section >

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Threshold Voltage	V_{thc}	Duty Cycle: 0%	—	—	4.5	V

■ ELECTRICAL CHARACTERISTICS

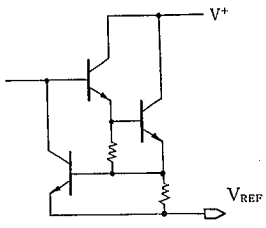
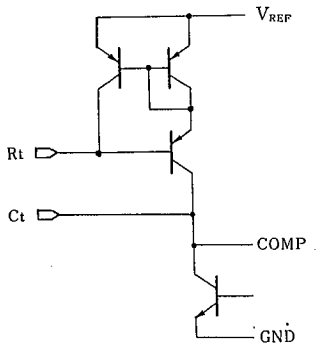
<Error Amplifer Section> (V^+=15V, Ta=25℃)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V_{IO}	FB=2.5V	—	1	10	mV
Input Offset Current	I_{IO}	FB=2.5V	—	5	250	nA
Input Bias Current	I_B	FB=2.5V	—	0.05	1	μA
Common Mode Input Voltage Range	V_{ICM}	V^+=7.5V~50V	0	—	V_{CC}-2	V
Voltage Gain	A_V	FB=0.5V~3.5V	70	100	—	dB
Band Width	f_t	AV=1	—	800	—	kHz
Common Mode Rejection Ratio	CMR	V_{CC}=50V	65	80	—	dB
Output Sink Current	I_{SINK}	V_{ID}=5V, FB=0.7V	0.2	0.4	—	mA
Output Source Current	I_{SOURCE}	V_{ID}=5V, FB=3.5V	−1	−2.5	—	mA

< Output Section >

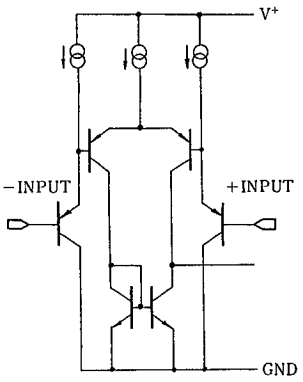
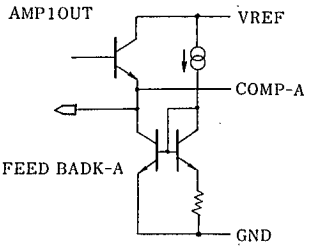
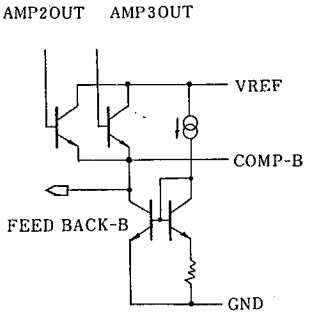
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Leak Current	I_{CER}	V_{CE}=50V	—	—	100	μA
Saturation Voltage	V_{SAT}	I_O=100mA	—	0.9	1.3	V

■ TERMINAL EXPLANATION

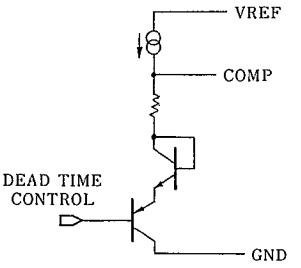
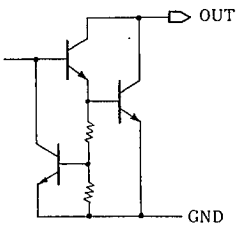
PIN NO.	PIN SYMBOL	FUNCTION	EQUIVALENT CIRCUIT
1.	V_{REF}	5V Reference Voltage Output	
2.	Ct	The oscillator frequency is decided by putting Capacitor, Ct.	
3.	Rt	The oscillator frequency is decided by putting resistor, Rt.	

6

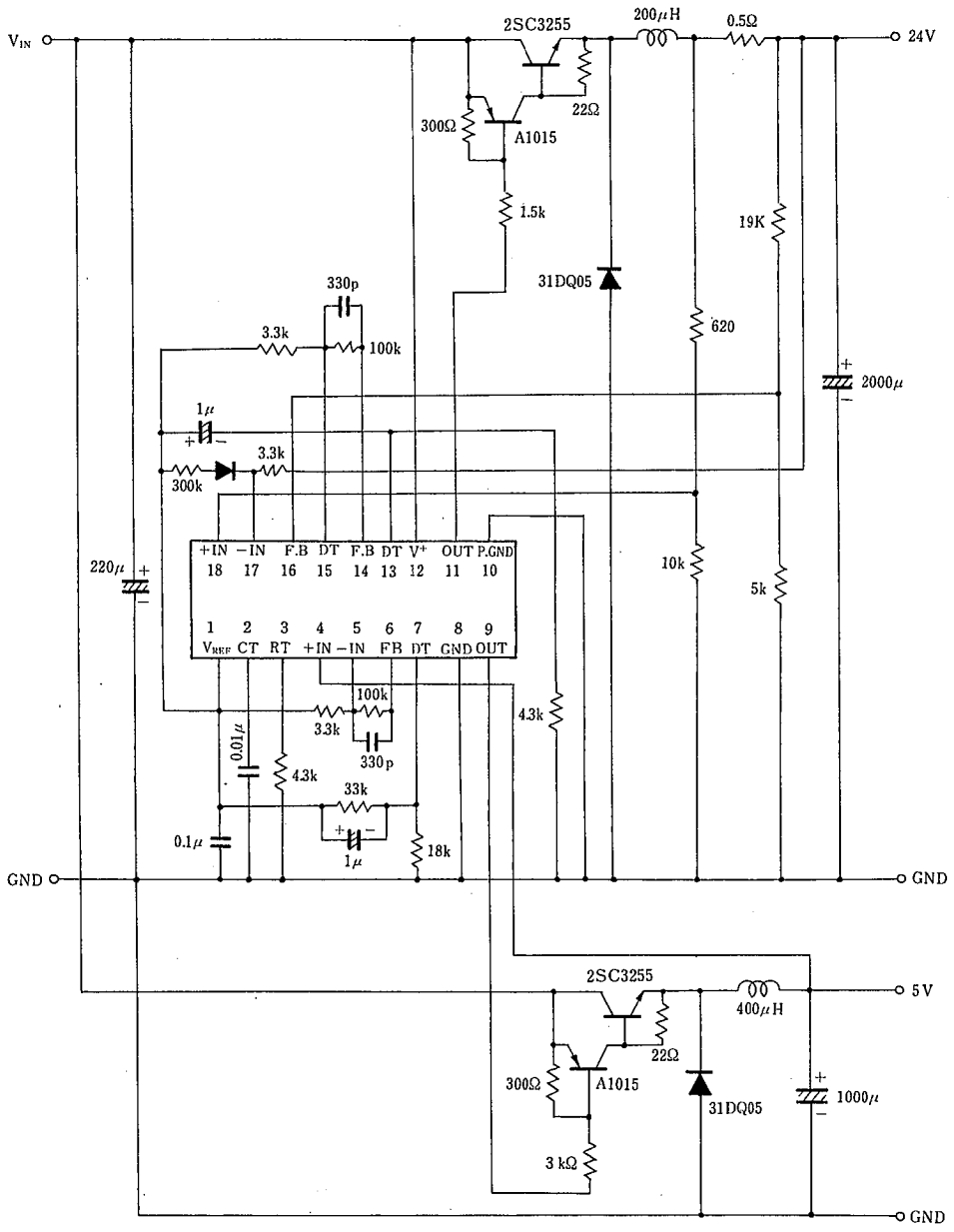
■ TERMINAL EXPLANATION

PIN NO.	PIN SYMBOL	FUNCTION	EQUIVALENT CIRCUIT
4. 5. 16. 15. 18. 17.	+INPUT1 −INPUT1 +INPUT3 −INPUT3 +INPUT2 −INPUT2	+INPUT of Error Amp 1 (A Channel) −INPUT of Error Amp 1 (A Channel) +INPUT of Error Amp 3 (B Channel) −INPUT of Error Amp 3 (B Channel) +INPUT of Error Amp 2 (B Channel) −INPUT of Error Amp 2 (B Channel)	
6.	FEED BACK-A	OUTPUT of Error Amp 1 (A Channel)	
14.	FEED BACK-B	OUTPUT of Error Amp 2 and Error Amp 3 (B Channel)	

■ TERMINAL EXPLANATION

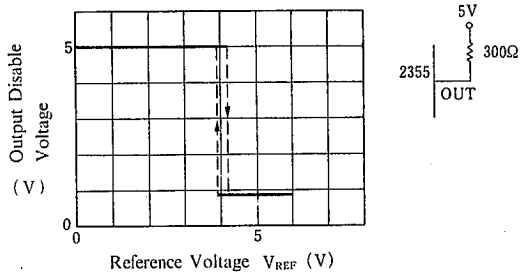
PIN NO.	PIN SYMBOL	FUNCTION	EQUIVALENT CIRCUIT
7. 13.	DEAD TIME CONTROL-A DEAD TIME CONTROL-B	The Dead Time Width is adjustable by terminal voltage adjust. (A Channel) (B-Channel)	
8.	SYSTEM GND	Ground	
9. 11.	OUT-A OUT-B	Internal Switching Transistor: Open Collector (A Channel) (B-Channel)	
10.	POWER GND	Ground Connect to PIN 8.	
12.	V^+	Power Supply	

■ TYPICAL APPLICATION

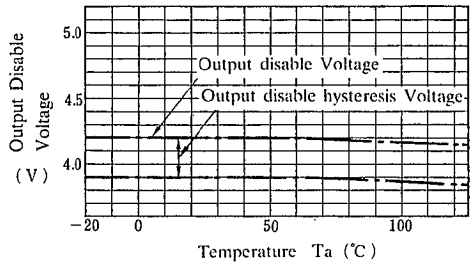


■ TYPICAL CHARACTERISTICS

Output Disable Voltage at Low Input Voltage

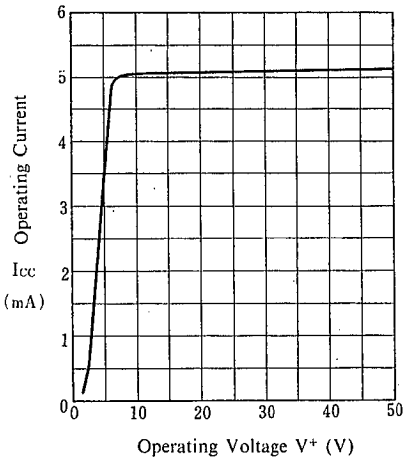


Output Disable Voltage at Low Input Voltage vs. Temperature

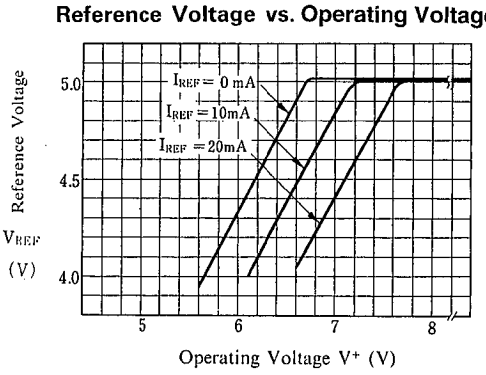


Operating Current vs. Operating Voltage

(I_{REF} = 0 mA)

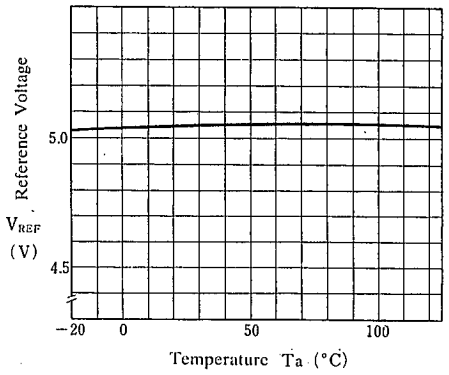


Reference Voltage vs. Operating Voltage

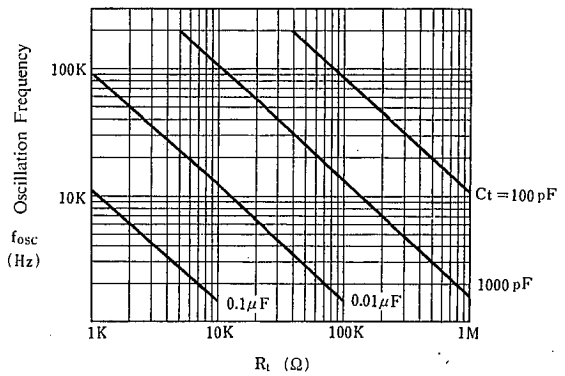


Reference Voltage vs. Temperature

(V_{ct}=15V, I_{REF}=0mA)



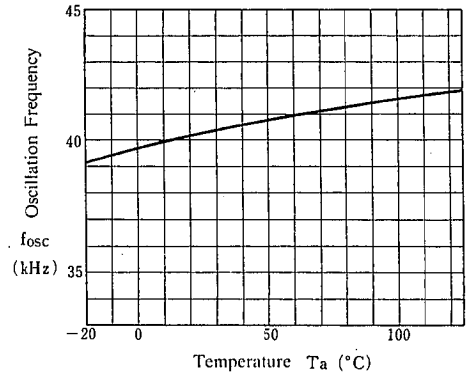
Oscillation Frequency vs. Rt, Ct



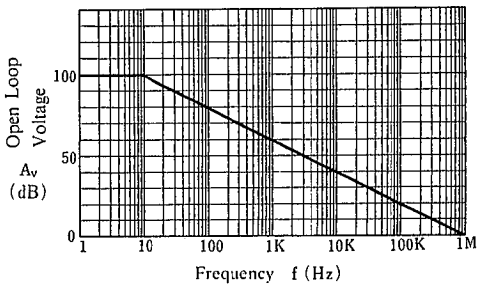
■ TYPICAL CHARACTERISTICS

Oscillation Frequency vs. Temperature

(V^+=15V, C_T=1000pF, R_T=30kΩ)

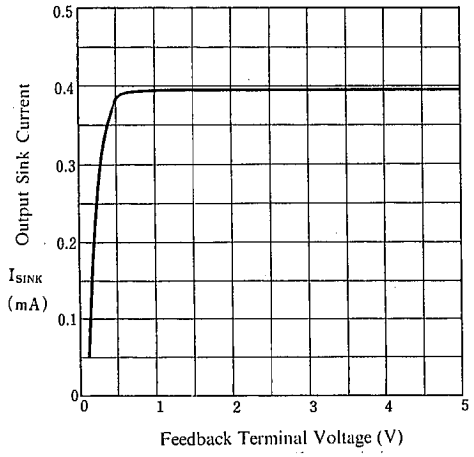


Open Loop Voltage Gain vs. Frequency



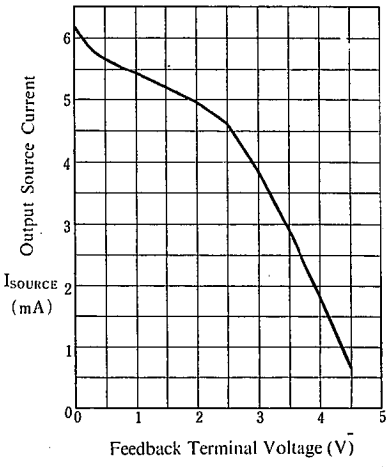
< Error Amplifier Section >
Output Sink Current vs. Feedback Terminal Voltage

(V^+=15V, +INPUT= 0 V, −INPUT= 5 V)



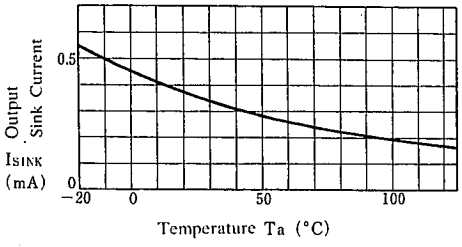
< Error Amplifier Section >
Output Source Current vs. Feedback Terminal Voltage

(V^+=15V, +INPUT= 5 V, −INPUT= 0 V)



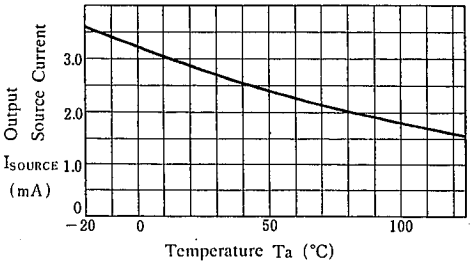
< Error Amplifier Section >
Output Sink Current vs. Temperature

(V^+=15V, F.B_{PIN}=0.1V, +INPUT=0V, −INPUT=5V)



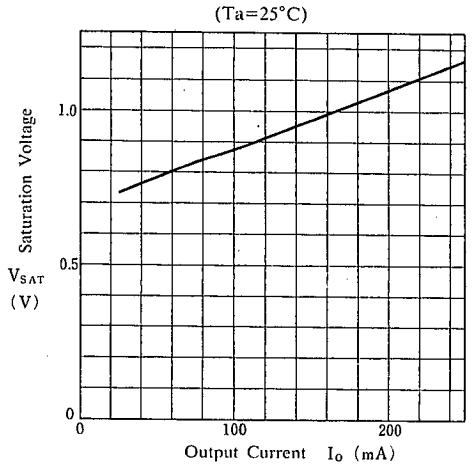
< Error Amplifier Section >
Output Source Current vs. Temperature

(V^+=15V, F.B_{PIN}=3.5V, +INPUT=5V, −INPUT=0V)

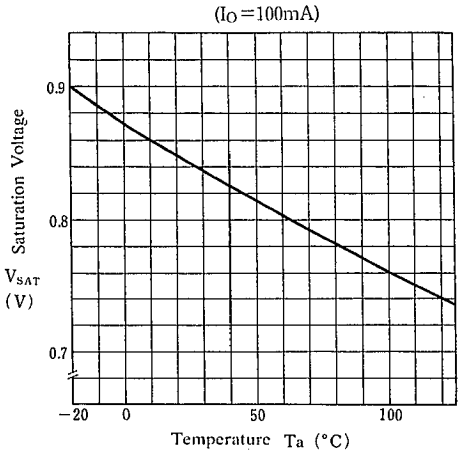


■ TYPICAL CHARACTERISTICS

< Output Section >
Saturation Voltage vs. Output Current



< Output Section >
Saturation Voltage vs. Temperature



MEMO