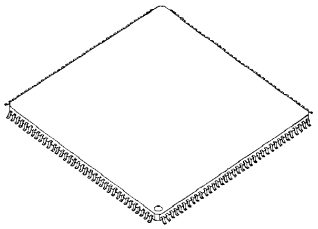
1/2 1/3 1/4 Duty LCD Driver

■ GENERAL DESCRIPTION

NJU6543 is a 1/2 or 1/3,1/4 duty segment type LCD driver. It incorporates 4 common driver circuits and 128 segment driver circuits. **NJU6543** can drive maximum 256 segments in 1/2 duty ratio and maximum 384 segments in 1/3 duty ratio and maximum 512 segments in 1/4 duty ratio.
In addition, the **NJU6543**'s useful functions meet a wide range of applications.

■ PACKAGE OUTLINE



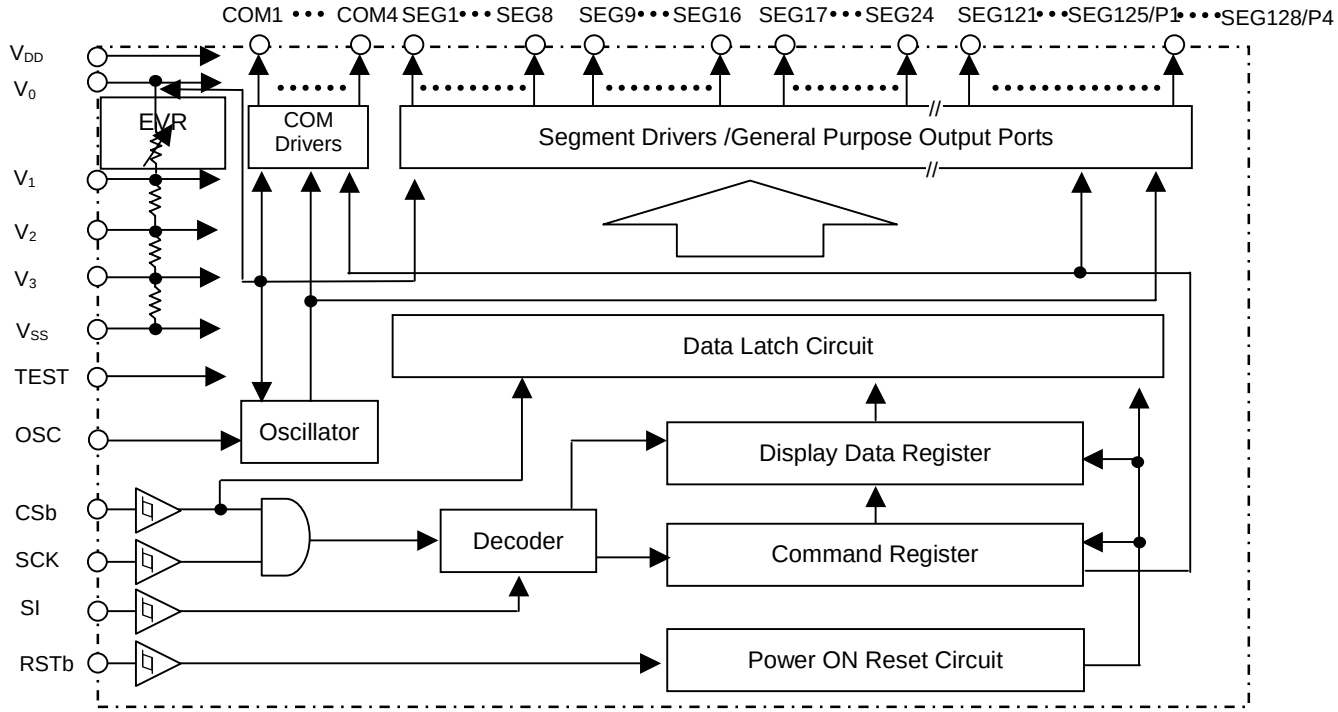
NJU6543

■ FEATURES

- LCD driving circuit :Max. 128outputs (4 outputs as for general purpose ports)
- Programmable Duty Ratio
  1/2 Duty Ratio :Driving max. 256 segments
  1/3 Duty Ratio :Driving max. 384 segments
  1/4 Duty Ratio :Driving max. 512 segments
- Programmable Bias Ratio :1/2, 1/3 bias ratio
- Electrical Variable Resistance :8-steps
- Serial Data Transfer :Shift clock max. 2MHz
- Built-in Oscillator :CR oscillation with external resistor and capacitance, or external oscillation signal input

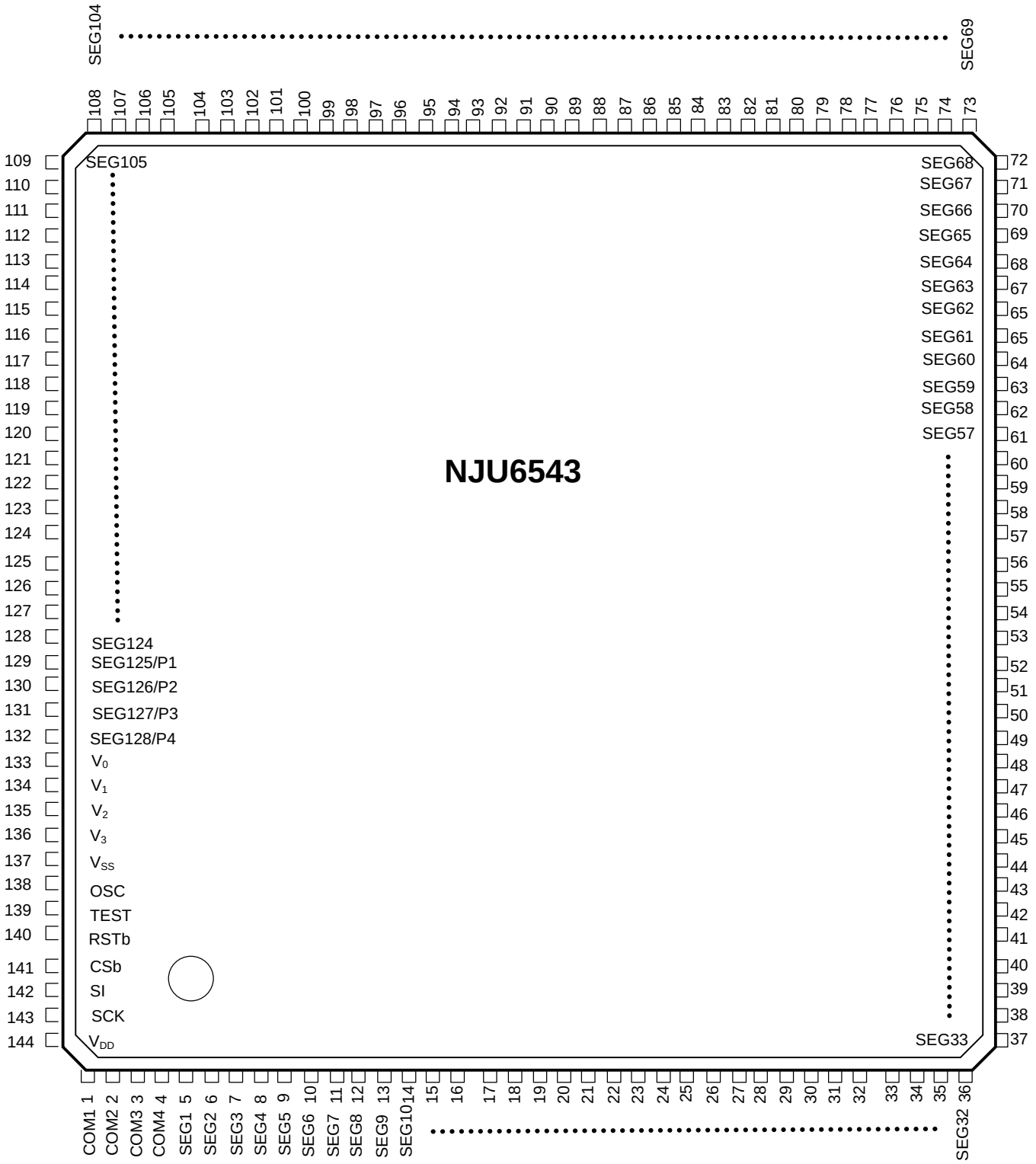
- Operating Voltage :3.0V / 5.0V
- C-MOS Technology :P-Sub
- Package Outline :LQFP144 20mm*20mm t=1.7mm(max) Pin-pitch=0.5mm

■ BLOCK DIAGRAM



■ PIN CONFIGURATION

• LQFP144



■ TERMINAL DISCRIPTION

No.	Pad Name	Function
144	V_{DD}	Power supply: 3V /5V
133	V_0	LCD driving voltage $V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_{SS}$, $V_0 \geq V_{DD}$
134 135 136	V_1 V_2 V_3	Bias At 1/3 bias ratio, keep V_2- V_3 open. At 1/2 bias ratio, short V_2- V_3.
137	V_{SS}	GND V_{SS} =0V
139	TEST	TEST Keep TEST-V_{SS} short
140	RSTb	Reset When RSTb is “L", command register and latch circuit is reset. When this terminal is not used, should be V_{DD} short. (keep power supply condition when hardware reset circuit is used)
141	CSb	Chip select When CSb is "L", data can be read in.
142	SI	Serial data input (8 bit=1word)
143	SCK	Serial clock
138	OSC	External resistor and capacitance connection terminal for CR oscillation, or external clock input terminal
1~4	COM1 ~ COM4	Common driver outputs
5~128	SEG1 ~ SEG124	Segment driver outputs
129~132	SEG125/P1 ~ SEG128/P4	Segment driver outputs/general purpose output ports These 4 terminals can be used as segment outputs or general purpose output ports by setting Command Register. When selected as general purpose ports, data can be outputted via these ports during COM1 timing. According to transferred data, "H"=V_{DD} or "L"=V_{SS} will be outputted.

■ FUNCTION DESCRIPTION

(1) Block Function

- Oscillator
  The oscillator includes an external capacitor and an resistor. It generates clock signal for LCD driving. When use external clock, input the clock signal to OSC.

- Decoder
  Input serial data is decoded and sent to the appropriate block.

- Command Register
  Command data is written to this 8 bits command register to control **NJU6543** operation.

- Display Data Register
  Data is written to this 8 bits register as display data.

- Latch Circuit
  Data stored in display data register is assigned to the corresponding SEG/port.

- Segment Driver/General Purpose Ports
  Basing on display data, segment drivers output LCD SEG driving signal.
  And, SEG125/P1 ~ SEG128/P4 terminals can be selected as segment driver output or general-purpose ports by instruction.

- Common Driver
  Common drivers output LCD COM driving signal.

- Power On Reset
  When power is on, **NJU6543** is automatically initialized. And if RSTb="L", **NJU6543** is reset too.

- Electrical Variable Resistance (E.V.R.)
  The Electrical Variable Resistance adjusts LCD Driving Voltage from V1 to V3.

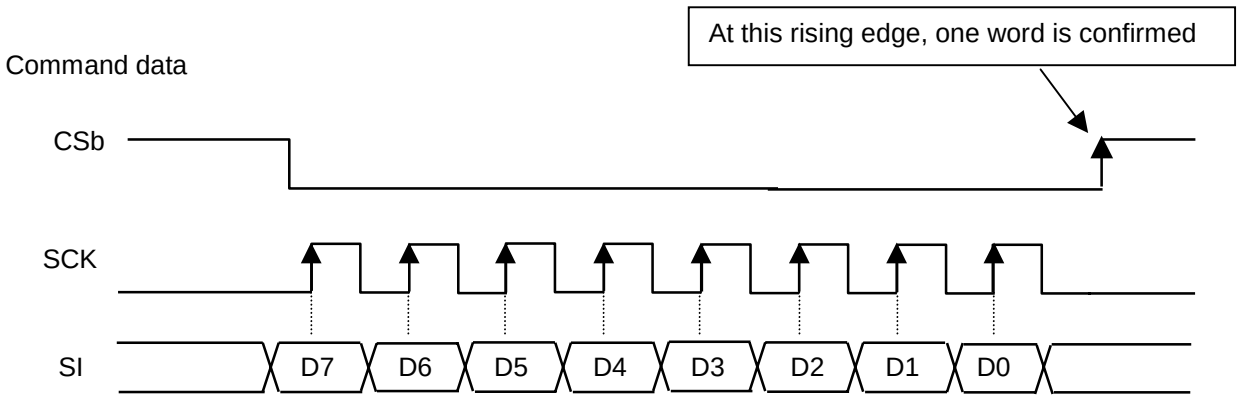
(2) Serial Data Transfer

The transfer of an 8-bit/word serial data is conducted by synchronizing clock via interface with CPU. During CSb="L", serial data is obtainable and will be read in at the rising edge of SCK signal.

After CSb becoming low, by the first word, address data is distinguished by D7 and D6.
In the case of address data(D7,D6="0,1"), the 2nd data can be transferred continually and interrupted as display data even if CSb maintained low. In this case, every 8-bits data will be confirmed as a word either by the falling edge of the8th SCK clock or by the rising edge of the CSb clock.

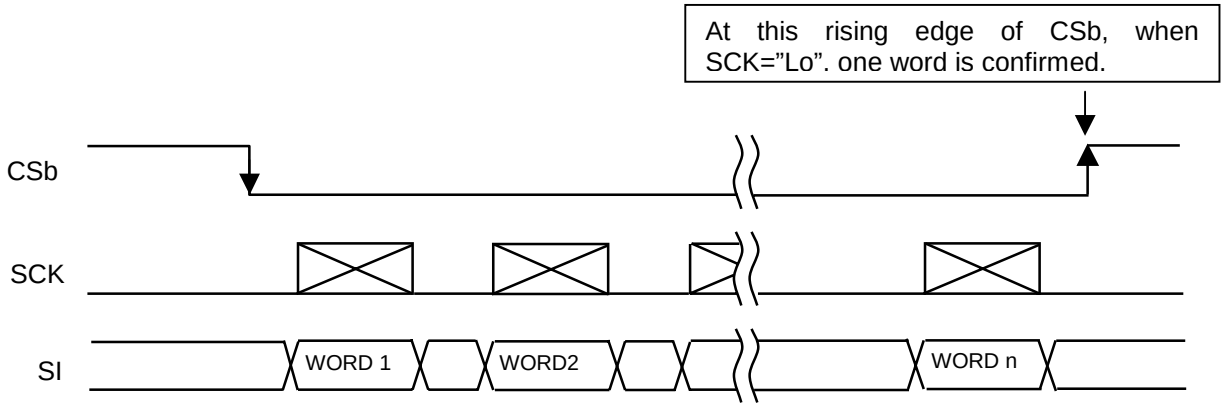
After CSb becoming low, if the first word is command data(D7,D6="1,0"or "1,1"), the after data is invalid even though transfer can be continued without changing the polarity of CSb.(Effective the first word)

At the falling edge of CSb, SCK can be either "H" or "L", but, at the rising edge of CSb, SCK must be low.



Timing of Serial Data Transfer

SCK and SI (Address data and display data)



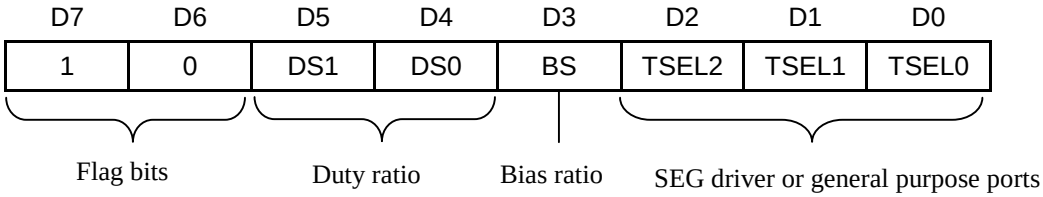
Serial Interface Format

(3) Command Register1

Command Register1 is used to set the duty ratio, the bias ratio, and the SEG driver/general purpose ports. When the D7 to D6 bits of the 1st word are (1,0), the D5 ~ D0 bits are recognized as command data.
The contents of Command Register will be initialized as following when applying Power On Reset or Reset.

The Default Value of Command Register

- Duty ratio : 1/4
- Bias ratio : 1/3
- SEG driver/General purpose ports : SEG drivers(SEG125,SEG126, SEG127, SEG128)



- Duty ratio

DS1	DS0	Duty ratio
0	0	1/4
0	1	1/3
1	0	1/2

*) Do not change the duty ratio during display ON.
**) If DS1 and DS0 are set as (1, 1), it set as the same 1/4Duty as (0, 0).

- Bias ratio

BS	Bias ratio
0	1/3
1	1/2

- SEG driver or general purpose ports

TSEL2	TSEL1	TSEL0	SEG125/P1	SEG126/P2	SEG127/P3	SEG128/P4
0	0	0	SEG125	SEG126	SEG127	SEG128
0	0	1	SEG125	SEG126	SEG127	P4
0	1	0	SEG125	SEG126	P3	P4
0	1	1	SEG125	P2	P3	P4
1	0	0	P1	P2	P3	P4

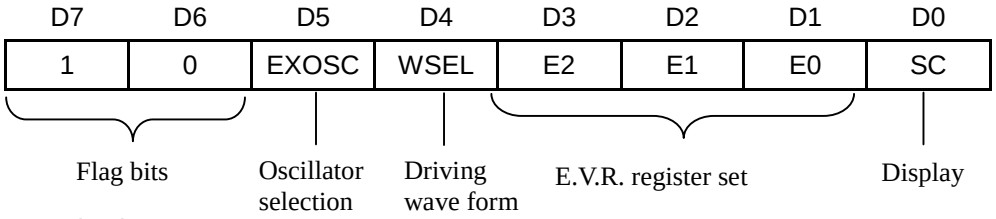
***) If TSEL2 ~ TSEL0 is set to (1, 0, 1), (1, 1, 0), (1, 1, 1) all outputs are used as segment drivers.

(4) Command Register2

- Command Register2 is used to set the oscillator, driving waveform, and E.V.R. resister set. When the D7 to D6 bits of the 1st word are (1,1), the D5 ~ D0 bits are recognized as command data.
  The contents of Command Register will be initialized as following when applying Power On Reset or Reset.

The Default Value of Command Register

- Oscillator selection : External resistor and capacitor
- Driving waveform : A(Time sharing system frequency) waveform
- E.V.R. Register Set : V0(0,0,0)
- Display :OFF



- Oscillator selection

EXOSC	Oscillator circuit
0	External resistor and capacitor
1	External oscillation signal input

- Driving waveform

WSEL	Driving waveform
0	A(Time sharing system frequency) waveform
1	B(Flame reversal) waveform

Driving waveform is chosen according to the characteristic of a panel.

- E.V.R. resister set

E.V.R. resistor set instruction adjusts the contrast of the LCD, by 3-bits selects(E2,E1,E0).
One LCD driving voltage VLCD out of 8 voltage-stages by setting E.V.R. register.
Set the binary code “000” when contrast adjustment is unused.

E2	E1	E0	V1		V_{LCD} (V_0~V_{SS})
			1/2bias	1/3bias	
0	0	0	V_0	V_0	High
0	0	1	$0.933V_0$	$0.955V_0$	:
0	1	0	$0.875V_0$	$0.913V_0$	:
0	1	1	$0.824V_0$	$0.875V_0$	:
1	0	0	$0.778V_0$	$0.840V_0$	:
1	0	1	$0.737V_0$	$0.808V_0$	:
1	1	0	$0.700V_0$	$0.778V_0$	:
1	1	1	$0.667V_0$	$0.750V_0$	Low

- Display ON/OFF

SC	Display ON/OFF
0	OFF
1	ON

When Display OFF

- All segment and common terminal output V_{SS}
  (When general purpose output ports are selected, even Display OFF, these ports can output data)
- Suspending Oscillation (but, if RSTb="L", oscillator works)
- V_1 , V_2 and V_3 become “H” (no current pass through the bleeder resistors)

Even during Display OFF, interface can be accessed, and data can be written into the command register, address counter and data register.

(5) Output Address Counter

Output Address Counter will specify the addresses of the SEG and COM drivers for the display data.
When the MSB (D7 to D6) of the 1st data is “01”, the LSB 6 bits (D5 to D0) specify the addresses of COM and SEG drivers, and the 2nd data is the display data which will be sent to the 1st-data-specified drivers. At the same time, SEG and COM driver addresses will be increased automatically shown in **Table 1**. In other words, as of the SEG and COM driver addresses specified by the first data in the Output Address Counter, display data can be transferred to the SEG and COM drivers without further address setting.
The address setting range is from "000000" to "111111". if the data transferred additionally , then it will be reset to “000000” and renew the auto-increment operation.

- Address Data

D7	D6	D5	D4	D3	D2	D1	D0
0	1	C1	C0	S3	S2	S1	S0
Flag bits		COM driver Address		SEG driver Address			

Table 1. The Relationship Between Output Address and SEG/COM Drivers

C1	C0	S3	S2	S1	S0	COM Driver	SEG Driver							
							D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	COM1	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8
		0	0	0	1		SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16
		0	0	1	0		SEG17	SEG18	SEG19	SEG20	SEG21	SEG22	SEG23	SEG24
		0	0	1	1		SEG25	SEG26	SEG27	SEG28	SEG29	SEG30	SEG31	SEG32
		0	1	0	0		SEG33	SEG34	SEG35	SEG36	SEG37	SEG38	SEG39	SEG40
		0	1	0	1		SEG41	SEG42	SEG43	SEG44	SEG45	SEG46	SEG47	SEG48
		0	1	1	0		SEG49	SEG50	SEG51	SEG52	SEG53	SEG54	SEG55	SEG56
		0	1	1	1		SEG57	SEG58	SEG59	SEG60	SEG61	SEG62	SEG63	SEG64
		1	0	0	0		SEG65	SEG66	SEG67	SEG68	SEG69	SEG70	SEG71	SEG72
		1	0	0	1		SEG73	SEG74	SEG75	SEG76	SEG77	SEG78	SEG79	SEG80
		1	0	1	0		SEG81	SEG82	SEG83	SEG84	SEG85	SEG86	SEG87	SEG88
		1	0	1	1		SEG89	SEG90	SEG91	SEG92	SEG93	SEG94	SEG95	SEG96
		1	1	0	0		SEG97	SEG98	SEG99	SEG100	SEG101	SEG102	SEG103	SEG104
		1	1	0	1		SEG105	SEG106	SEG107	SEG108	SEG109	SEG110	SEG111	SEG112
		1	1	1	0		SEG113	SEG114	SEG115	SEG116	SEG117	SEG118	SEG119	SEG120
		1	1	1	1		SEG121	SEG122	SEG123	SEG124	SEG125	SEG126	SEG127	SEG128
0	1	0	0	0	0	COM2	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8
		0	0	0	1		SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16
		0	0	1	0		SEG17	SEG18	SEG19	SEG20	SEG21	SEG22	SEG23	SEG24
		0	0	1	1		SEG25	SEG26	SEG27	SEG28	SEG29	SEG30	SEG31	SEG32
		0	1	0	0		SEG33	SEG34	SEG35	SEG36	SEG37	SEG38	SEG39	SEG40
		0	1	0	1		SEG41	SEG42	SEG43	SEG44	SEG45	SEG46	SEG47	SEG48
		0	1	1	0		SEG49	SEG50	SEG51	SEG52	SEG53	SEG54	SEG55	SEG56
		0	1	1	1		SEG57	SEG58	SEG59	SEG60	SEG61	SEG62	SEG63	SEG64
		1	0	0	0		SEG65	SEG66	SEG67	SEG68	SEG69	SEG70	SEG71	SEG72
		1	0	0	1		SEG73	SEG74	SEG75	SEG76	SEG77	SEG78	SEG79	SEG80
		1	0	1	0		SEG81	SEG82	SEG83	SEG84	SEG85	SEG86	SEG87	SEG88
		1	0	1	1		SEG89	SEG90	SEG91	SEG92	SEG93	SEG94	SEG95	SEG96
		1	1	0	0		SEG97	SEG98	SEG99	SEG100	SEG101	SEG102	SEG103	SEG104
		1	1	0	1		SEG105	SEG106	SEG107	SEG108	SEG109	SEG110	SEG111	SEG112
		1	1	1	0		SEG113	SEG114	SEG115	SEG116	SEG117	SEG118	SEG119	SEG120
		1	1	1	1		SEG121	SEG122	SEG123	SEG124	SEG125	SEG126	SEG127	SEG128
1	0	0	0	0	0	COM3	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8
		0	0	0	1		SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16
		0	0	1	0		SEG17	SEG18	SEG19	SEG20	SEG21	SEG22	SEG23	SEG24
		0	0	1	1		SEG25	SEG26	SEG27	SEG28	SEG29	SEG30	SEG31	SEG32
		0	1	0	0		SEG33	SEG34	SEG35	SEG36	SEG37	SEG38	SEG39	SEG40
		0	1	0	1		SEG41	SEG42	SEG43	SEG44	SEG45	SEG46	SEG47	SEG48
		0	1	1	0		SEG49	SEG50	SEG51	SEG52	SEG53	SEG54	SEG55	SEG56
		0	1	1	1		SEG57	SEG58	SEG59	SEG60	SEG61	SEG62	SEG63	SEG64
		1	0	0	0		SEG65	SEG66	SEG67	SEG68	SEG69	SEG70	SEG71	SEG72
		1	0	0	1		SEG73	SEG74	SEG75	SEG76	SEG77	SEG78	SEG79	SEG80
		1	0	1	0		SEG81	SEG82	SEG83	SEG84	SEG85	SEG86	SEG87	SEG88
		1	0	1	1		SEG89	SEG90	SEG91	SEG92	SEG93	SEG94	SEG95	SEG96
		1	1	0	0		SEG97	SEG98	SEG99	SEG100	SEG101	SEG102	SEG103	SEG104
		1	1	0	1		SEG105	SEG106	SEG107	SEG108	SEG109	SEG110	SEG111	SEG112
		1	1	1	0		SEG113	SEG114	SEG115	SEG116	SEG117	SEG118	SEG119	SEG120
		1	1	1	1		SEG121	SEG122	SEG123	SEG124	SEG125	SEG126	SEG127	SEG128
1	1	0	0	0	0	COM4	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8
		0	0	0	1		SEG9	SEG10	SEG11	SEG12	SEG13	SEG14	SEG15	SEG16
		0	0	1	0		SEG17	SEG18	SEG19	SEG20	SEG21	SEG22	SEG23	SEG24
		0	0	1	1		SEG25	SEG26	SEG27	SEG28	SEG29	SEG30	SEG31	SEG32
		0	1	0	0		SEG33	SEG34	SEG35	SEG36	SEG37	SEG38	SEG39	SEG40
		0	1	0	1		SEG41	SEG42	SEG43	SEG44	SEG45	SEG46	SEG47	SEG48
		0	1	1	0		SEG49	SEG50	SEG51	SEG52	SEG53	SEG54	SEG55	SEG56
		0	1	1	1		SEG57	SEG58	SEG59	SEG60	SEG61	SEG62	SEG63	SEG64
		1	0	0	0		SEG65	SEG66	SEG67	SEG68	SEG69	SEG70	SEG71	SEG72
		1	0	0	1		SEG73	SEG74	SEG75	SEG76	SEG77	SEG78	SEG79	SEG80
		1	0	1	0		SEG81	SEG82	SEG83	SEG84	SEG85	SEG86	SEG87	SEG88
		1	0	1	1		SEG89	SEG90	SEG91	SEG92	SEG93	SEG94	SEG95	SEG96
		1	1	0	0		SEG97	SEG98	SEG99	SEG100	SEG101	SEG102	SEG103	SEG104
		1	1	0	1		SEG105	SEG106	SEG107	SEG108	SEG109	SEG110	SEG111	SEG112
		1	1	1	0		SEG113	SEG114	SEG115	SEG116	SEG117	SEG118	SEG119	SEG120
		1	1	1	1		SEG121	SEG122	SEG123	SEG124	SEG125	SEG126	SEG127	SEG128

Increment Direction

- ✧ If general purpose ports are selected by Command Register, under (C1, C0, S3, S2, S1, S0)=(0, 0, 1, 1, 1, 1), D0 ~ D4 bits are the addresses of (P1, P2, P3,P4) ports which corresponds to (SEG125,SEG126, SEG127, SEG128).
- ✧ When SEG125~SEG128 are set as general purpose output ports, data for SEG125~SEG128 during COM2~COM4 scanning will be ignored.

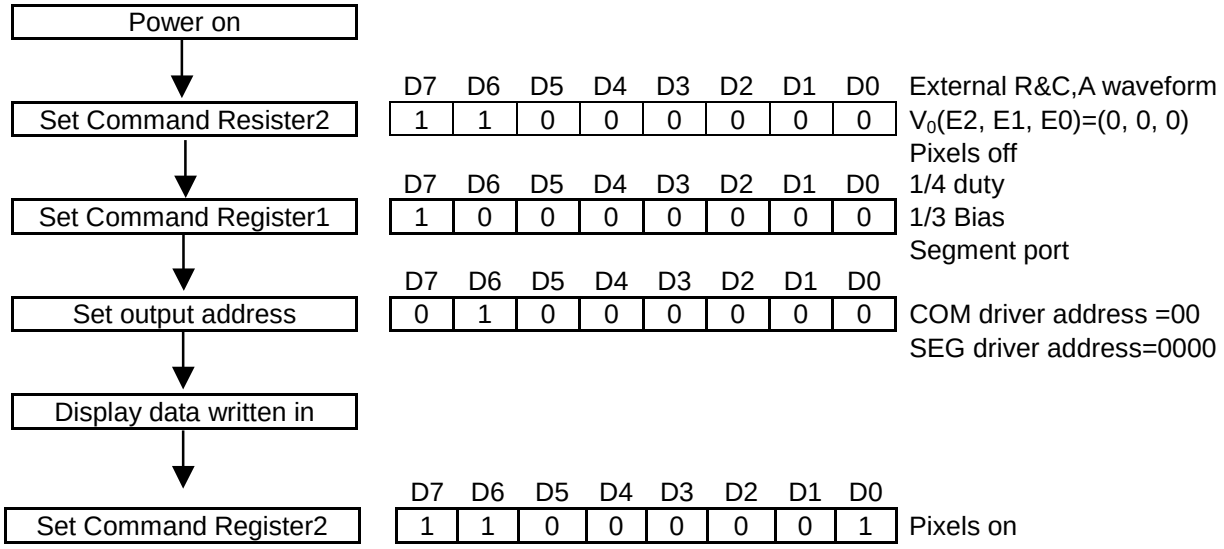
(6) Power ON Reset

After power ON, **NJU6543** is initialized to the following values:

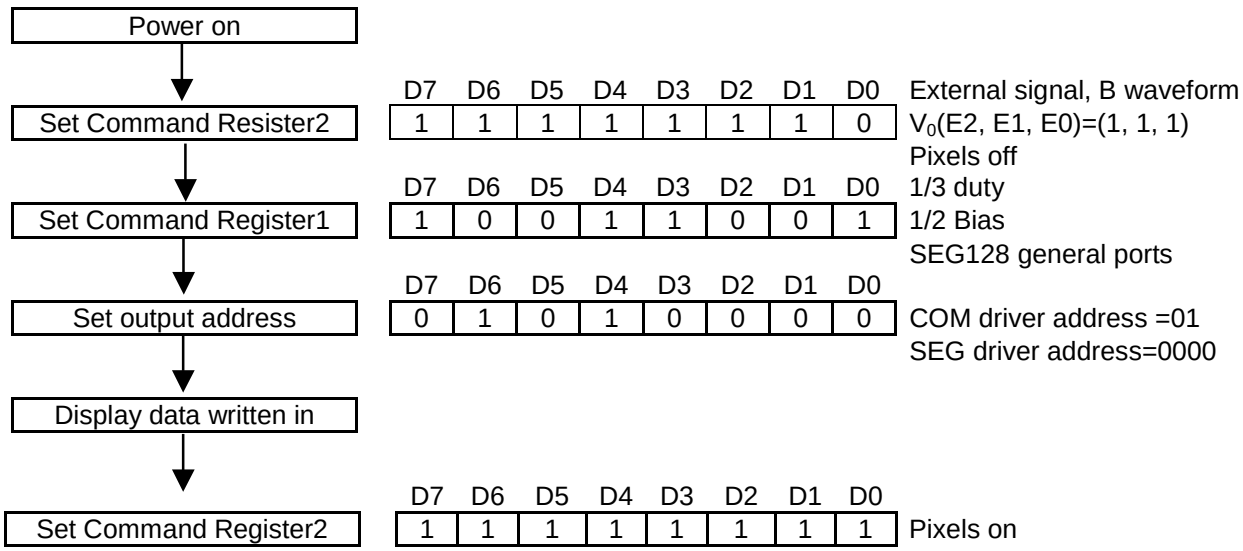
- Address counter (C1, C0, S3, S2, S1, S0)=(0, 0, 0, 0, 0, 0)
- Display data register all "0"
- Duty ratio 1/4 duty
- Bias ratio 1/3 bias
- Oscillator selection External resistor and capacitor
- Driving waveform A waveform
- E.V.R. resister V_0(E2, E1, E0)=(0, 0, 0)
- Segment/General purpose port: Segment output(SEG125,SEG126, SEG127, SEG128)
- Display OFF

(7) Sequence of Initialization

(7-1)1/4 duty,1/3 bias,SEG125 ~ SEG128 used as SEG drivers, external resister and capacitor, A waveform,E.V.R. V_0(E2, E1, E0)=(0, 0, 0) data written in from COM1.



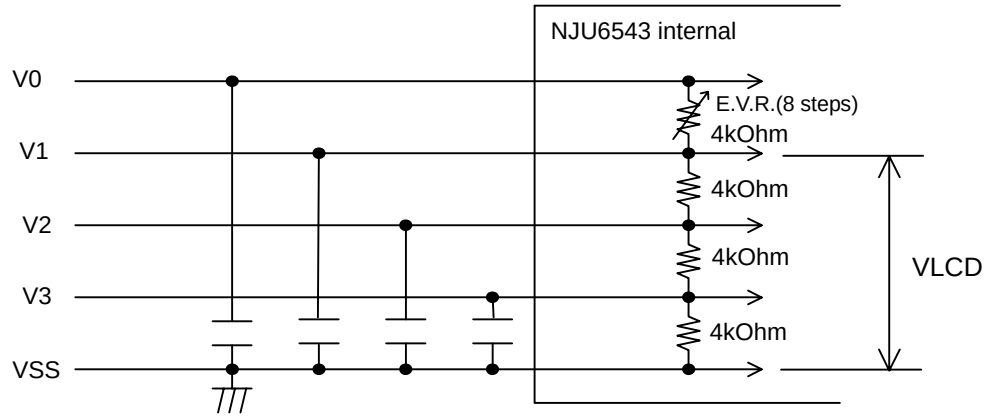
(7-2)1/3 duty,1/2 bias,SEG128 used as general purpose ports, external oscillation signal input, B waveform,E.V.R. V_0(E2, E1, E0)=(1, 1, 1) data written in from COM2.



(8-1) LCD driving voltage generation circuit

LCD driving voltage generation circuit generates LCD driving bias voltages V_1 , V_2 and V_3. It adjusts the voltage by 8 steps electrical volume from V_0 and allots the voltage to V_0, V_1 , V_2 and V_3 by resistor-voltage-dividing as shown in below.

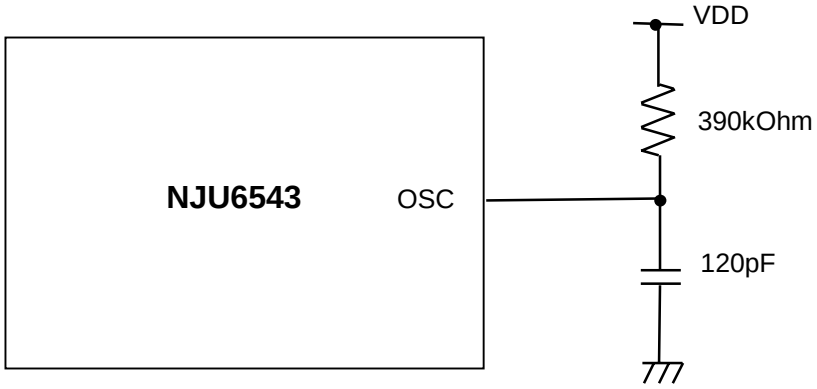
V_0, V_1, V_2 and V_3 terminals requires external capacitors for bias voltage stabilization for display quality. These values of capacitors should be fixed in accordance with evaluation in the application.



When the E.V.R. is not used, V1 terminal should connect to V0.
When the **NJU6543** operates as 1/2 bias operation, V2 terminal should connect to V3.

(8-2) Oscillator circuit

The oscillator consists of an external capacitor and an resistor
It generates clock signal for LCD driving. When use external clock, input the clock signal to OSC.



(f_{OSC}=14.5kHz TYP)

■ ABSOLUTE MAXIMAM RATINGS

(V_{SS}=0V, Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT	CONDITIONS
Supply Voltage 1	V_{DD}	-0.3 ~ +7.0	V	
Supply Voltage 2	V_0	-0.3 ~ +7.0	V	
Supply Voltage 3	V_1, V_2, V_3	-0.3 ~ V_0+0.3	V	
Input Voltage	V_{IN}	-0.3 ~ V_{DD}+0.3	V	INHb, CSb, SCK, SI, RSTb, OSC applicable.
Operating Temp.	Topr	-40 ~ +105	°C	
Storage Temp.	Tstg	-55 ~ +125	°C	
Dissipation Power	P_D	1000	mW	The power dissipation is value mounted on 4 layer glass epoxy board in size 76.2mm x 114.3mm x 1.6tmm

Note-1) Do not exceed the absolute maximum ratings, otherwise the stress may cause a permanent damage to the IC. It is also recommended that the IC be used within the range specified in the DC electrical characteristics, or the electrical stress may cause mulfunctions and impact on the reliability.

Note-2) All voltages are relative to V_{SS} = 0V reference.

Note-3) The following relationship shall be maintained.
$V_0 \geq V_1 \geq V_2 \geq V_3 \geq V_{SS}$, $V_0 \geq V_{DD}$, and V_0 shall be input after V_{DD}.

Note-4) To stabilize the LSI operation, place decoupling capacitors between V_{DD}-V_{SS} and between V_0-V_{SS}.

■ ELECTRICAL CHARACTERISTICS

• DC characteristics 1

(V_{DD}=2.4 to 3.6V, V_{SS}=0V, Ta=-40 to 105°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	Note
Power Supply	V_{DD}		2.4		3.6	V	
LCD Driving Voltage	V_0	$V_0 \geq V_{DD}$	2.4		6.0	V	
LCD Bias Voltage	V_2	Ta=25°C Testing via COM/SEG terminals COM/SEG without load	2/3 V_1-0.2	2/3 V_1	2/3 V_1+0.2	V	
	V_3		1/3 V_1-0.2	1/3 V_1	1/3 V_1+0.2	V	
"H" Level Input Voltage	V_{IH}	CSb, SCK, SI, RESb, OSC	0.8 V_{DD}		V_{DD}	V	
"L" Level Input Voltage	V_{IL}	CSb, SCK, SI, RESb, OSC	0		0.2 V_{DD}	V	
Hysteresis Voltage	V_H	CSb, SCK, SI, RESb		0.2V_{DD}		V	
"H" Level Input Current	I_{IH}	V_{IN}= V_{DD} CSb, SCK, SI, RESb			1.0	µA	
"L" Level Input Current	I_{IL}	V_{IN}= V_{SS} CSb, SCK, SI, RESb			1.0	µA	
"H" Level Output Voltage	V_{OH}	V_{DD} =3V, I_O=5mA, P1 to P4	V_{DD}-0.6			V	
"L" Level Output Voltage	V_{OL}	V_{DD} =3V, I_O=5mA, P1 to P4			0.6	V	
Driver-on Resistance (COM)	R_{COM}	±Id=1µA, V_{LCD}=3V/5.5V	-	-	10	kOhm	5
Driver-on Resistance (SEG)	R_{SEG}	±Id=1µA, V_{LCD}=3V/5.5V	-	-	10	kOhm	5
Oscillating Frequency	f_{OSC}	V_{DD} =3V, R_{OSC}=390kOhm, Cosc=120pF, Ta=25°C	12.6	15.4	18.2	kHz	
External Clock Frequency	f_{CP}	Input into OSC	45	50	55	kHz	
External Clock Duty	duty	Input into OSC	9	12	15	%	
Bleeder Resistor	R_B	V_{LCD}-V_{SS} Ta=25°C	3	4	5	kOhm	
E.V.R	R_{EVR}	V0-V1 Ta=25°C E.V.R.=V0(1,1,1)	3	4	5	kOhm	
Operating Current	I_{DD1}	V_{DD} =3V, Display off Ta=25°C			10	µA	
	I_{DD2}	V_{DD} =3V, V_{LCD}=5V, Ta=25°C, Checker flag display, 1/3 bias Using external R & C, no output			90	µA	
	I_{LCD1}	V_{DD}=3V, V_{LCD}=5V, Display off Ta=25°C			1	µA	
	I_{LCD2}	V_{DD} =3V, V_{LCD}=5V, Ta=25°C, Checker flag display, 1/3 bias no output, E.V.R.=(1,1,1)		320	450	µA	

Note-5) Driver-On resistance (R_{SEG}/R_{COM}) is measured from V_0, V_{SS}, V_1 , V_2 or V_3 terminal to each SEG/COM terminal when Id current flows through COM/SEG terminals.

Note-6) ["H" Level Input Voltage], ["L" Level Input Voltage], [Hysteresis Voltage], ["H" Level Input Current], ["L" Level Input Current], [External Clock Frequency] and [External Clock Duty] are as the same as if V_{DD}=4.5 to 5.5V.

- DC characteristics 2

(V_{DD}=4.5 to 5.5V, V_{SS}=0V, Ta=-40 to 105°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	Note
Power Supply	V_{DD}		4.5		5.5	V	
LCD Driving Voltage	V_{LCD}	$V_0 \geq V_{DD}$	4.5		6.0	V	
LCD Bias Voltage	V_2	Ta=25°C Testing via COM/SEG terminals COM/SEG without load	2/3 V_1-0.2	2/3 V_1	2/3 V_1+0.2	V	
	V_3		1/3 V_1-0.2	1/3 V_1	2/3 V_1+0.2	V	
"H" Level Input Voltage	V_{IH}	CSb, SCK, SI, RESb, OSC	0.8V_{DD}		V_{DD}	V	
"L" Level Input Voltage	V_{IL}	CSb, SCK, SI, RESb, OSC	0		0.2 V_{DD}	V	
Hysteresis Voltage	V_H	CSb, SCK, SI, RESb		0.2V_{DD}		V	
"H" Level Input Current	I_{IH}	V_{IN}= V_{DD} CSb, SCK, SI, RESb			1.0	µA	
"L" Level Input Current	I_{IL}	V_{IN}= V_{SS} CSb, SCK, SI, RESb			1.0	µA	
"H" Level Output Voltage	V_{OH}	V_{DD} =5V, I_O=10mA, P1 to P4	V_{DD}-1.0			V	
"L" Level Output Voltage	V_{OL}	V_{DD} =5V, I_O=10mA, P1 to P4			1.0	V	
Driver-on Resistance (COM)	R_{COM}	±Id=1µA, V_{LCD}=4.5V/5.5V	-	-	10	kOhm	7
Driver-on Resistance (SEG)	R_{SEG}	±Id=1µA, V_{LCD}=4.5V/5.5V	-	-	10	kOhm	7
Oscillating Frequency	f_{OSC}	V_{DD} =3V, R_{OSC}=390kOhm, Cosc=120pF, Ta=25°C	12.6	15.4	18.2	kHz	
External Clock Frequency	f_{CP}	Input into OSC	12.6	15.4	18.2	kHz	
External Clock Duty	duty	Input into OSC	45	50	55	%	
Bleeder Resistor	R_B	V1-V_{SS} Ta=25°C	9	12	15	kOhm	
E.V.R	R_{EVR}	V0-V1 Ta=25°C E.V.R.=V0(1,1,1)	3	4	5	kOhm	
Operating Current	I_{DD1}	V_{DD} =5V, Display off, Ta=25°C			12.5	µA	
	I_{DD2}	V_{DD} =5V, Ta=25°C, Checker flag display, 1/3 bias Using external R & C, no output			130	µA	
	I_{LCD1}	V_{DD} =5V, V_0=5V,Display off, Ta=25°C			1	µA	
	I_{LCD2}	V_{DD} =5V, V0=5V, Ta=25°C, Checker flag display, 1/3 bias Using external R & C, no output E.V.R.=Vo(1,1,1)		320	450	µA	

Note-7) Driver-On resistance (R_{SEG}/R_{COM}) is measured from V_0, V_{SS}, V_1 , V_2 or V_3 terminal to each SEG/COM terminal when Id current flows through COM/SEG terminals.

Note-8) ["H" Level Input Voltage], ["L" Level Input Voltage], [Hysteresis Voltage], ["H" Level Input Current], ["L" Level Input Current], [External Clock Frequency] and [External Clock Duty] are as the same as if V_{DD}=2.4 to 3.6V.

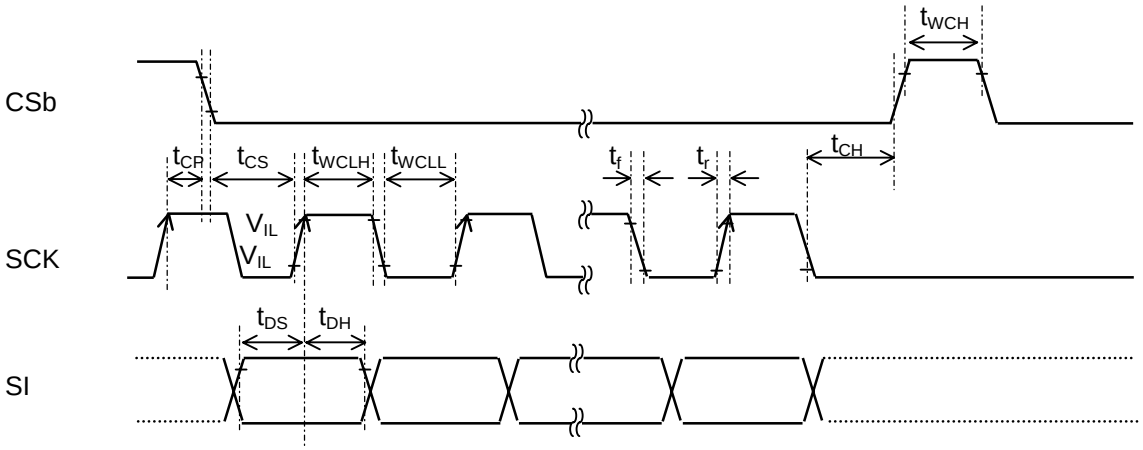
- AC characteristics

(V_{DD}=V_{LCD}=2.4 to 5.5V, V_{SS}=0V, Ta=-40 to 105°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT	Note
"L" Level Clock Pulse Width	t_{WCLL}		230			ns	
"H" Level Clock Pulse Width	t_{WCLH}		230			ns	
Data Setup Time	t_{DS}		20			ns	
Data Hold Time	t_{DH}		20			ns	
CSb Wait Time	t_{CP}		50			ns	9
CSb Setup Time	t_{CS}		180			ns	
CSb Hold Time	t_{CH}		50			ns	
CSb"H" Level Pulse Width	t_{WCH}		50			ns	
Rising Time	t_r				20	ns	
Falling Time	t_f				20	ns	

Note-9) t_{CP} is the time when SCK is kept at “H” during CSb changed from “H” to “L”.

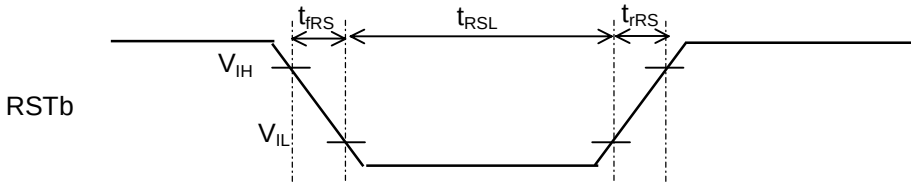
- Input Timing



- Input condition when hardware reset circuit is used

(Ta=25°C)

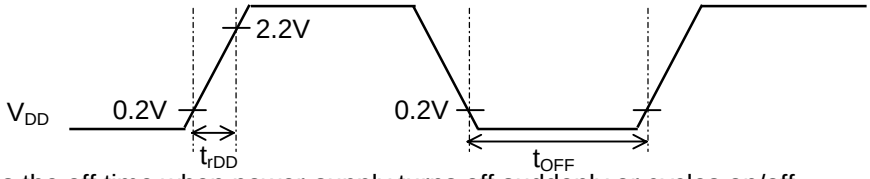
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Reset Input “L” Level Width	t_{RSL}	f_{OSC}= 15.4kHz	1.5			ms
Reset Rising Time	t_{rRS}				100	ns
Reset Falling Time	t_{fRS}				100	ns



- Power supply condition when hardware reset circuit is used

(Ta=-40 to 105°C)

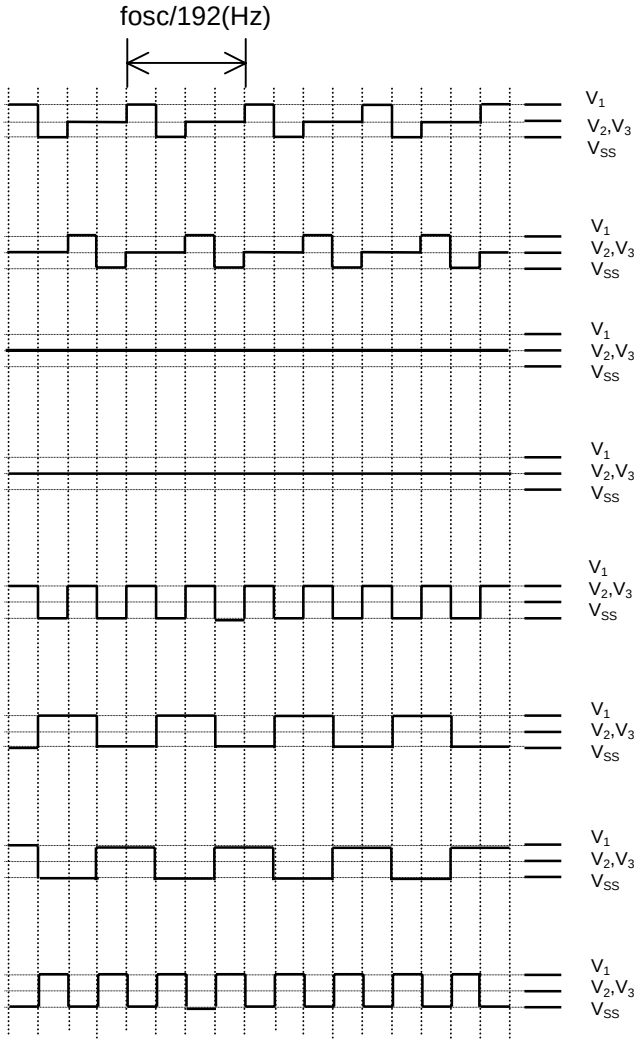
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Power-on Rising Time	t_{rDD}		0.1		5	ms
Power-off Time	t_{OFF}		1			ms



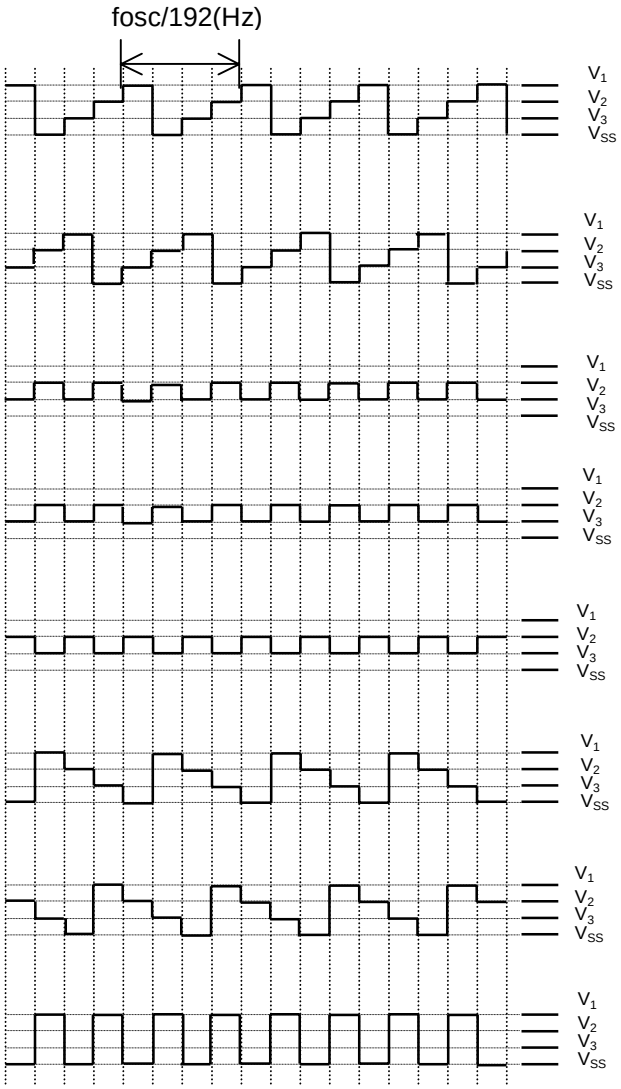
Note 10) t_{OFF} is the off time when power-supply turns off suddenly or cycles on/off.

■ LCD DRIVING WAVEFORM

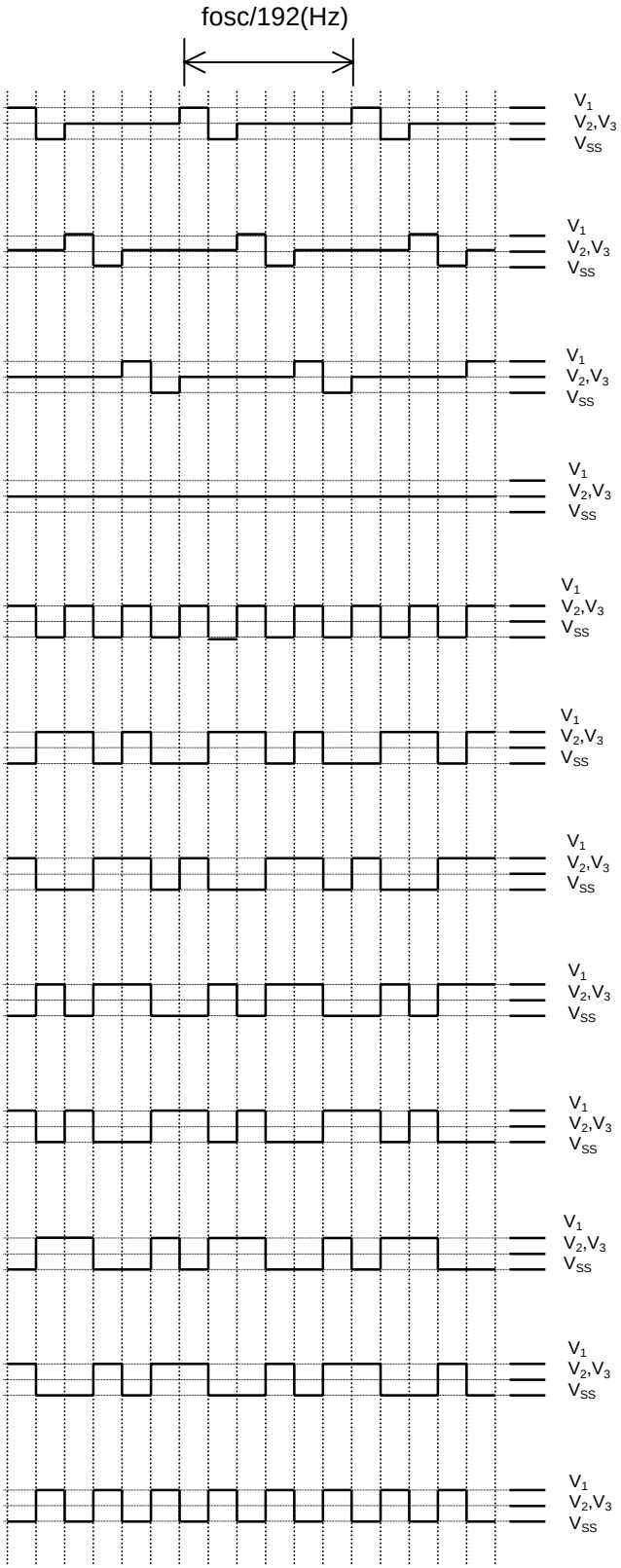
1/2 duty, 1/2 bias, A waveform



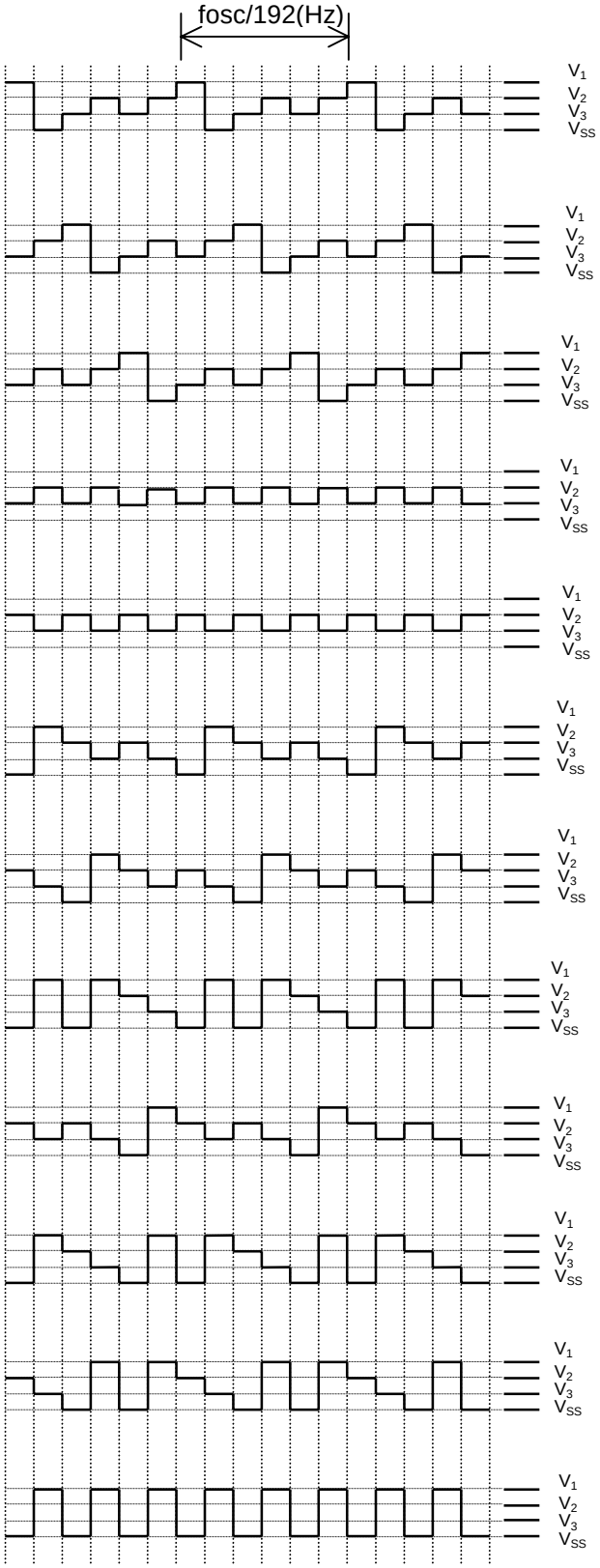
1/2duty, 1/3bias, Awaveform



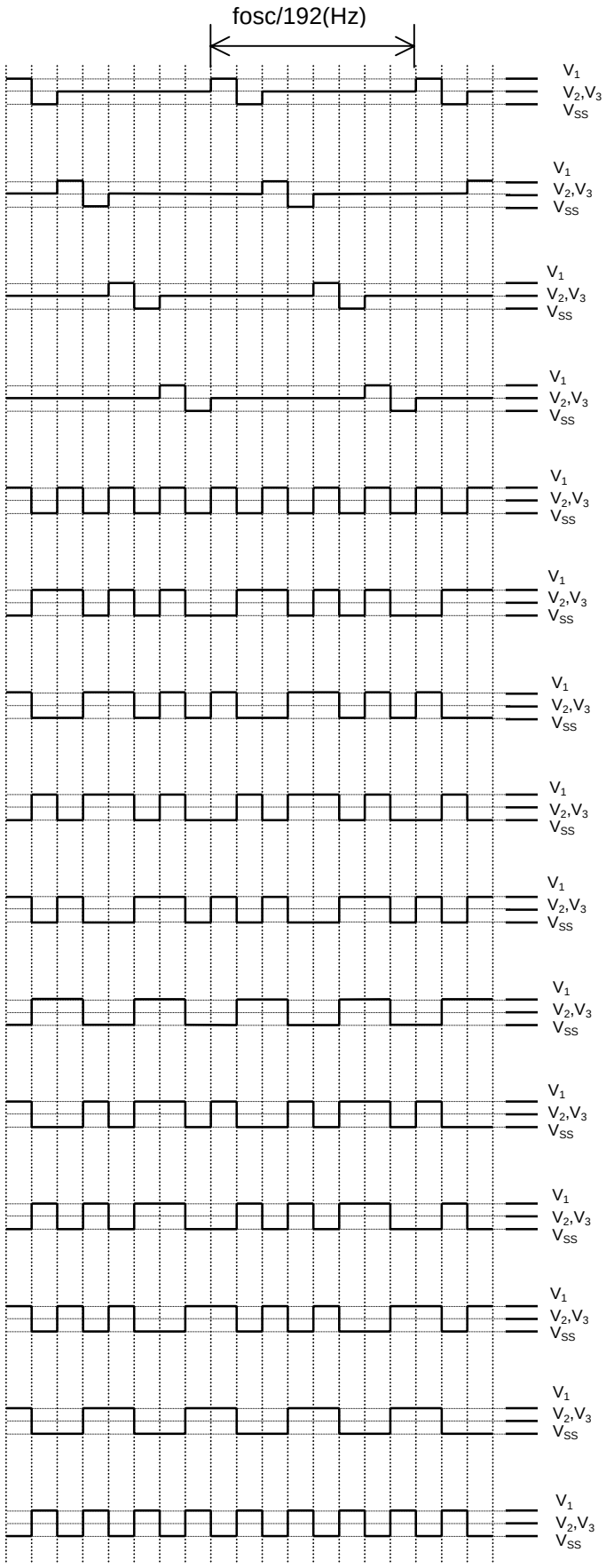
1/3duty, 1/2bias, Awaveform



1/3duty, 1/3bias, Awaveform



1/4duty, 1/2bias, A waveform



"OFF" segment output correspond to COM1, 2, 3 and 4.

"ON" segment output correspond to COM1.

"ON" segment output correspond to COM2.

"ON" segment output correspond to COM1 and 2.

"ON" segment output correspond to COM3.

"ON" segment output correspond to COM1 and 3.

"ON" segment output correspond to COM2 and 3.

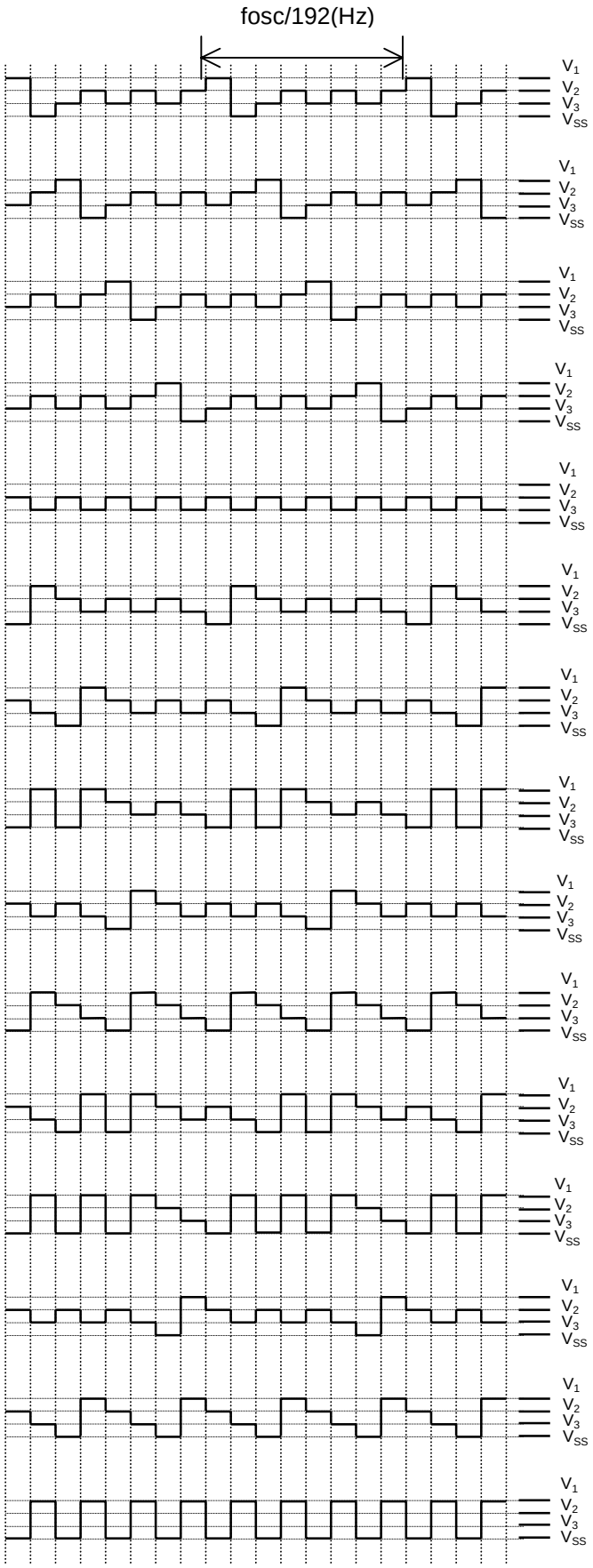
"ON" segment output correspond to COM1, 2 and 3

"ON" segment output correspond to COM4.

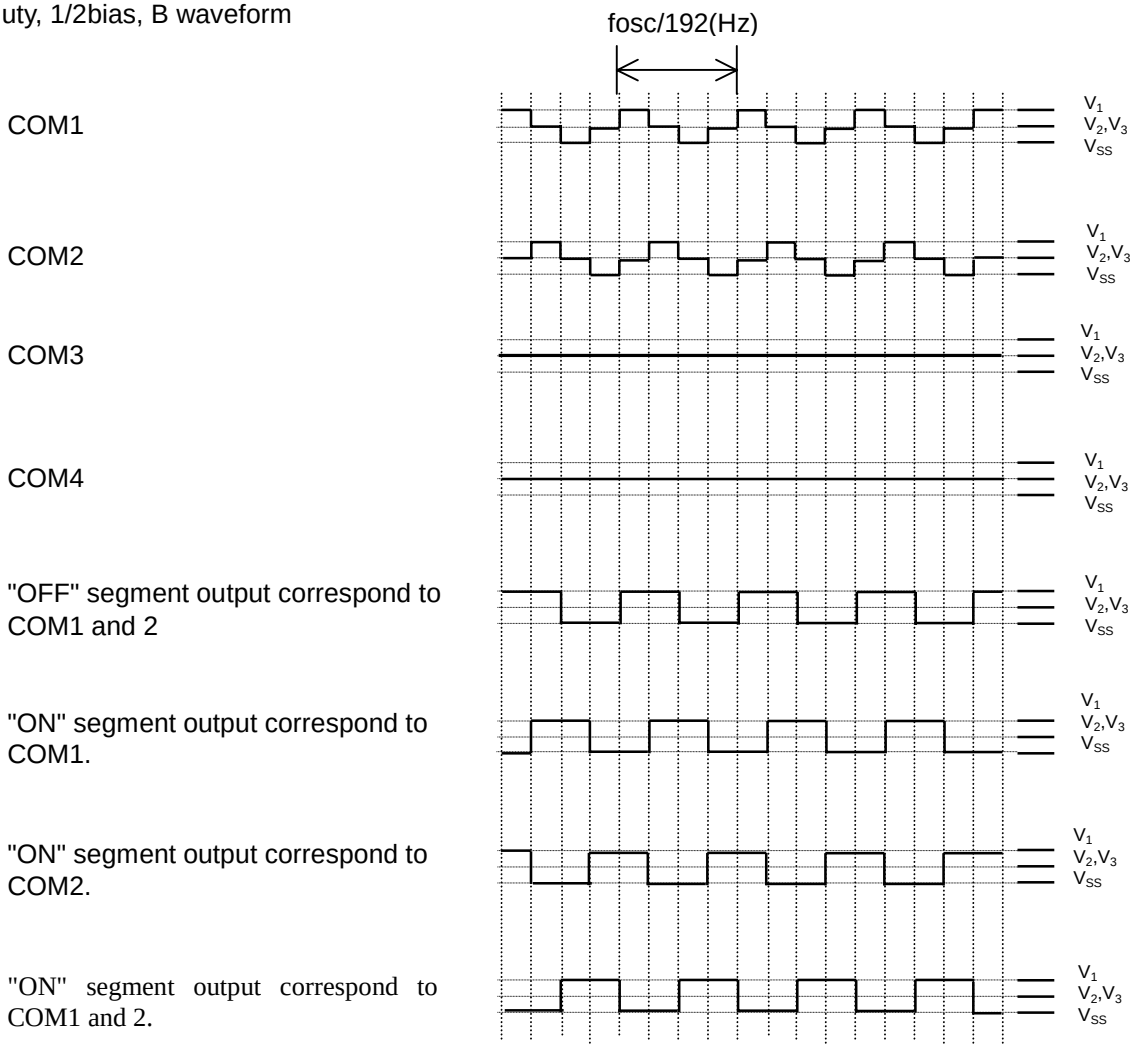
"ON" segment output correspond to COM2 and 4

"ON" segment output correspond to COM1, 2, 3 and 4.

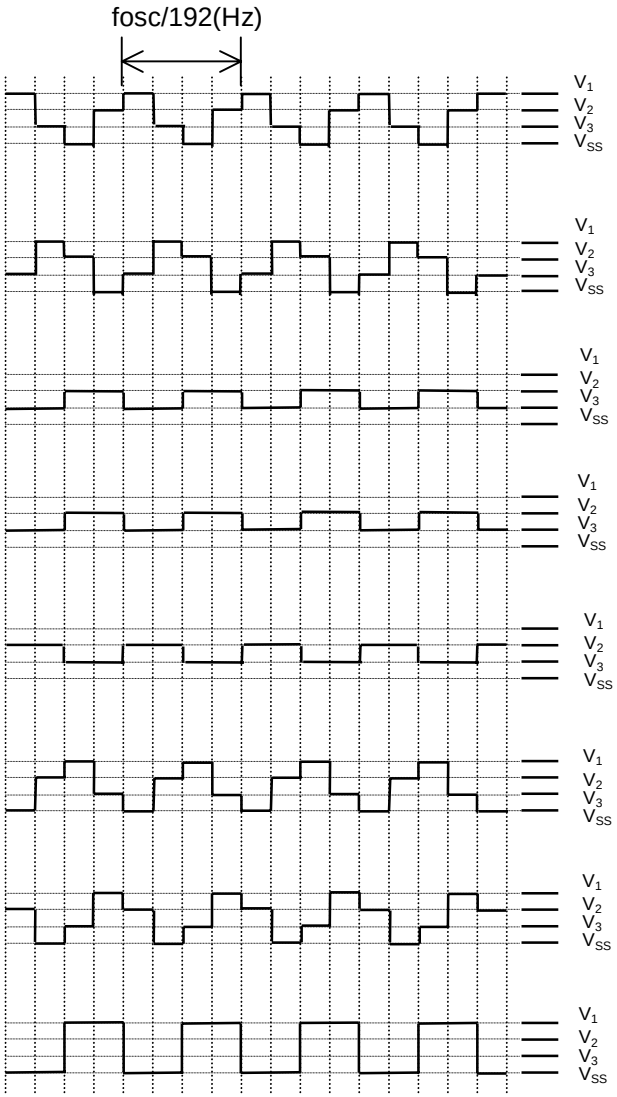
1/4duty, 1/3bias, A waveform



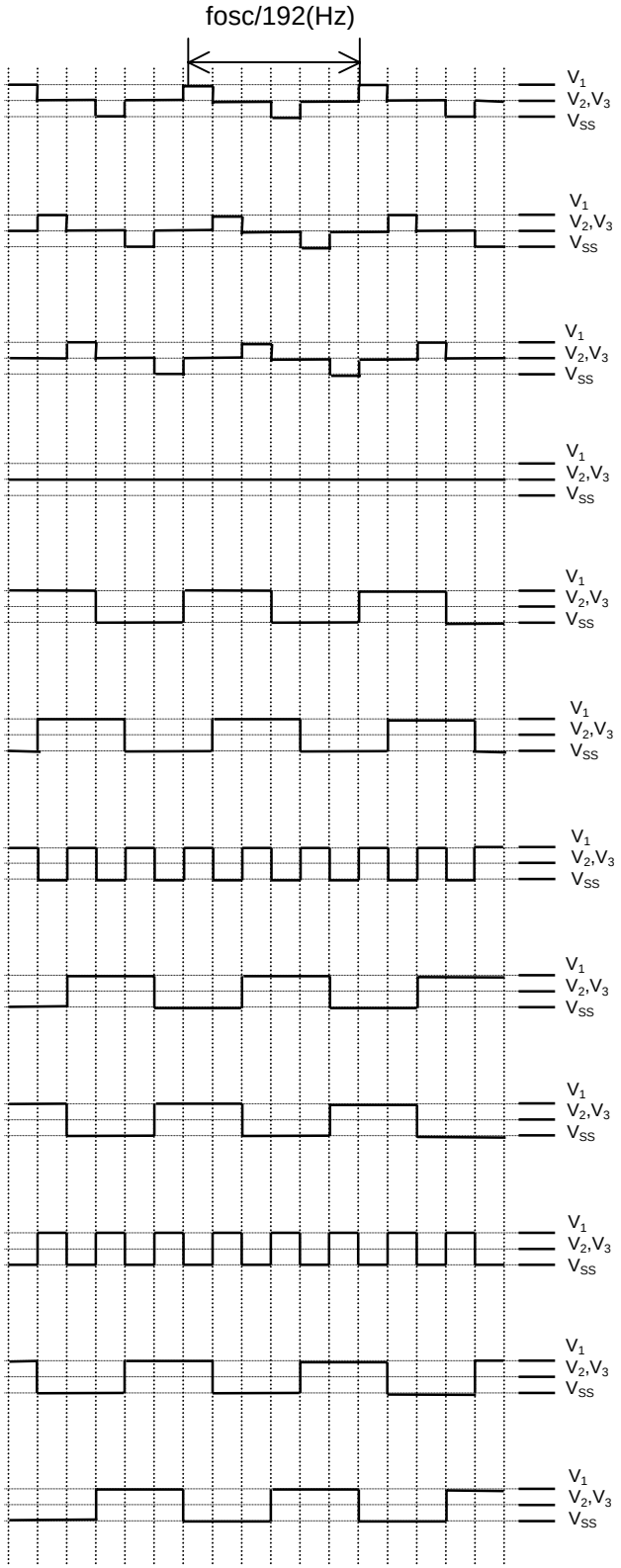
1/2duty, 1/2bias, B waveform



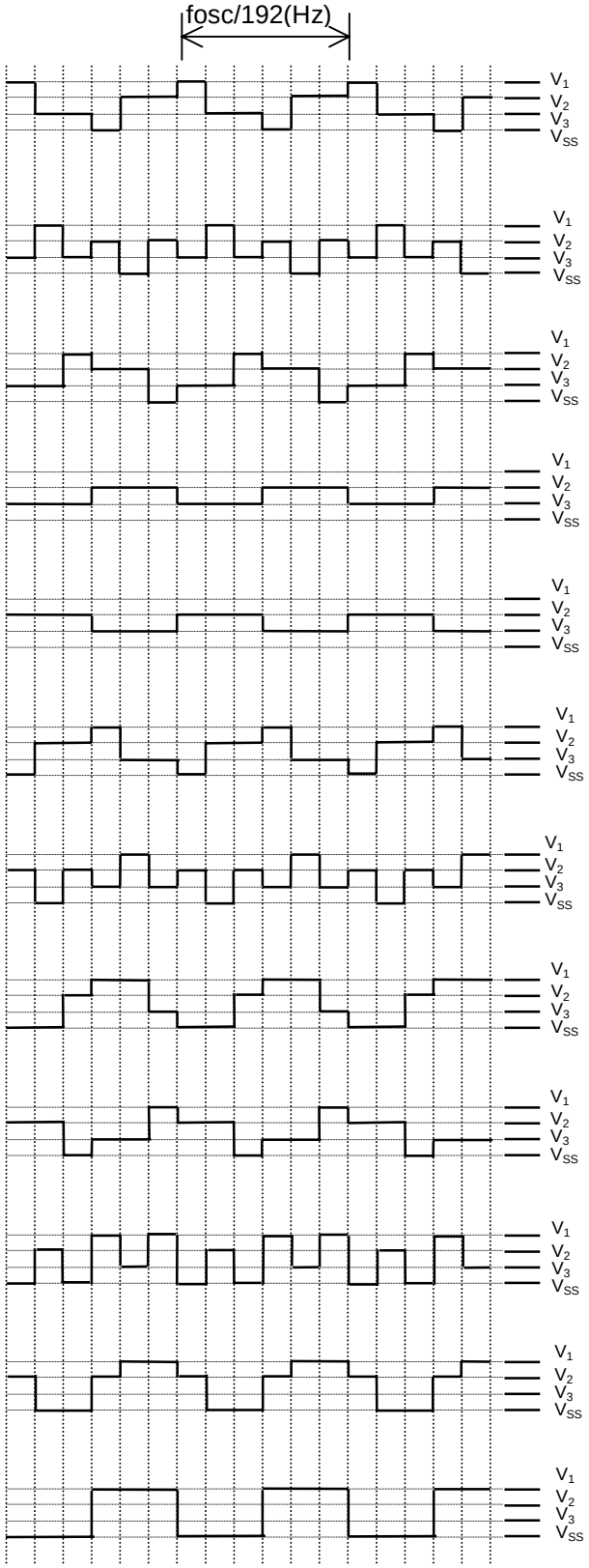
1/2duty, 1/3bias,B waveform



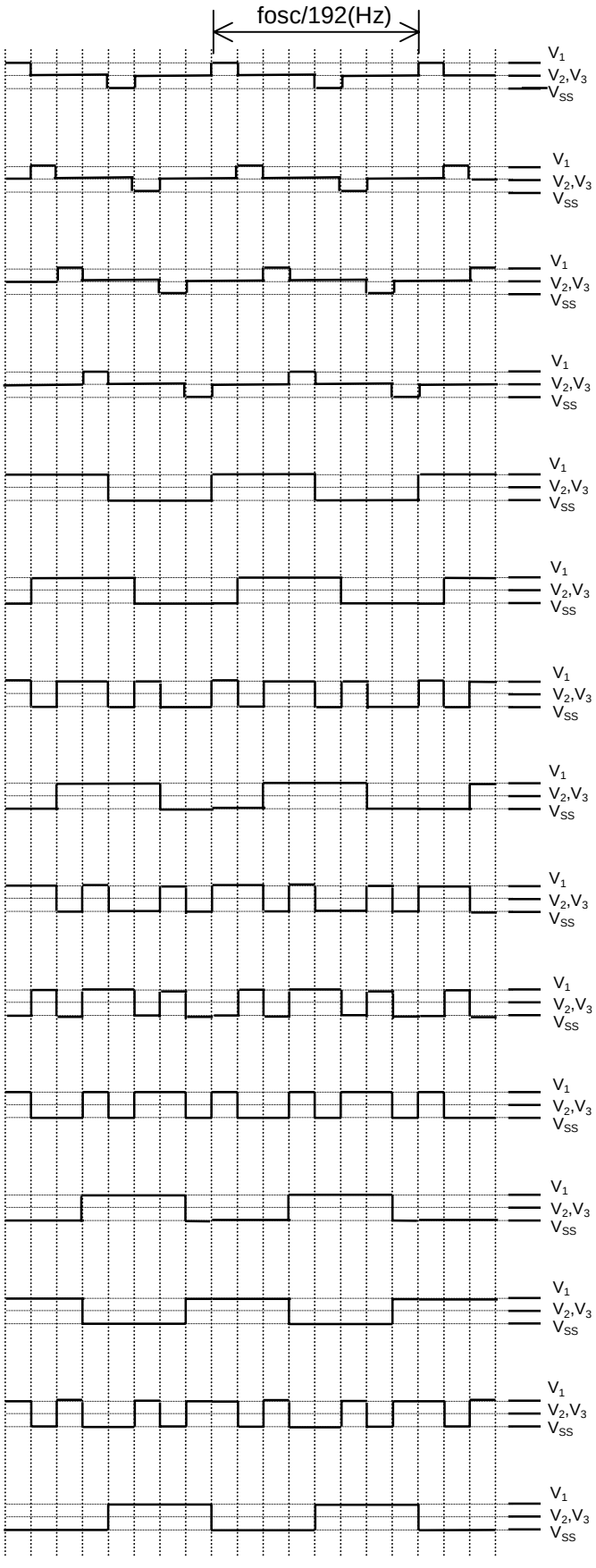
1/3duty, 1/2bias, B waveform



1/3duty, 1/3bias, B waveform



1/4duty, 1/2bias, B waveform



"OFF" segment output correspond to COM1, 2, 3 and 4.

"ON" segment output correspond to COM1.

"ON" segment output correspond to COM2.

"ON" segment output correspond to COM1 and 2.

"ON" segment output correspond to COM3.

"ON" segment output correspond to COM1 and 3.

"ON" segment output correspond to COM2 and 3.

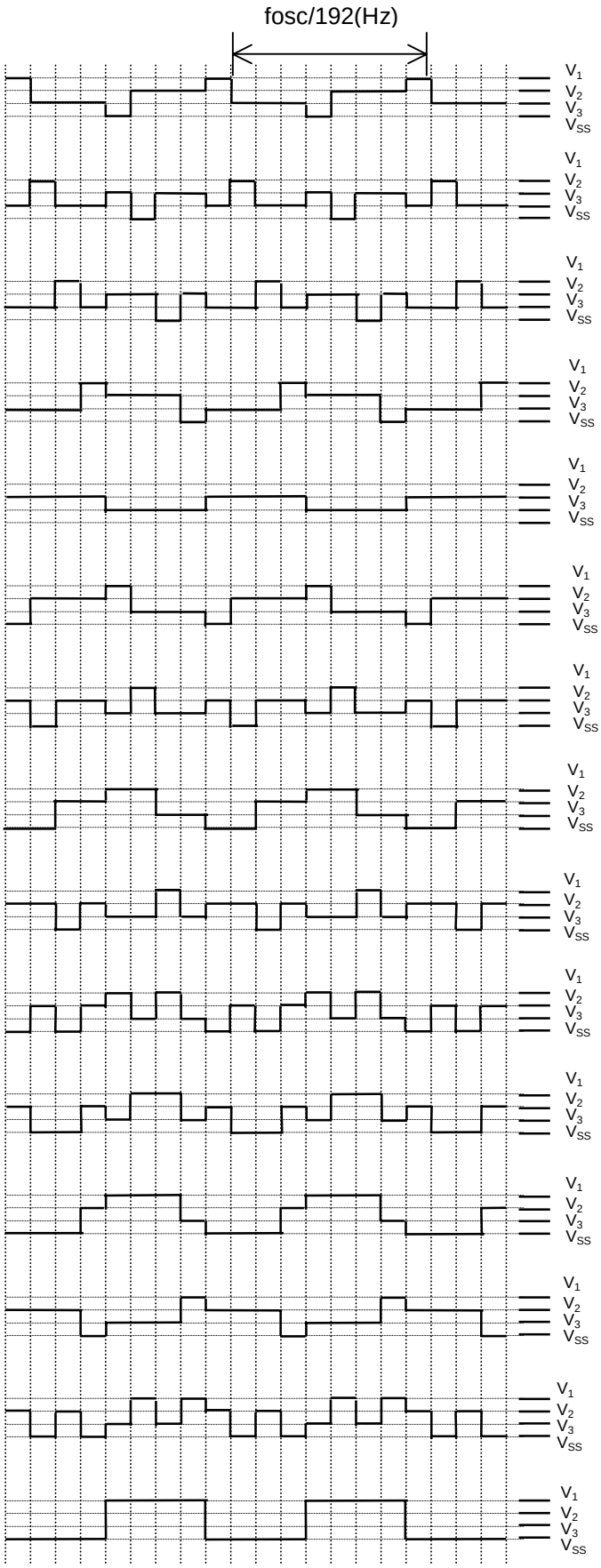
"ON" segment output correspond to COM1, 2 and 3.

"ON" segment output correspond to COM4.

"ON" segment output correspond to COM2 and 4.

"ON" segment output correspond to COM1, 2, 3 and 4.

1/4duty, 1/3bias, B waveform



"OFF" segment output correspond to COM1, 2, 3 and 4.

"ON" segment output correspond to COM1.

"ON" segment output correspond to COM2.

"ON" segment output correspond to COM1 and 2.

"ON" segment output correspond to COM3.

"ON" segment output correspond to COM1 and 3.

"ON" segment output correspond to COM2 and 3.

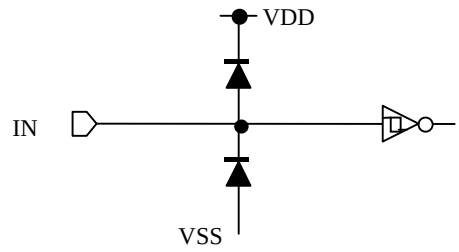
"ON" segment output correspond to COM1, 2 and 3.

"ON" segment output correspond to COM4.

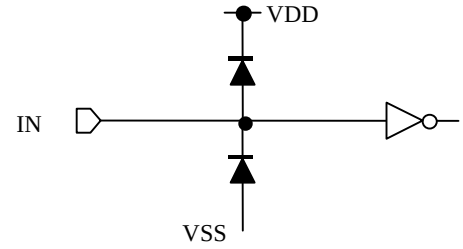
"ON" segment output correspond to COM2 and 4.

"ON" segment output correspond to COM1, 2, 3 and 4.

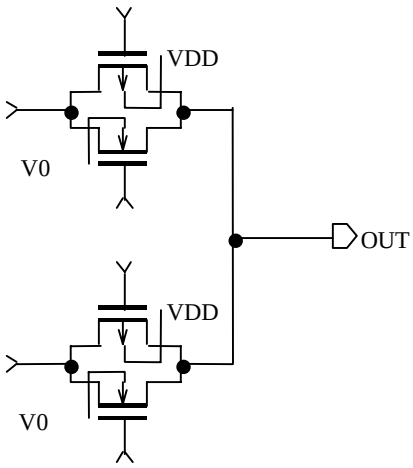
■ Input and Output terminal structure



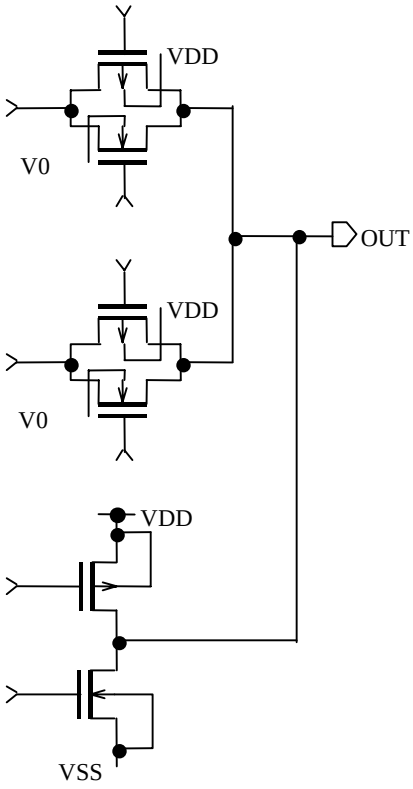
RSTb, TEST, CSb, SI,SCK



OSC



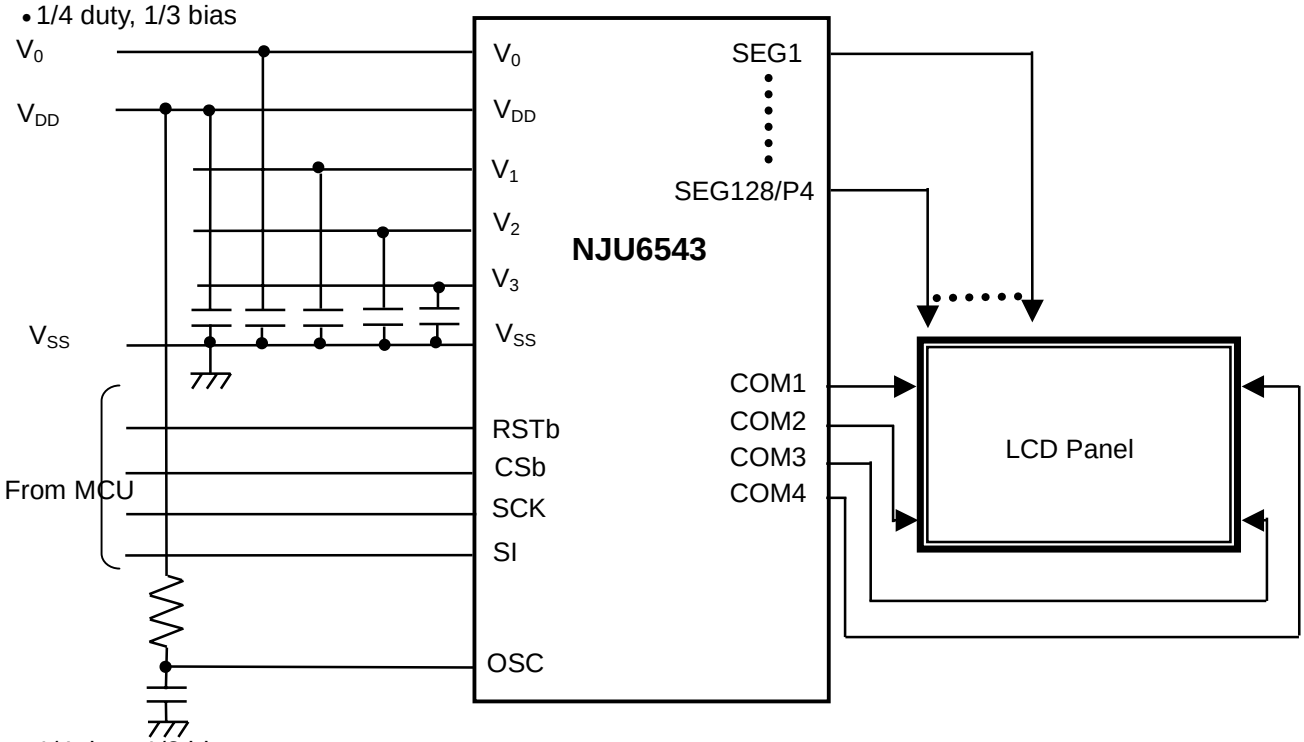
SEG1~SEG124, COM1~COM4



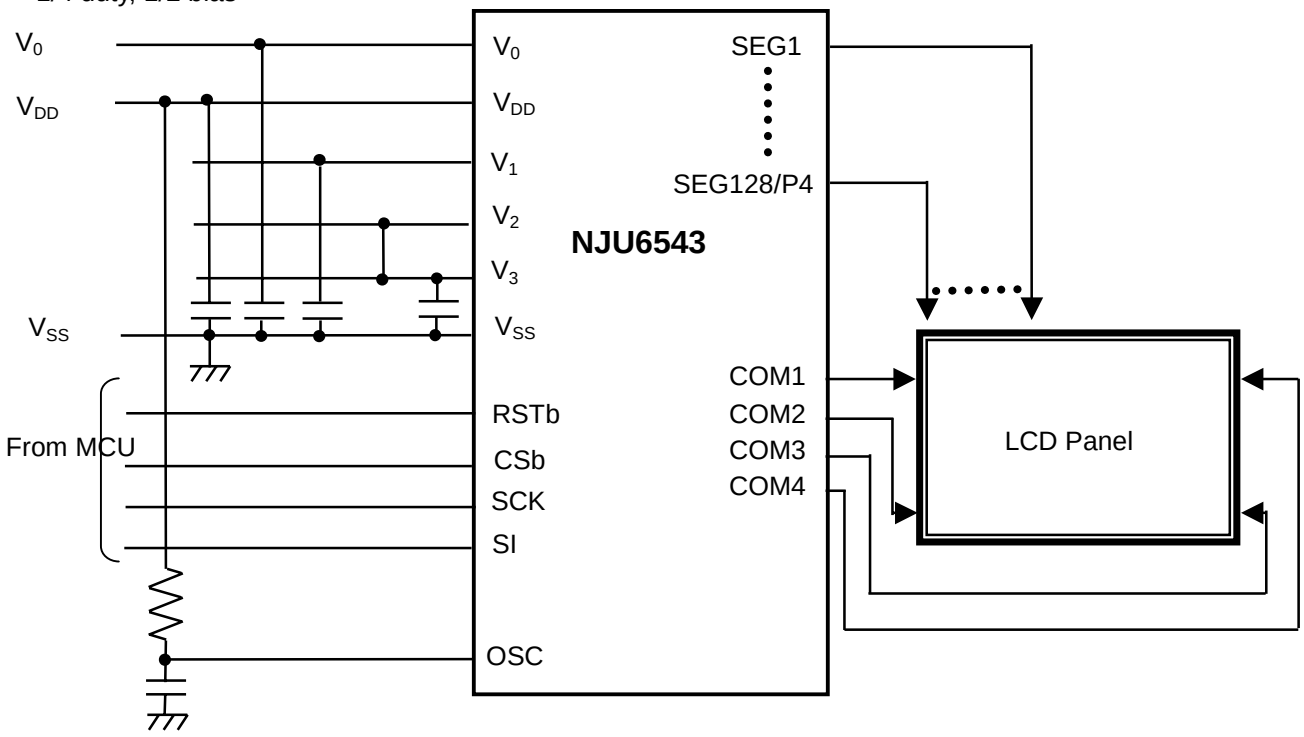
SEG125/P1~SEG128/P4

■ APPLICATION CIRCUIT

• 1/4 duty, 1/3 bias



• 1/4 duty, 1/2 bias



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