

## 8input-2output Video Switch with Isolation Amplifier & small AC-coupled Video Driver

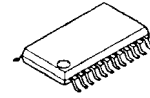
### ■ GENERAL DESCRIPTION

The NJW1341 is 8-Input,2-Output Video Switch.

The NJW1341 consists of switch and isolation amplifiers(2input) and Video Driver which features small AC-coupled(1output).

All of functions are controlled by I2C Bus.

### ■ PACKAGE OUTLINE



NJW1341VC3

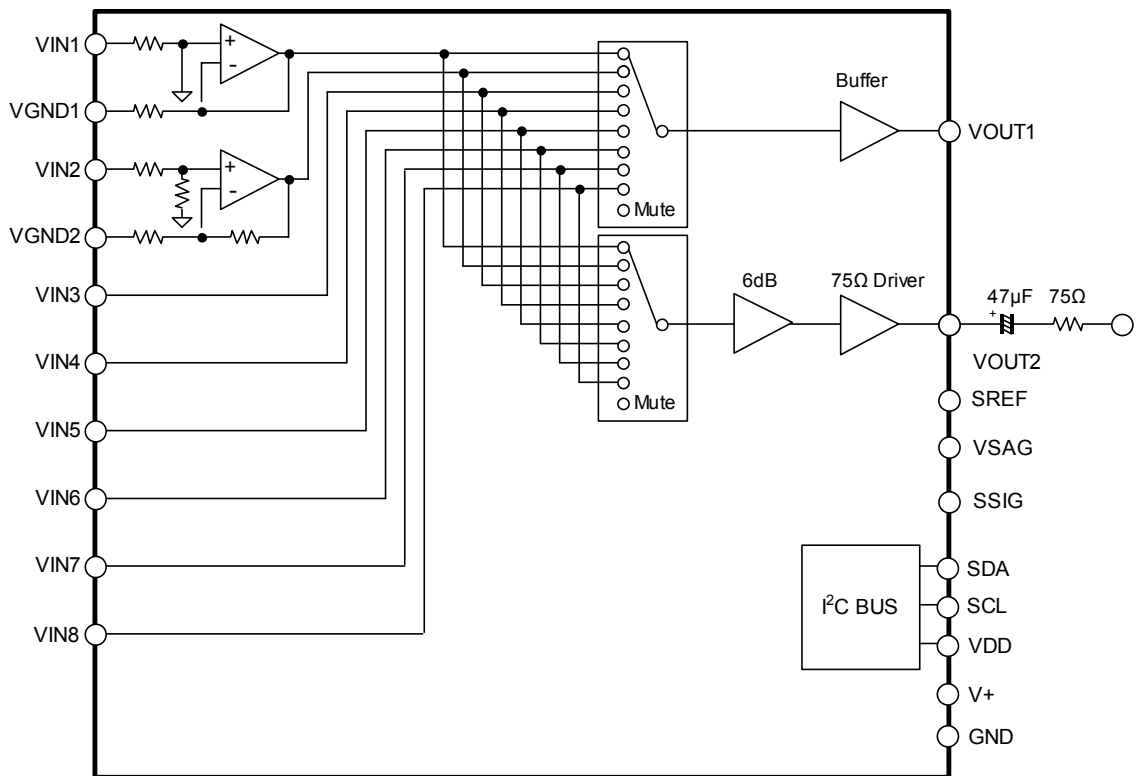
### ■ APPLICATIONS

- Car AVN
- Any Video System

### ■ FEATURES

- Operating Voltage 4.5 to 9.5V
- Small AC-coupled video amplifier (VOUT2)
- Isolation Amplifiers(VIN1,2)
- 8in-2out Video Switch
- Common Mode Rejection Ratio -50dB typ
- Bi-CMOS Technology
- I<sup>2</sup>C BUS interface
- Package Outline SSOP20-C3

### ■ BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATING (Ta=25°C)

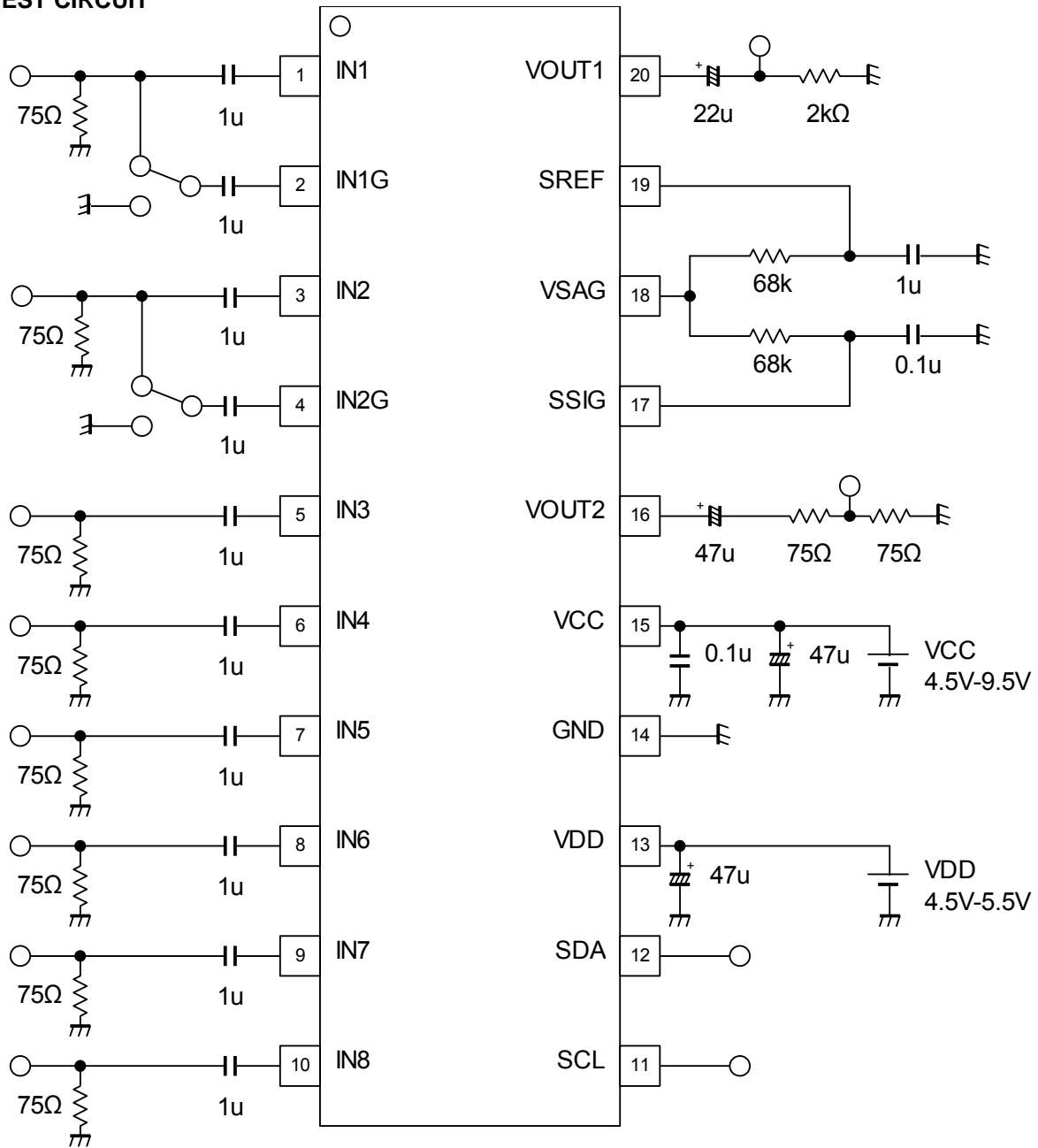
PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V <sup>+</sup>	VCC:+13,VDD:+7	V
Power Dissipation	P <sub>D</sub>	1,000(note1)	mW
Operating Temperature Range	Topr	-40 to +85	°C
Storage Temperature Range	Tstg	-40 to +150	°C

(note1)At on a board of EIA/JEDEC specification. (114.3 x 76.2 x 1.6mm 2 layers, FR-4)

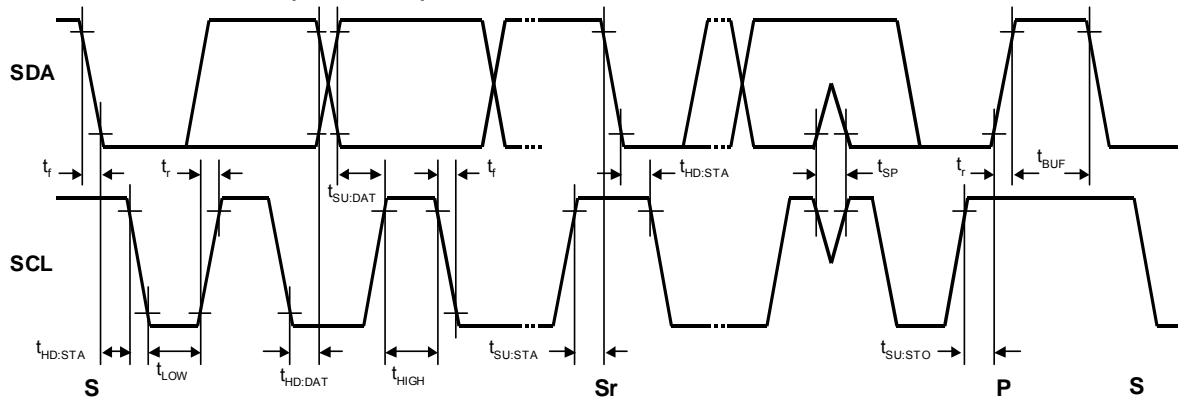
## ■ ELECTRICAL CHARACTERISTICS(V<sup>+</sup>=5V,Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Voltage 1	V <sub>CC</sub>		4.5	5	9.5	V
Operating Voltage 1	V <sub>DD</sub>		4.5	5	5.5	V
Operating Current 1	I <sub>CC1</sub>	No,signal	-	25	40	mA
Operating Current 2	I <sub>CC2</sub>	OUT2 power save	-	10	15	mA
Operating Current 3	I <sub>CC3</sub>	OUT1 power save	-	20	35	mA
Operating Current 4	I <sub>save</sub>	OUT1,OUT2 power save		2	4	mA
Maximum Output Voltage	V <sub>vom</sub>	f=100kHz,THD=1%	2.4	-	-	Vp-p
Voltage Gain1	Gv1	OUT1,Vin=1MHz,1.0Vp-p,Sine Signal	-1.0	0	1.0	dB
Voltage Gain2	Gv2	OUT2,Vin=1MHz,1.0Vp-p,Sine Signal	5.5	6.0	6.5	dB
Low Pass Filter Characteristic 1	Gf	Vin=10MHz /1MHz, 1.0Vp-p sine wave	-1.0	0	1.0	dB
Differential Gain	DG	Vin=1.0Vp-p,10step Video Signal	-	0.5	-	%
Differential Phase	DP	Vin=1.0Vp-p,10step Video Signal	-	0.5	-	deg
S/N Ratio	SN	Vin=1.0Vp-p, 100% White video signal,RL=75Ω, 100KHz to 6MHz	-	60	-	dB
Common mode Rejection Ratio	CMR	Vin=20kHz, 1.0Vp-p Sine Signal	-	-55	-	dB
CrossTalk	CT	Vin=4.43MHz, 1.0Vp-p Sine Signal		-60		dB

## ■ TEST CIRCUIT



## ■TIMING on the I<sup>2</sup>C BUS (SDA, SCL)



## ■CHARACTERISTICS OF BUS LINES (SDA, SCL) FOR I<sup>2</sup>C BUS DEVICES

I<sup>2</sup>C BUS Load Conditions

STANDARD MODE : Pull up resistance 4kΩ (Connected to +3.3V), Load capacitance 200pF (Connected to GND)

FAST MODE : Pull up resistance 4kΩ (Connected to +3.3V), Load capacitance 50pF (Connected to GND)

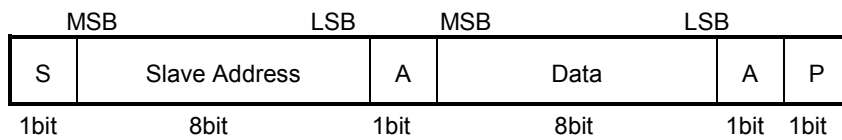
PARAMETER	SYM BOL	Standard mode			Fast mode			UNIT
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Low Level Input Voltage	V <sub>IL</sub>	0.0	-	1.5	0.0	-	1.5	V
High Level Input Voltage	V <sub>IH</sub>	2.7	-	5.0	2.7	-	5.0	V
Hysteresis of Schmitt Trigger Inputs	V <sub>hys</sub>	-	-	-	0.25	-	-	V
Low level Output Voltage (3mA at SDA pin)	V <sub>OL</sub>	0	-	0.4	0	-	0.4	V
Output Fall Time From V <sub>IHmin</sub> to V <sub>ILmax</sub> with a Bus Capacitance from 10pF to 400pF	t <sub>of</sub>	-	-	250	20 +0.1C <sub>b</sub>	-	250	ns
Pulse width of spikes which must be suppressed by the input filter	t <sub>SP</sub>	-	-	-	0	-	50	ns
Input Current each I/O pin with an Input Voltage between 0.1 and 0.9V <sub>DDmax</sub>	I <sub>i</sub>	-10	-	10	-10	-	10	μA
Capacitance for each I/O pin	C <sub>i</sub>	-	-	10	-	-	10	pF
SCL Clock Frequency	f <sub>SCL</sub>	-	-	100	-	-	400	kHz
Data Transfer Start Minimum Waiting Time	t <sub>HD:STA</sub>	4.0	-	-	0.6	-	-	μs
Low Level Clock Pulse Width	t <sub>LOW</sub>	4.7	-	-	1.3	-	-	μs
High Level Clock Pulse Width	t <sub>HIGH</sub>	4.0	-	-	0.6	-	-	μs
Minimum Start Preparation Waiting Time	t <sub>SU:STA</sub>	4.7	-	-	0.6	-	-	μs
Minimum Data Hold Time <sup>(NOTE)</sup>	t <sub>HD:DAT</sub>	0.0	-	3.45	0.0	-	0.9	μs
Minimum Data Preparation Time	t <sub>SU:DAT</sub>	250	-	-	100	-	-	ns
Rise Time	t <sub>r</sub>	-	-	1000	-	-	300	ns
Fall Time	t <sub>f</sub>	-	-	300	-	-	300	ns
Minimum Stop Preparation Waiting Time	t <sub>SU:STO</sub>	4.0	-	-	0.6	-	-	μs
Data Change Minimum Waiting Time	t <sub>BUF</sub>	4.7	-	-	1.3	-	-	μs
Capacitive load for each bus line	C <sub>b</sub>	-	-	400	-	-	400	pF
Noise Margin at the Low Level	V <sub>nL</sub>	0.5	-	-	0.5	-	-	V
Noise Margin at the High Level	V <sub>nH</sub>	1	-	-	1	-	-	V

C<sub>b</sub> ; total capacitance of one bus line in pF.

(NOTE). Please hold the Data Hold Time (t<sub>HD:DAT</sub>) to 300ns or more to avoid status of unstable at SCL falling edge.

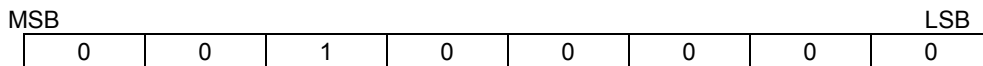
## ■ DEFINITION OF I<sup>2</sup>C REGISTER

### ◆ I<sup>2</sup>C BUS FORMAT



S: Starting Term  
A: Acknowledge Bit  
P: Ending Term

### ◆ SLAVE ADDRESS



R/W=0: Receive Only  
R/W=1: Data is not transmitted.

### ◆ CONTROL REGISTER DEFAULT VALUE

Control register default values are as follows :

	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
Data	0	0	0	0	0	0	0	0

### ◆ INSTRUCTION CODE

	BIT							
	D7	D6	D5	D4	D3	D2	D1	D0
Data	OUT1 MUTE	OUT1 Select			OUT2 MUTE	OUT2 Select		

### ◆ MUTE TABLE

MUTE	OUT1
D7	
0	MUTE OFF
1	MUTE ON

MUTE	OUT2
D3	
0	MUTE OFF
1	MUTE ON

MUTE OFF: Active mode  
MUTE ON: Power save mode

## ◆VOUT SELECT TABLE

OUT1 Select			OUT1
D6	D5	D4	
0	0	0	VIN1
0	0	1	VIN2
0	1	0	VIN3
0	1	1	VIN4
1	0	0	VIN5
1	0	1	VIN6
1	1	0	VIN7
1	1	1	VIN8

OUT2 Select			OUT2
D2	D1	D0	
0	0	0	VIN1
0	0	1	VIN2
0	1	0	VIN3
0	1	1	VIN4
1	0	0	VIN5
1	0	1	VIN6
1	1	0	VIN7
1	1	1	VIN8

**[CAUTION]**

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