FAIRCHILD
SEMICONDUCTOR™

PRELIMINARY
March 1999

NM25C640
64K-Bit Serial CMOS EEPROM
(Serial Peripheral Interface (SPI) Synchronous Bus)

General Description

The NM25C640 is a 65,536-bit CMOS EEPROM with an SPI compatible serial interface. The NM25C640 is designed for data storage in applications requiring both non-volatile memory and in-system data updates. This EEPROM is well suited for applications using the 68HC11 series of microcontrollers that support the SPI interface for high speed communication with peripheral devices via a serial bus to reduce pin count. The NM25C640 is implemented in Fairchild Semiconductor's floating gate CMOS process that provides superior endurance and data retention.

The serial data transmission of this device requires four signal lines to control the device operation: Chip Select ($\overline{CS}$), Clock (SCK), Data In (SI), and Serial Data Out (SO). All programming cycles are completely self-timed and do not require an erase before WRITE.

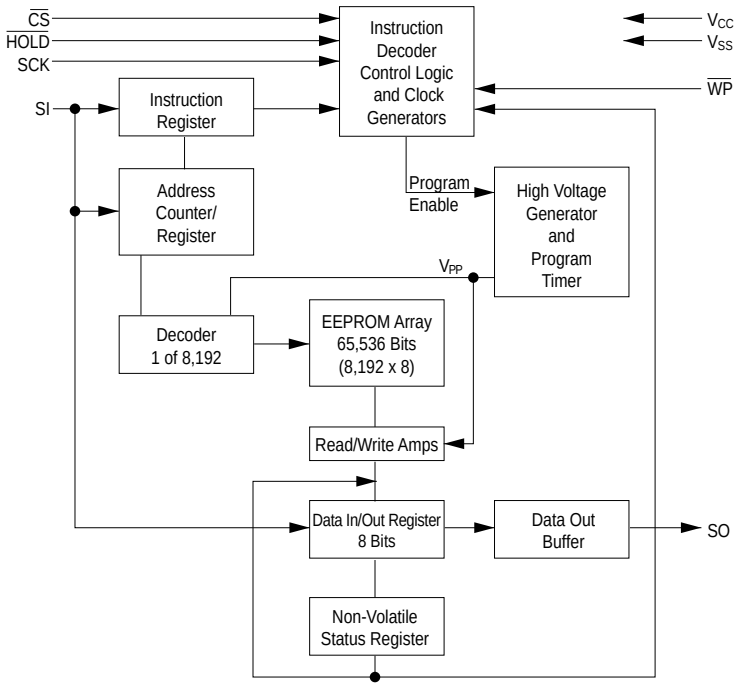
BLOCK WRITE protection is provided by programming the STATUS REGISTER with one of four levels of write protection. Additionally, separate WRITE enable and WRITE disable instructions are provided for data protection.

Hardware data protection is provided by the $\overline{WP}$ pin to protect against inadvertent programming. The $\overline{HOLD}$ pin allows the serial communication to be suspended without resetting the serial sequence.

Features

- 2.75 MHz clock rate @ 4.5V to 5.5V
  2.1 MHz @ 2.7V to 4.5V
- 65,536 bits organized as 8,192 x 8
- Multiple chips on the same 3-wire bus with separate chip select lines
- Self-timed programming cycle
- Simultaneous programming of 1 to 32 bytes at a time
- Status register can be polled during programming to monitor READY/BUSY
- Write Protect ($\overline{WP}$) pin and write disable instruction for both hardware and software write protection
- Block write protect feature to protect against accidental writes
- Endurance: 1,000,000 data changes
- Data retention greater than 40 years
- Packages available: 8-pin DIP or 8-Pin SO

Block Diagram



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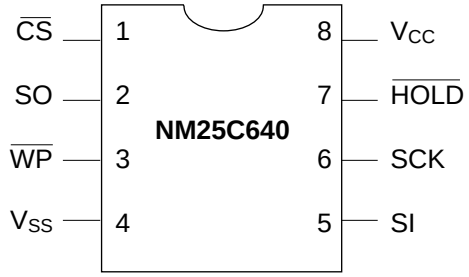
Connection Diagram

**Dual-In-Line Package (N)
and SO Package (M8)**



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Top View

Pin Names

$\overline{CS}$	Chip Select Input
SO	Serial Data Output
$\overline{WP}$	Write Protect
V_{SS}	Ground
SI	Serial Data Input
SCK	Serial Clock Input
$\overline{HOLD}$	Suspends Serial Data
V_{CC}	Power Supply

Ordering Information

		Letter	Description
NM 25 C XX LZ E XX	**Package**	N	8-Pin DIP
		M8	8-Pin SO
	Temp. Range	None	0 to 70°C
		V	-40 to +125°C
		E	-40 to +85°C
	Voltage Operating Range	Blank	4.5V to 5.5V
		L	2.7V to 4.5V
		LZ	2.7V to 4.5V and <1µA Standby Current
	Density/Mode	640	64K, mode 0
		C	CMOS
	Interface	25	SPI
		NM	**Fairchild Nonvolatile Memory**

Standard Voltage 4.5 ≤ V_{CC} ≤ 5.5V Specifications

Absolute Maximum Ratings (Note 1)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM25C640	0°C to +70°C
NM25C640E	-40°C to +85°C
NM25C640V	-40°C to +125°C
Power Supply (V_{CC})	4.5V to 5.5V

DC and AC Electrical Characteristics 4.5V ≤ V_{CC} ≤ 5.5V (unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Units
I_{CC}	Operating Current	$\overline{CS}$ = V_{IL}		3	mA
I_{CCSB}	Standby Current	$\overline{CS}$ = V_{CC}		50	µA
I_{IL}	Input Leakage	V_{IN} = 0 to V_{CC}	-1	+1	µA
I_{OL}	Output Leakage	V_{OUT} = GND to V_{CC}	-1	+1	µA
V_{IL}	CMOS Input Low Voltage		-0.3	V_{CC} * 0.3	V
V_{IH}	CMOS Input High Voltage		V_{CC} * 0.7	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = -0.8 mA	V_{CC} - 0.8		V
f_{OP}	SCK Frequency			2.75	MHz
t_{RI}	Input Rise Time			2.0	µs
t_{FI}	Input Fall Time			2.0	µs
t_{CLH}	Clock High Time	(Note 2)	155		ns
t_{CLL}	Clock Low Time	(Note 2)	155		ns
t_{CSH}	Min $\overline{CS}$ High Time	(Note 3)	240		ns
t_{CSS}	$\overline{CS}$ Setup Time		176		ns
t_{DIS}	Data Setup Time		50		ns
t_{HDS}	$\overline{HOLD}$ Setup Time		90		ns
t_{CSN}	$\overline{CS}$ Hold Time		155		ns
t_{DIN}	Data Hold Time		50		ns
t_{HDN}	$\overline{HOLD}$ Hold Time		90		ns
t_{PD}	Output Delay	C_L = 200 pF		135	ns
t_{DH}	Output Hold Time		0		ns
t_{LZ}	$\overline{HOLD}$ to Output Low Z			240	ns
t_{DF}	Output Disable Time	C_L = 200 pF		290	ns
t_{HZ}	$\overline{HOLD}$ to Output High Z			240	ns
t_{WP}	Write Cycle Time	1–32 Bytes		10	ms

Capacitance T_A = 25°C, f = 2.1/1 MHz (Note 4)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance	3	8	pF
C_{IN}	Input Capacitance	2	6	pF

AC Test Conditions

Output Load	C_L = 200 pF
Input Pulse Levels	0.1 * V_{CC} – 0.9 * V_{CC}
Timing Measurement Reference Level	0.3 * V_{CC} - 0.7 • V_{CC}

Note 1: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The f_{OP} frequency specification specifies a minimum clock period of $1/f_{OP}$. Therefore, for every f_{OP} clock cycle, t_{CLH} + t_{CLL} must be equal to or greater than $1/f_{OP}$. For example, if the 2.1MHz period = 476ns and t_{CLH} = 190ns, t_{CLL} must be 286ns.

Note 3: $\overline{CS}$ must be brought high for a minimum of t_{CSH} between consecutive instruction cycles.

Note 4: This parameter is periodically sampled and not 100% tested.

Low Voltage 2.7V ≤ V_{CC} ≤ 4.5V Specifications

Absolute Maximum Ratings (Note 5)

Ambient Storage Temperature	-65°C to +150°C
All Input or Output Voltage with Respect to Ground	+6.5V to -0.3V
Lead Temp. (Soldering, 10 sec.)	+300°C
ESD Rating	2000V

Operating Conditions

Ambient Operating Temperature	
NM25C640L/LZ	0°C to +70°C
NM25C640LZ/LZE	-40°C to +85°C
NM25C640LV	-40°C to +125°C
Power Supply (V_{CC})	2.7V–4.5V

DC and AC Electrical Characteristics 2.7V ≤ V_{CC} ≤ 4.5V (unless otherwise specified)

Symbol	Parameter	Part	Conditions	25C640L/LE 25C640LZ/LZE		25C640LV		Units
				Min.	Max.	Min	Max	
I_{CC}	Operating Current		$\overline{CS}$ = V_{IL}		3		3	mA
I_{CCSB}	Standby Current	L LZ	$\overline{CS}$ = V_{CC}		10 1		10 N/A	µA µA
I_{IL}	Input Leakage		V_{IN} = 0 to V_{CC}	-1	1	-1	1	µA
I_{OL}	Output Leakage		V_{OUT} = GND to V_{CC}	-1	1	-1	1	µA
V_{IL}	Input Low Voltage			-0.3	0.3 * V_{CC}	-0.3	0.3 * V_{CC}	V
V_{IH}	Input High Voltage			0.7 * V_{CC}	V_{CC} + 0.3	0.7 * V_{CC}	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage		I_{OL} = 1.6 mA		0.4		0.4	V
V_{OH}	Output High Voltage		I_{OH} = –0.8 mA	V_{CC} - 0.8		V_{CC} - 0.8		V
f_{OP}	SCK Frequency				2.1		1.0	MHz
t_{RI}	Input Rise Time				2.0		2.0	µs
t_{FI}	Input Fall Time				2.0		2.0	µs
t_{CLH}	Clock High Time		(Note 6)	190		410		ns
t_{CLL}	Clock Low Time		(Note 6)	190		410		ns
t_{CSH}	Min. $\overline{CS}$ High Time		(Note 7)	240		500		ns
t_{CSS}	$\overline{CS}$ Setup Time			240		500		ns
t_{DIS}	Data Setup Time			100		100		ns
t_{HDS}	$\overline{HOLD}$ Setup Time			90		240		ns
t_{CSN}	$\overline{CS}$ Hold Time			240		500		ns
t_{DIN}	Data Hold Time			100		100		ns
t_{HDN}	$\overline{HOLD}$ Hold Time			90		240		ns
t_{PD}	Output Delay		C_L = 200 pF		240		500	ns
t_{DH}	Output Hold Time			0		0		ns
t_{LZ}	$\overline{HOLD}$ Output Low Z				100		240	ns
t_{DF}	Output Disable Time		C_L = 200 pF		240		500	ns
t_{HZ}	$\overline{HOLD}$ to Output Hi Z				100		240	ns
t_{WP}	Write Cycle Time		1-32 Bytes		15		15	ms

Capacitance T_A = 25°C, f = 2.1/1 MHz (Note 8)

Symbol	Test	Typ	Max	Units
C_{OUT}	Output Capacitance	3	8	pF
C_{IN}	Input Capacitance	2	6	pF

AC Test Conditions

Output Load	C_L = 200pF
Input Pulse Levels	0.1 * V_{CC} - 0.9 * V_{CC}
Timing Measurement Reference Level	0.3 * V_{CC} - 0.7 * V_{CC}

Note 5: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 6: The f_{OP} frequency specification specifies a minimum clock period of $1/f_{OP}$. Therefore, for every f_{OP} clock cycle, t_{CLH} + t_{CLL} must be equal to or greater than $1/f_{OP}$. For example, if the 2.1MHz period = 476ns and t_{CLH} = 190ns, t_{CLL} must be 286ns.

Note 7: $\overline{CS}$ must be brought high for a minimum of t_{CSH} between consecutive instruction cycles.

Note 8: This parameter is periodically sampled and not 100% tested.

AC Test Conditions (Continued)

FIGURE 1. Synchronous Data Timing Diagram

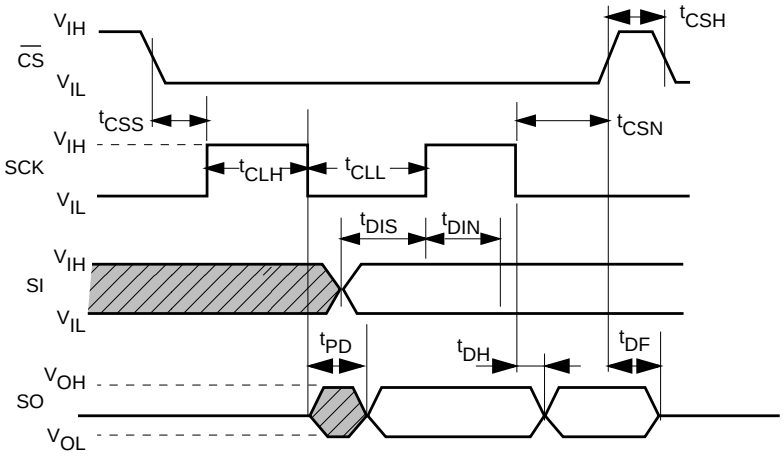

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FIGURE 2. Hold Timing

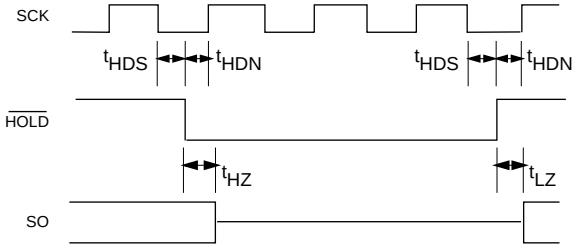

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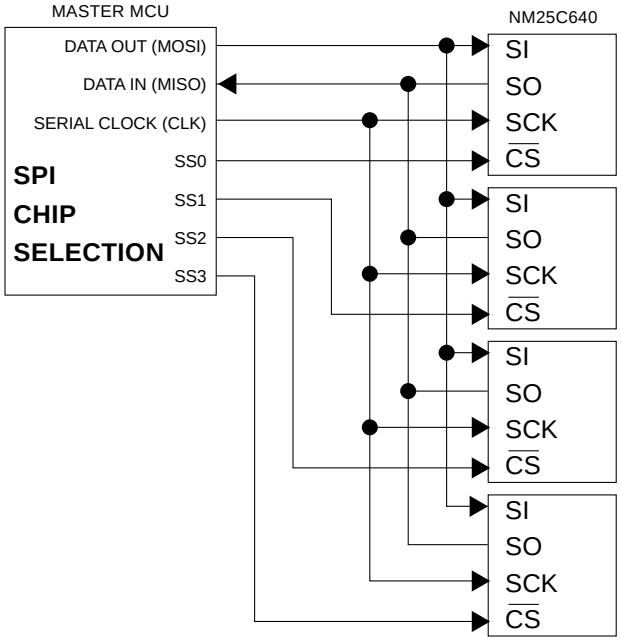
FIGURE 3. SPI Serial Interface



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Functional Description

TABLE 1. Instruction Set

Instruction Name	Instruction Opcode	Operation
WREN	00000110	Set Write Enable Latch
WRDI	00000100	Reset Write Enable Latch
RDSR	00000101	Read Status Register
WRSR	00000001	Write Status Register
READ	00000011	Read Data from Memory Array
WRITE	00000010	Write Data to Memory Array

MASTER: The device that generates the serial clock is designated as the master. The NM25C640 can never function as a master.

SLAVE: The NM25C640 always operates as a slave as the serial clock pin is always an input.

TRANSMITTER/RECEIVER: The NM25C640 has separate pins for data transmission (SO) and reception (SI).

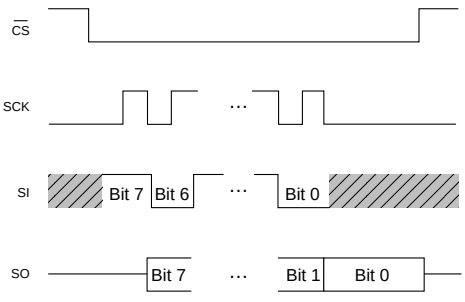
MSB: The Most Significant Bit is the first bit transmitted and received.

CHIP SELECT: The chip is selected when pin $\overline{CS}$ is low. When the chip is *not* selected, data will not be accepted from pin SI, and the output pin SO is in high impedance.

SERIAL OP-CODE: The first byte transmitted after the chip is selected with $\overline{CS}$ going low contains the op-code that defines the operation to be performed.

PROTOCOL: When connected to the SPI port of a 68HC11 microcontroller, the NM25C640 accepts a clock phase of 0 and a clock polarity of 0. The SPI protocol for this device defines the byte transmitted on the SI and SO data lines for proper chip operation. See Figure 4.

FIGURE 4. SPI Protocol



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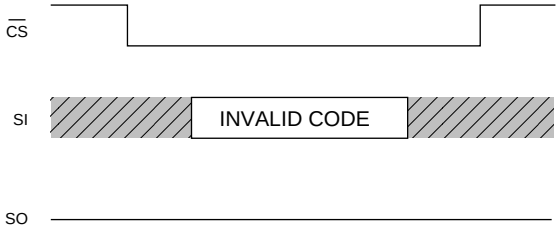
Data is clocked in on the positive SCK edge and out on the negative SCK edge.

HOLD: The $\overline{HOLD}$ pin is used in conjunction with the $\overline{CS}$ to select the device. Once the device is selected and a serial sequence is underway, $\overline{HOLD}$ may be forced low to suspend further serial communication with the device without resetting the serial sequence. Note that $\overline{HOLD}$ must be brought low while the SCK pin is low. The device must remain selected during this sequence. To resume serial communication $\overline{HOLD}$ is brought high while the SCK pin is low. The SO pin is at a high impedance state during $\overline{HOLD}$.

INVALID OP-CODE: After an invalid code is received, no data is shifted into the NM25C640, and the SO data output pin remains high impedance until a new $\overline{CS}$ falling edge reinitializes the serial communication. See Figure 5 .

FIGURE 5. Invalid Op-Code



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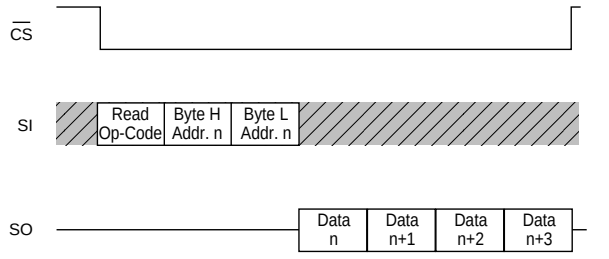
Functional Description (Continued)

READ SEQUENCE: Reading the memory via the serial SPI link requires the following sequence. The $\overline{CS}$ line is pulled low to select the device. The READ op-code is transmitted on the SI line followed by the high order address byte (A12–A8), and the low order address byte (A7–A0). The leading three bits in the high order address byte will be ignored. After this is done, data on the SI line becomes don't care. The data (D7–D0) at the address specified is then shifted out on the SO line. If only one byte is to be read, the $\overline{CS}$ line can be pulled back to the high level. It is possible to continue the READ sequence as the byte adress is automatically incremented and data will continue to be shifted out. When the highest address is reached (1FFF), the address counter rolls over to lowest address (000) allowing the entire memory to be read in one continuous READ cycle. See Figure 6.

FIGURE 6. Read Sequence



READ STATUS REGISTER (RDSR) : The Read Status Register (RDSR) instruction provides access to the status register is used to interrogate the READY/BUSY and WRITE ENABLE status of the chip. Two non-volatile status register bits are used to select one of four levels of BLOCK WRITE PROTECTION. The status register format is shown in Table 2.

TABLE 2. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
X	X	X	X	BP1	BP0	WEN	$\overline{RDY}$

X = Don't Care.

Status register Bit 0 = 0 ($\overline{RDY}$) indicates that the device is READY; Bit 0 = 1 indicates that a program cycle is in progress. Bit 1 = 0 (WEN) indicates that the device is not WRITE ENABLED; Bit 1 = 1 indicates that the device is WRITE ENABLED. Non-volatile status register Bits 2 and 3 (BP0 and BP1) indicate the level of BLOCK WRITE PROTECTION selected. The block write protection levels and corresponding status register control bits are shown in Table 3. **Note that if a RDSR instruction is executed during a programming cycle only the RDY bit is valid. All other bits are 1s.** See Figure 7.

FIGURE 7. Read Status

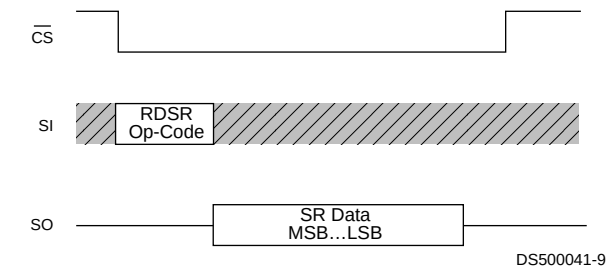
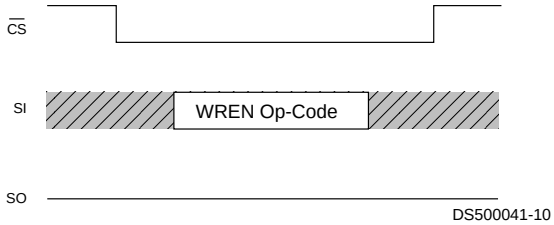


TABLE 3. Block Write Protection Levels

Level	Status Register Bits		Array Address Protected
	BP1	BP0	
0	0	0	None
1	0	1	1800-1FFF
2	1	0	1000-1FFF
3	1	1	0000–1FFF

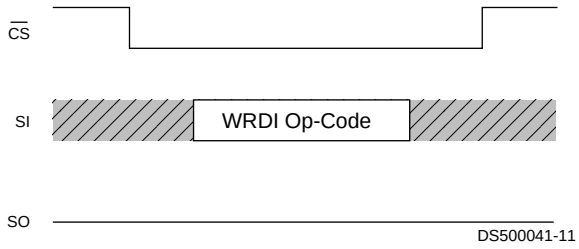
WRITE ENABLE (WREN): When V_{CC} is applied to the chip, it "powers up" in the write disable state. Therefore, all programming modes must be preceded by a WRITE ENABLE (WREN) instruction. Additionally, the WP must be held high during a write engble instruction. At the completion of a WRITE or WRSR cycle the device is automatically returned to the write disable state. Note that a WRITE DISABLE (WRD) instruction will also return the device to the write disable state. See Figure 8.

FIGURE 8. Write Enable



WRITE DISABLE (WRDI): To protect against accidental data disturbance the WRITE DISABLE (WRDI) instruction disables all programming modes. See Figure 9.

FIGURE 9. Write Disable

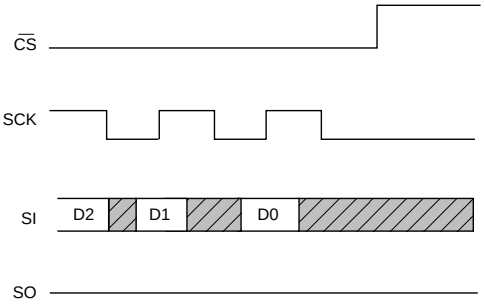


Functional Description (Continued)

WRITE SEQUENCE: To program the device, the WRITE PROTECT ($\overline{WP}$) pin must be held high and two separate instructions must be executed. The chip must first be write enabled via the WRITE ENABLE instruction and then a WRITE instruction must be executed. Moreover, the address of the memory location(s) to be programmed must be outside the protected address field selected by the Block Write Protection Level. See Table 3.

A WRITE command requires the following sequence. The $\overline{CS}$ line is pulled low to select the device, then the WRITE op-code is transmitted on the SI line followed by the high order address byte (A12-A8) and the low order address byte (A7–A0). The leading five bits in the high order address byte will be ignored. The address is followed by the data (D7–D0) to be written. Programming will start after the $\overline{CS}$ pin is forced back to a high level. Note that the LOW to HIGH transition of the $\overline{CS}$ pin must occur during the SCK low time immediately after clocking in the D0 data bit. See Figure 10.

FIGURE 10. End of WRITE Sequence



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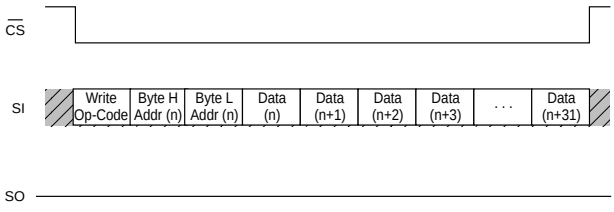
The READY/BUSY status of the device can be determined by executing a READ STATUS REGISTER (RDSR) instruction. Bit 0 = 1 indicates that the WRITE cycle is still in progress and Bit 0 = 0 indicates that the WRITE cycle has ended. During the WRITE programming cycle (Bit 0 = 1) only the READ STATUS REGISTER instruction is enabled.

The NM25C640 is capable of a 32 byte PAGE WRITE operation. After receipt of each byte of data the five low order address bits are internally incremented by one. The eight high order bits of the address will remain constant. If the master should transmit more than 32 bytes of data, the address counter will "roll over," and the previously loaded data will be reloaded. See Figure 11.

FIGURE 11. 32 Byte Page Write



DS500041-13

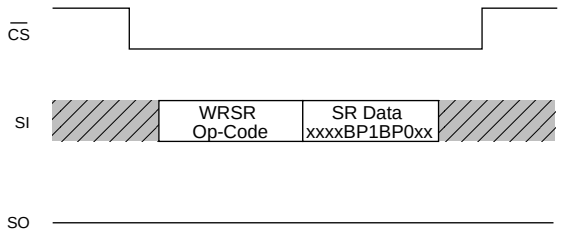
At the completion of a WRITE cycle the device is automatically returned to the write disable state.

If the device is not WRITE enabled, the device will ignore the WRITE instruction and return to the standby state when CS is forced high. A new CS falling edge is required to re-initialize the serial communication.

WRITE STATUS REGISTER (WRSR): The WRITE STATUS REGISTER (WRSR) instruction is used to program the non-volatile status register Bits 2 and 3 (BP0 and BP1). The WRITE PROTECT (WP) pin must be held high and two separate instructions must be executed. The chip must first be write enabled via the WRITE ENABLE instruction and then a WRSR instruction must be executed.

The WRSR command requires the following sequence. The CS line is pulled low to select the device and then the WRSR op-code is transmitted on the SI line followed by the data to be programmed. See Figure 12.

FIGURE 12. Write Status Register



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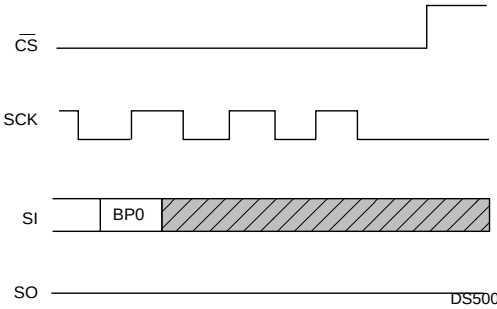
Note that the first four bits are don't care bits followed by BP1 and BP0 then two additional don't care bits. Programming will start after the CS pin is forced back to a high level. As in the WRITE instruction the LOW to HIGH transition of the CS pin must occur during the SCK low time immediately after clocking in the last don't care bit. See Figure 13.

FIGURE 13. Start WRSR Condition

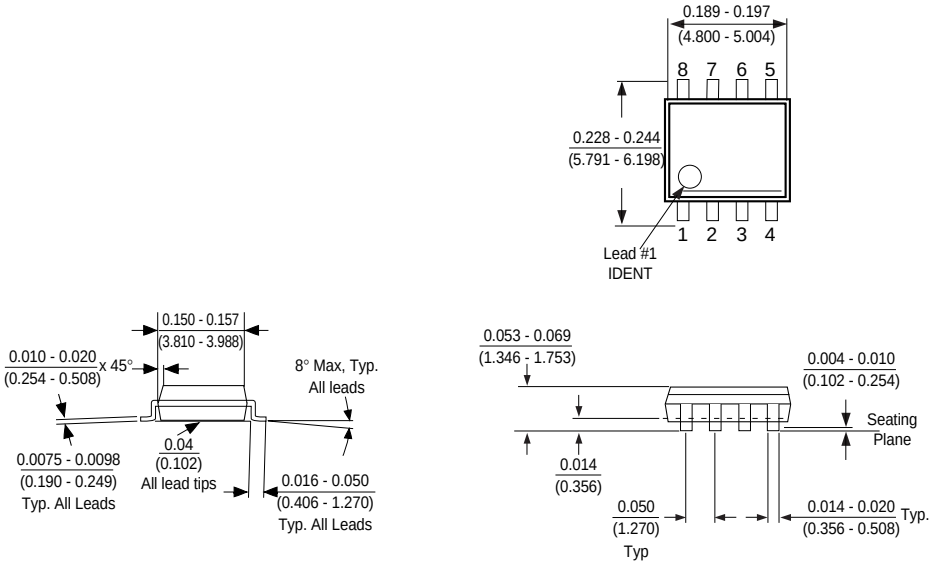


DS500041-15

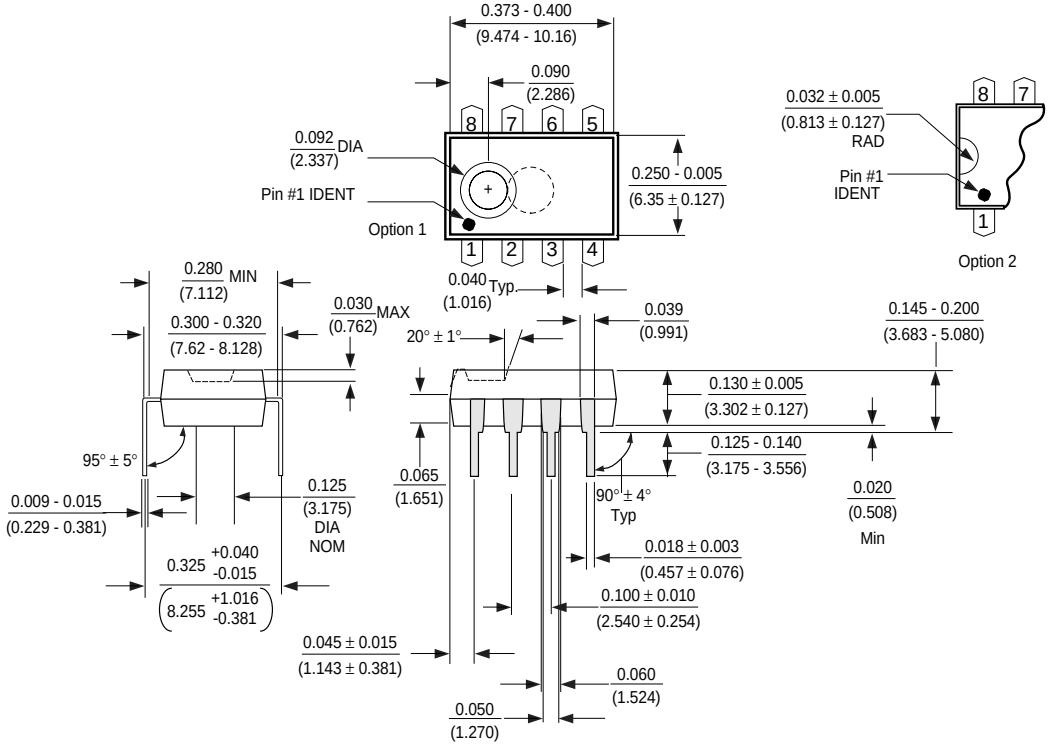
The READY/BUSY status of the device can be determined by executing a READ STATUS REGISTER (RDSR) instruction. Bit 0 = 1 indicates that the WRSR cycle is still in progress and Bit 0 = 0 indicates that the WRSR cycle has ended.

At the completion of a WRITE cycle the device is automatically returned to the write disable state.

Physical Dimensions inches (millimeters) unless otherwise noted



Molded Small Out-Line Package (M8)
Package Number M08A



Molded Dual-In-Line Package (N)
Package Number N08E

Life Support Policy

Fairchild's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Fairchild Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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