Data Sheet

NP90N03VLG

R07DS0129EJ0100
Rev.1.00
Sep 24, 2010

MOS FIELD EFFECT TRANSISTOR

Description

The NP90N03VLG is N-channel MOS Field Effect Transistor designed for high current switching applications.

Features

- Low on-state resistance
  — $R_{DS(on)1}$ = 3.2 mΩ MAX. (V_{GS} = 10 V, I_D = 45 A)
  — $R_{DS(on)2}$ = 8.0 mΩ MAX. (V_{GS} = 4.5 V, I_D = 35 A)
- Low input capacitance
  — Ciss = 5000 pF TYP. (V_{DS} = 25 V, V_{GS} = 0 V)
- Designed for automotive application and AEC-Q101 qualified

Ordering Information

Part No.	LEAD PLATING	PACKING	Package
NP90N03VLG-E1-AY*1	Pure Sn (Tin)	Tape 2500 p/reel	TO-252, Taping (E1 type)
NP90N03VLG-E2-AY*1			TO-252, Taping (E2 type)

Note: *1. Pb-free (This product does not contain Pb in the external electrode.)

Absolute Maximum Ratings (T_A = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	30	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	±90	A
Drain Current (pulse) *1	$I_{D(pulse)}$	±360	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	105	W
Total Power Dissipation (T_A = 25°C)	P_{T2}	1.2	W
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	–55 to +175	°C
Repetitive Avalanche Current *2	I_{AR}	41	A
Repetitive Avalanche Energy *2	E_{AR}	168	mJ

Notes: *1. T_C = 25°C, PW ≤ 10 μs, Duty Cycle ≤ 1%
*2. $T_{ch(peak)}$ ≤ 150°C, R_G = 25 Ω

Thermal Resistance

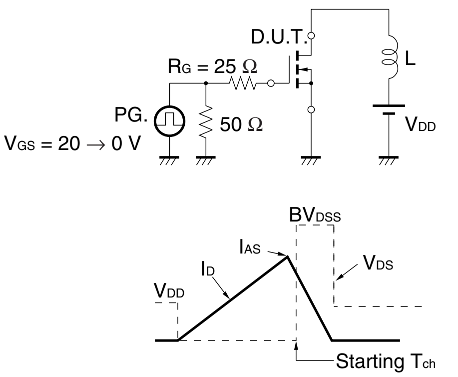
Channel to Case Thermal Resistance	$R_{th(ch-C)}$	1.43	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	125	°C/W

Electrical Characteristics (T_A = 25°C)

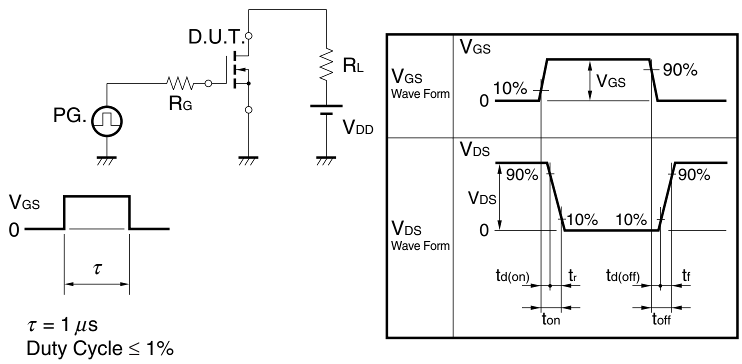
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}			1	µA	V_{DS} = 30 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}			±10	µA	V_{GS} = ±20 V, V_{DS} = 0 V
Gate to Source Threshold Voltage	$V_{GS(th)}$	1.4	1.8	2.5	V	V_{DS} = V_{GS}, I_D = 250 µA
Forward Transfer Admittance *1	| y_{fs} |	30	67		S	V_{DS} = 5 V, I_D = 45 A
Drain to Source On-state Resistance *1	$R_{DS(on)1}$		2.5	3.2	mΩ	V_{GS} = 10 V, I_D = 45 A
	$R_{DS(on)2}$		3.8	8.0	mΩ	V_{GS} = 4.5 V, I_D = 35 A
Input Capacitance	C_{iss}		5000	7500	pF	V_{DS} = 25 V,
Output Capacitance	C_{oss}		600	900	pF	V_{GS} = 0 V,
Reverse Transfer Capacitance	C_{rss}		420	760	pF	f = 1 MHz
Turn-on Delay Time	$t_{d(on)}$		17	34	ns	V_{DD} = 15 V, I_D = 45 A,
Rise Time	t_r		13	33	ns	V_{GS} = 10 V,
Turn-off Delay Time	$t_{d(off)}$		73	146	ns	R_G = 0 Ω
Fall Time	t_f		9	23	ns	
Total Gate Charge	Q_G		90	135	nC	V_{DD} = 24 V,
Gate to Source Charge	Q_{GS}		13		nC	V_{GS} = 10 V,
Gate to Drain Charge	Q_{GD}		26		nC	I_D = 90 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$		0.9	1.5	V	I_F = 90 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}		42		ns	I_F = 90 A, V_{GS} = 0 V,
Reverse Recovery Charge	Q_{rr}		35		nC	di/dt = 100 A/µs

Note: *1. Pulsed

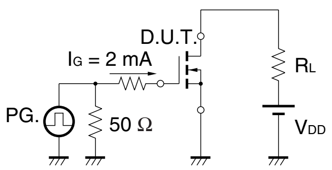
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

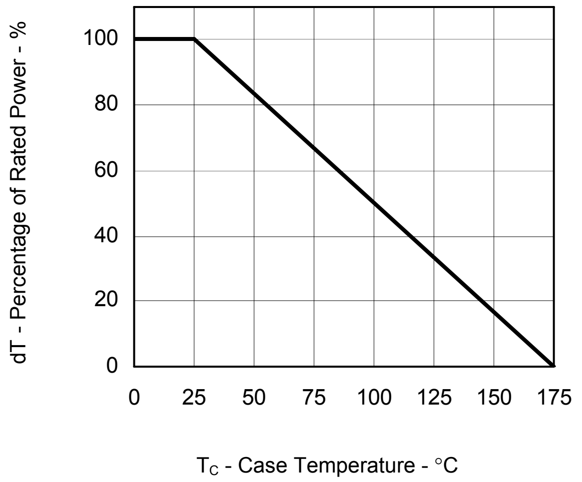


TEST CIRCUIT 3 GATE CHARGE

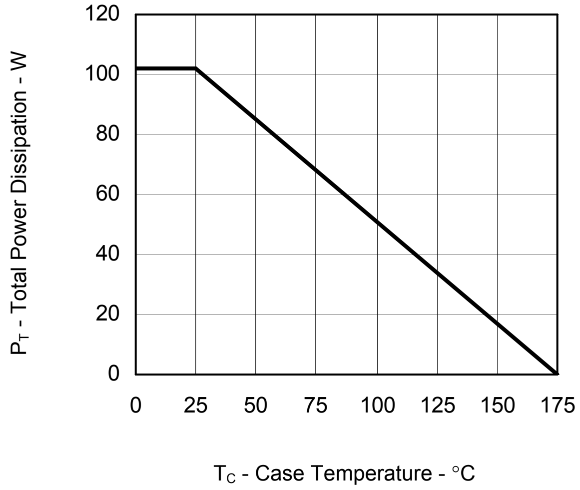


Typical Characteristics (T_A = 25°C)

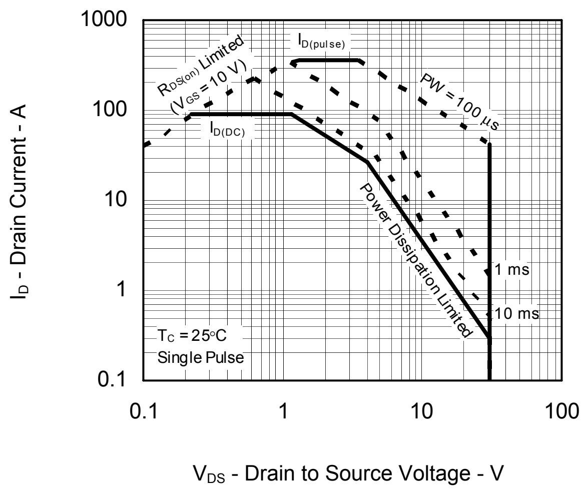
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



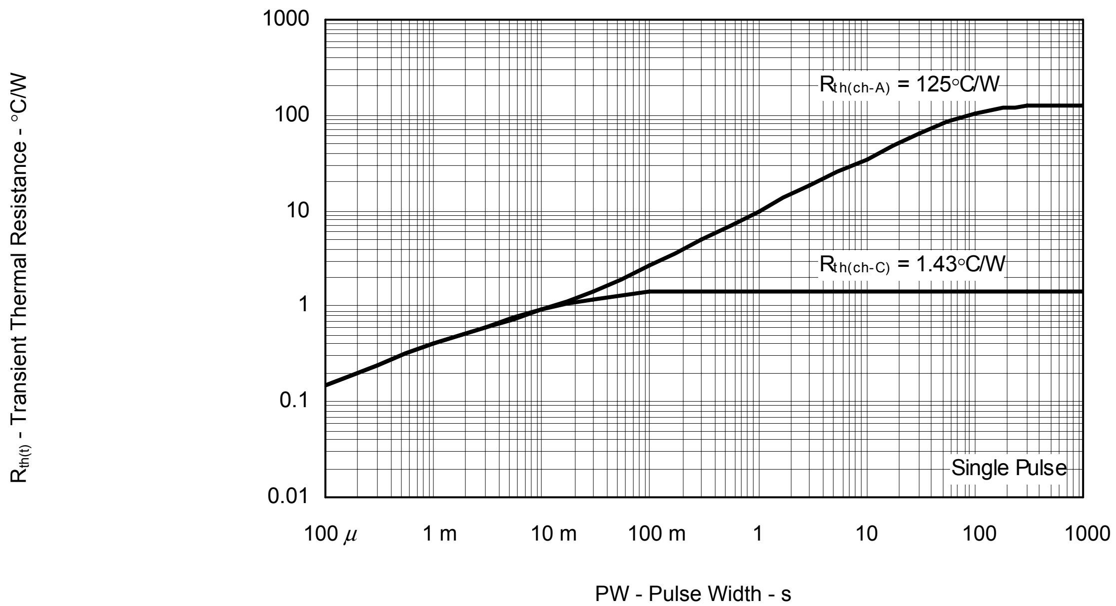
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



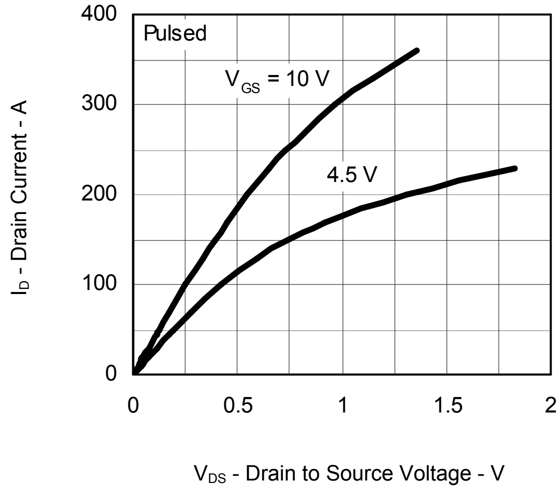
FORWARD BIAS SAFE OPERATING AREA



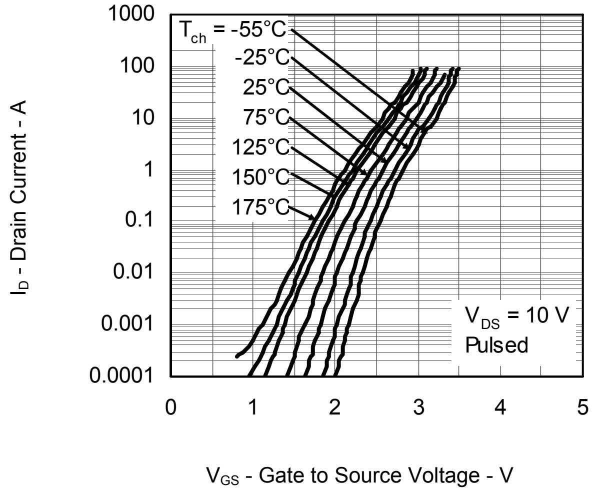
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



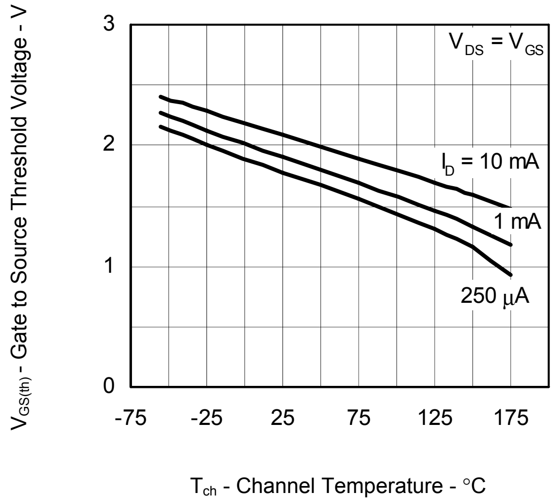
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



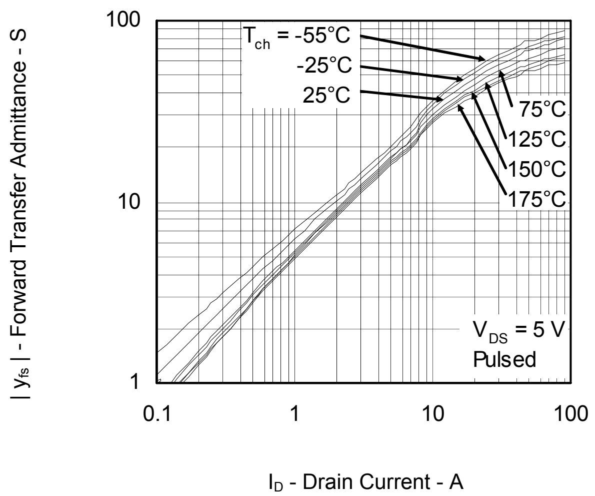
FORWARD TRANSFER CHARACTERISTICS



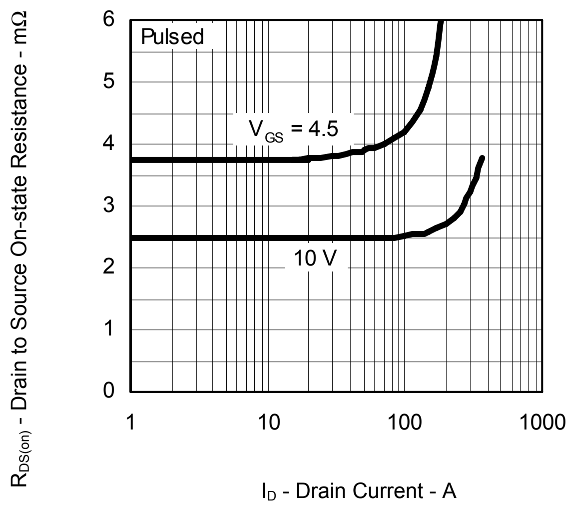
GATE TO SOURCE THRESHOLD VOLTAGE
vs. CHANNEL TEMPERATURE



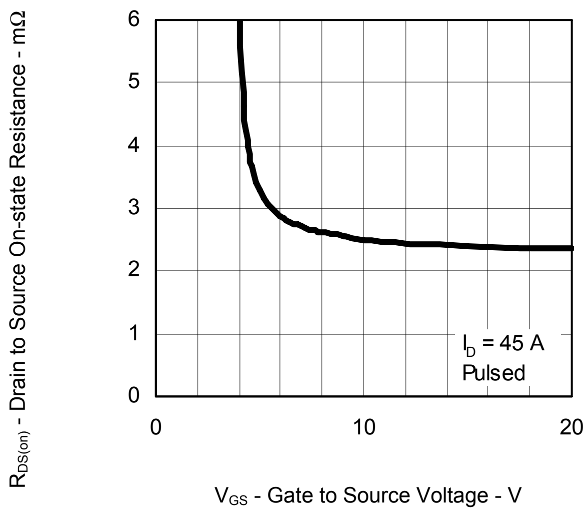
FORWARD TRANSFER ADMITTANCE vs. DRAIN
CURRENT



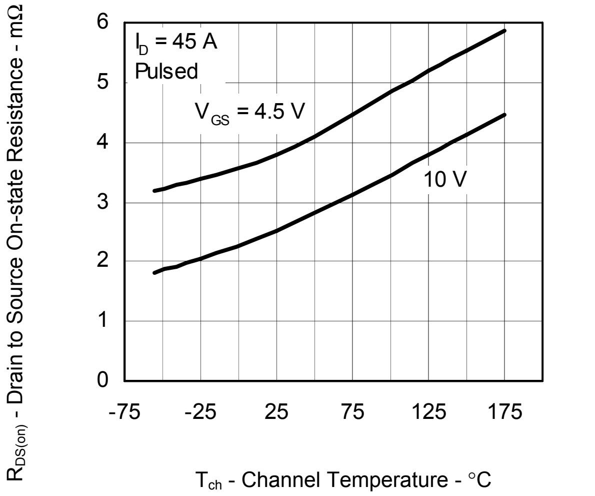
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



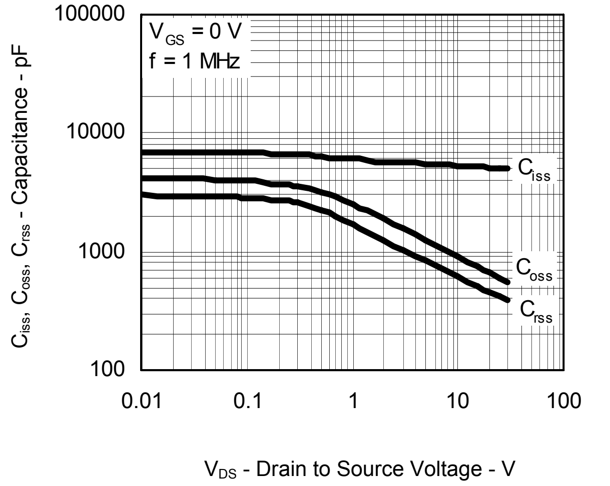
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



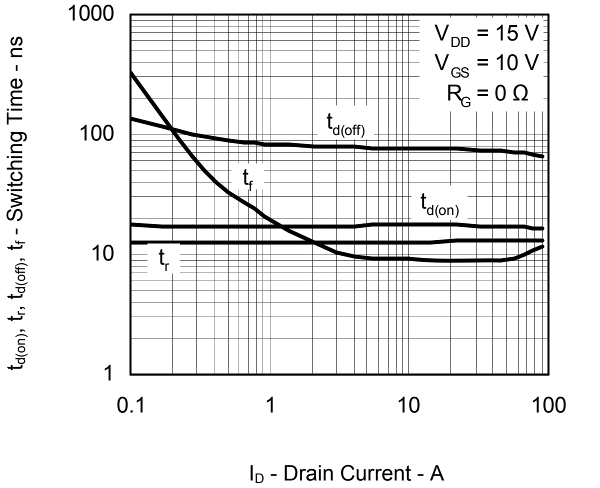
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



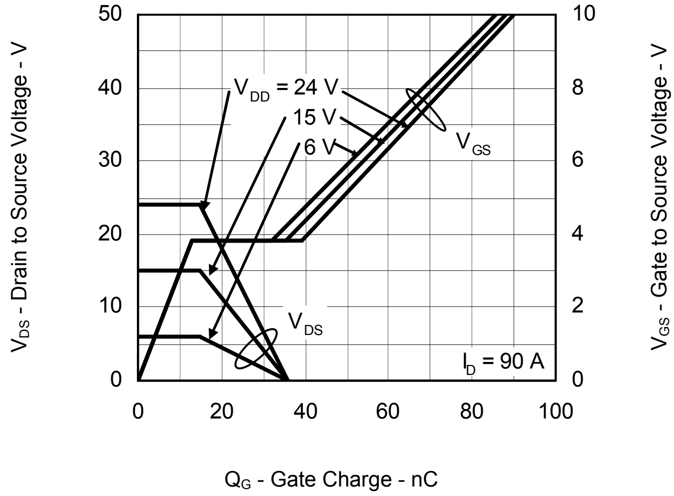
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



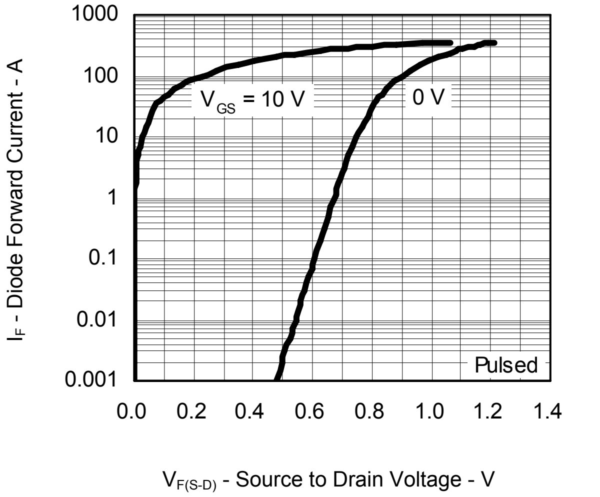
SWITCHING CHARACTERISTICS



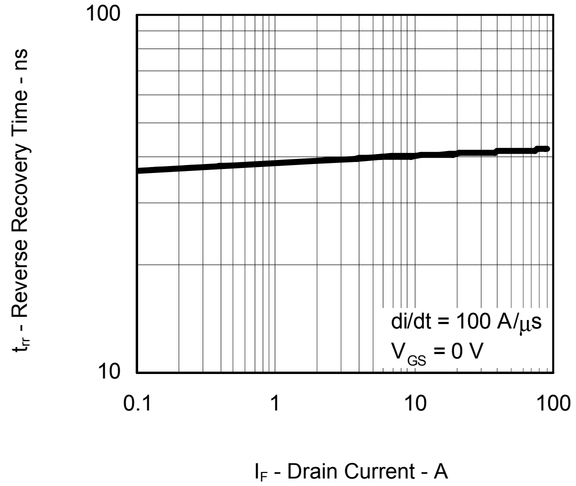
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

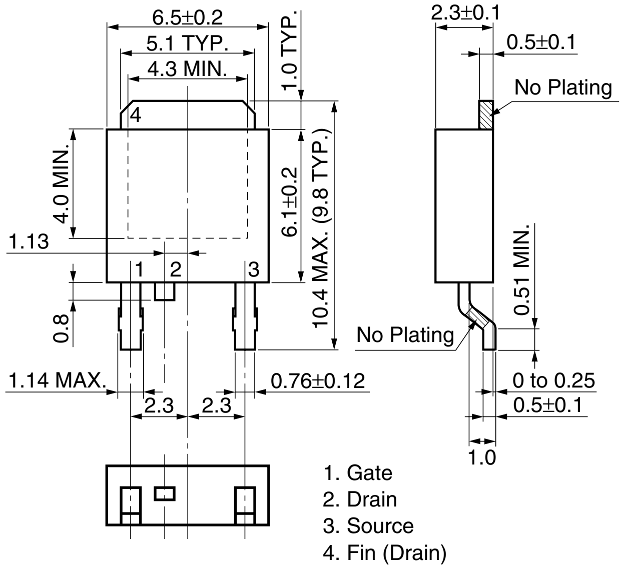


REVERSE RECOVERY TIME vs. DRAIN CURRENT

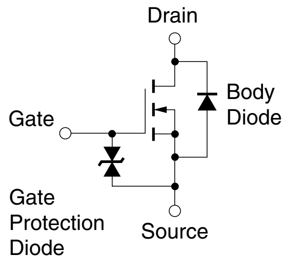


Package Drawings (Unit: mm)

TO-252 (MP-3ZP) (Mass: 0.27 g TYP.)



Equivalent Circuit



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

Revision History	NP90N03VLG

Rev.	Date	Description	
		Page	Summary
1.00	Sep 24, 2010	–	First Edition Issued

RENESAS

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