

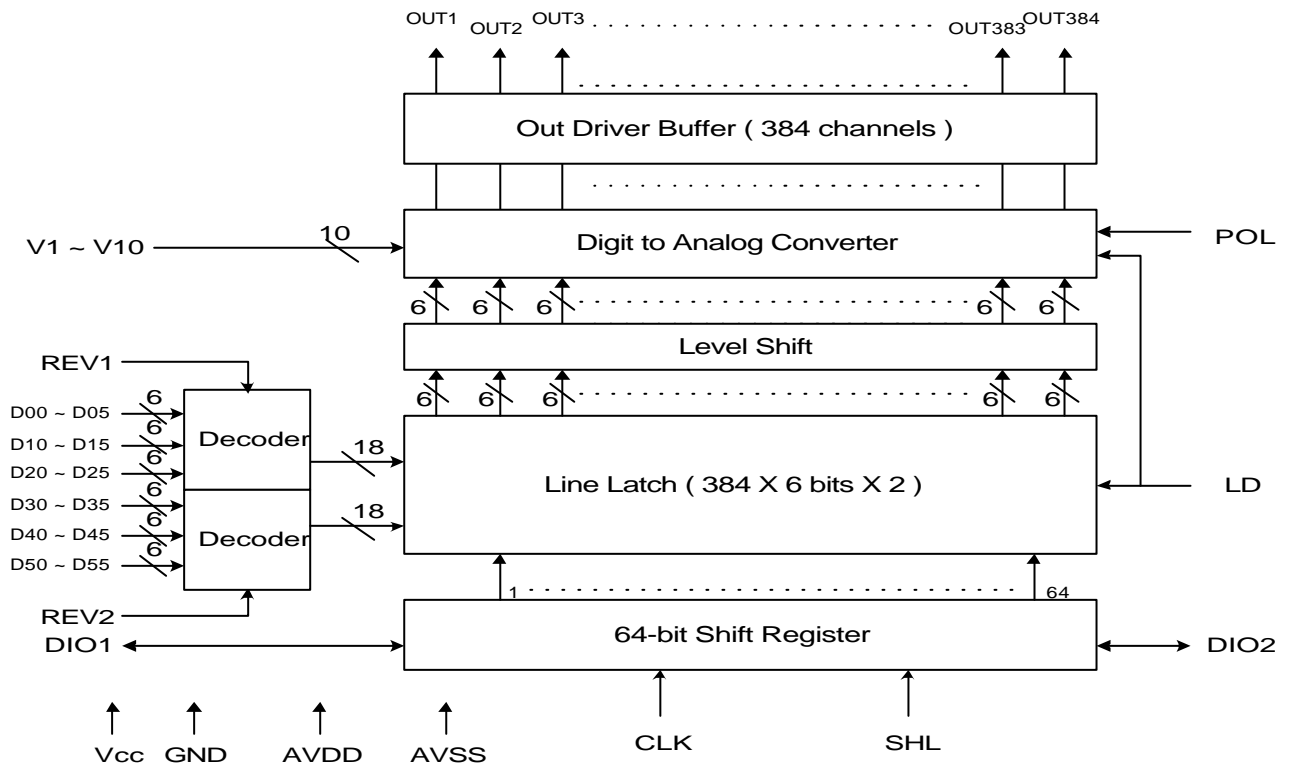
Features

- Output : 384 output channels
- 6-bit resolution /64 gray scale
- Dot inversion with polarity control
- V1 ~ V10 for adjusting Gamma correction
- Power of LCD driving voltage : 6.5 ~ 10V
- Output dynamic range : 0.1 ~ AVDD-0.1V
- Power consumption of analog circuit : 4mA
- Power for interface circuit : 2.7 ~ 3.6V
- Operating frequency : 55MHz
- Output deviation : 7 ~ 20mV
- Data inverting for reducing EMI
- Cascade function with bi-direction shift control
- CMOS silicon gate (p-type substrate)
- TCP package

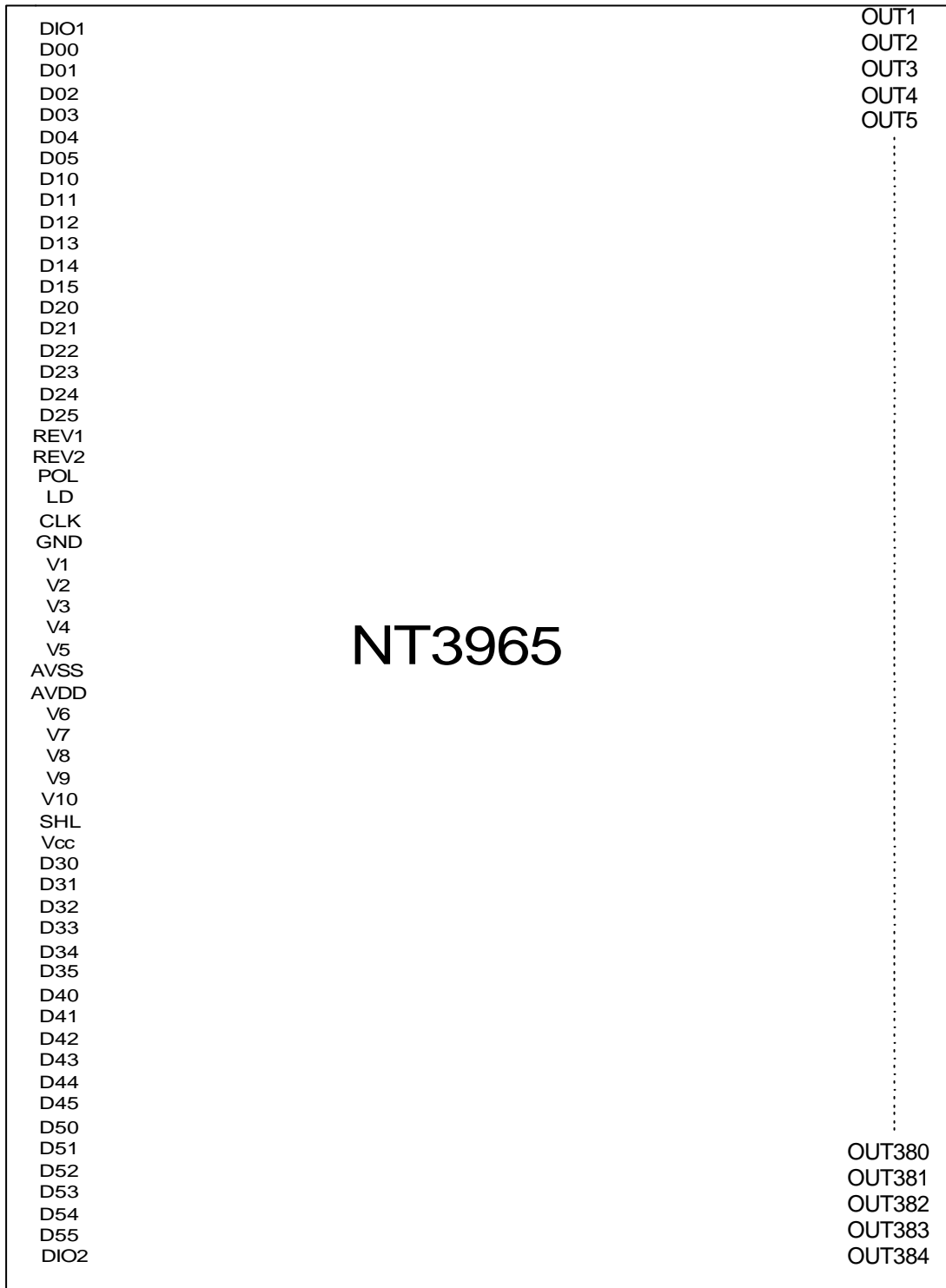
General Description

The NT3965 is a data driver IC for color TFT LCD panel, XGA and SXGA applications. For better performance, dot inversion and a wide range voltage output are designed in this chip and for reducing EMI, data inversion control is used. This chip supplies 10 sections of voltage-reference for Gamma correction.

Block diagram



NT3965 Pads configuration (Face down): This figure does not specify the TCP package.



Pin Description

Designation	I/O	Description												
D05 ~ D00 D15 ~ D10 D25 ~ D20 D35 ~ D30 D45 ~ D40 D55 ~ D50	I	Data input. For six 6-bit, 2 pixels, of color data (R, G, B) DX5 : MSB; DX0 : LSB												
REV1	I	Controls whether the D00~D25 data are inverted or not. When "REV1"=1 these data will be inverted. EX. "00" → "3F", "07" → "38", "15" → "2A," and so on.												
REV2	I	Controls whether the data of D30~D55 are inverted or not, same as REV1.												
CLK	I	Clock input; latching data onto the line latches at the rising edge.												
V1 ~ V10	I	Gamma correction reference voltage. The voltage of these pins must be AVSS < V10 < V9 < V8 < V7 < V6; V5 < V4 < V3 < V2 < V1 < AVDD												
OUT1 ~ OUT384	O	Output drive signals												
SHL	I	Selects left or right shift; SHL="1" : DIO1 → OUT1,2,3,4,5,6 → OUT7,8,9,10,11,12 → OUT379,380,381,382,383,384 = DIO2 SHL="0" : DIO1 = OUT1,2,3,4,5,6 ← OUT7,8,9,10,11,12 ← -- OUT379,380,381,382,383,384 ← DIO2 <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>SHL</th> <th>DIO1</th> <th>DIO2</th> <th>SHIFT</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>Input</td> <td>Output</td> <td>Right</td> </tr> <tr> <td>0</td> <td>Output</td> <td>Input</td> <td>Left</td> </tr> </tbody> </table>	SHL	DIO1	DIO2	SHIFT	1	Input	Output	Right	0	Output	Input	Left
SHL	DIO1	DIO2	SHIFT											
1	Input	Output	Right											
0	Output	Input	Left											
DIO1 DIO2	I/O	Start pulse signal input/output When SHL is applied high (SHL="1"), a start high-pulse on DIO1 is latched at the rising edge of the CLK. Then the data are latched serially onto internal latches at the rising edge of the CLK. After all line latches are filled with data, 64 clocks, a pulse is shifted out through the DIO2 pin at the rising edge of the CLK. This function can cascade two or more devices for dot-size expansion. In normal applications, the DIO2 signal of the first device is connected to the DIO1 of the second stage, and the DIO2 of the second one is connected to the DIO1 of the third, and so on, in a chain. In contrast, when SHL is applied low, a start pulse inputs on DIO2, and a pulse outputs through DIO1. *Remark: The input pulse-width of DIO1/2 may be over 1 clock-cycle.												
LD	I	Latches the polarity of outputs and switches the new data to outputs. 1. At the rising edge, latches the "POL" signal to control the polarity of the outputs. 2. This pin also controls the switch of the line registers that switches the new incoming data to outputs. *Remark: The LD may switch the new data to outputs at anytime even if the line data are not completely full.												
POL	I	Polarity selector for the dot-inversion control. Available at the rising edge of LD "POL" value is latched at the rising edge of "LD" to control the polarity of the even or odd outputs. "POL=1" represents that even outputs are of positive polarity with a voltage range from V1~V5, and odd outputs are of negative polarity with a voltage range from V6 to V10. On the other hand, if LD gets low level "POL", even outputs are of negative polarity and odd outputs are of positive polarity. POL=1: Even outputs range from V1 ~ V5 Odd outputs range from V6 ~ V10 POL=0: Even outputs range from V6 ~ V10 Odd outputs range from V1 ~ V5												
AVDD	I	Power supply for analog circuit												
AVSS	I	Ground pin for analog circuit												
Vcc	I	Power supply for digital circuit												
GND	I	Ground pin for digital circuit												

Power on/off sequence:

This IC is a high-voltage LCD driver, so it may be damaged by a large current flow when an incorrect power sequence is used. The recommended sequence should be: digital power (Vcc&GND) → logic signals → analog power (AVDD&AVSS) → Gamma correction reference voltage(V1~V10). Reverse this sequence to shut down, or turn off all signals and power simultaneously.

Relationship between the order of input data and output channels

(1) SHL="1", Start pulse from DIO1, shift right

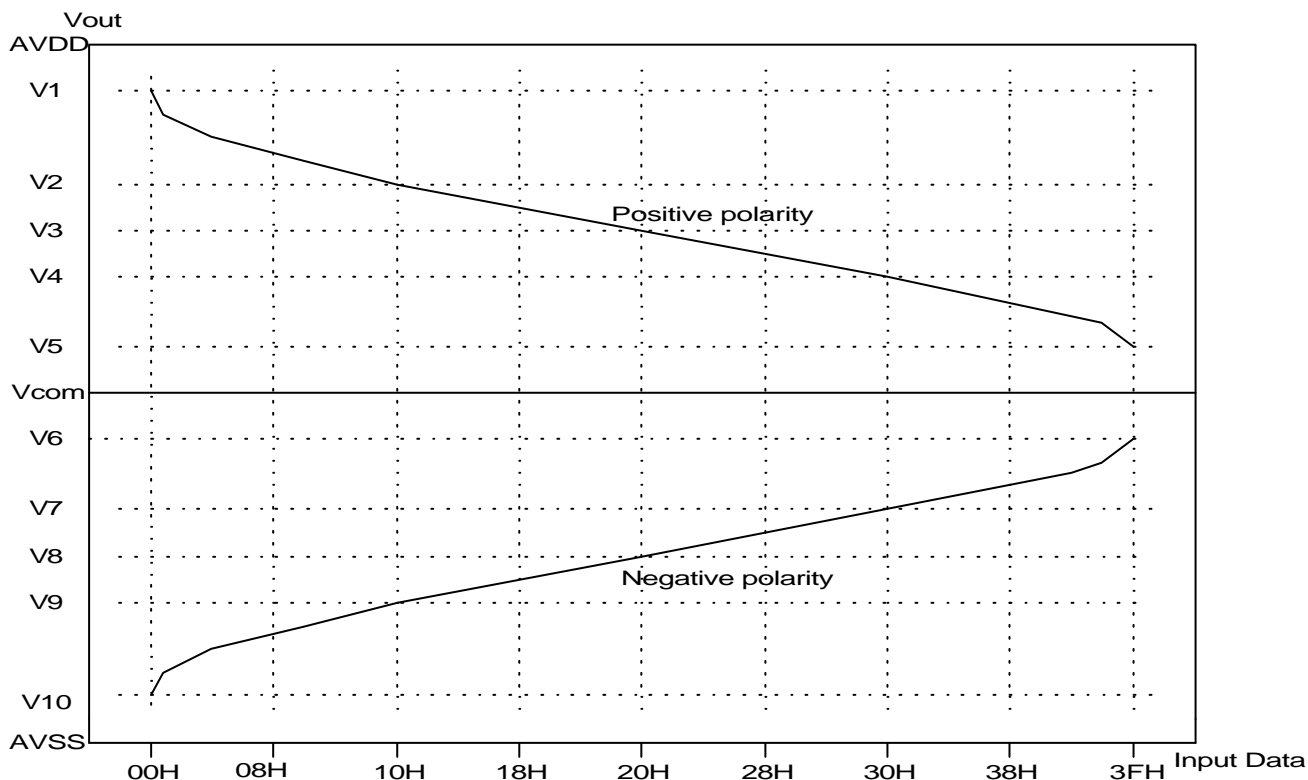
Output	OUT1	OUT2	OUT3	OUT4	OUT5	OUT6	---	OUT384
Order	First data						--→	Last data
Data	D05~D00	D15~D10	D25~D20	D35~D30	D45~D40	D55~D50	---	D55~D50

(2) SHL="0", Start pulse from DIO2, shift left

Output	OUT379	OUT380	OUT381	OUT382	OUT383	OUT384	---	OUT6
Order	First data						--→	Last data
Data	D05~D00	D15~D10	D25~D20	D35~D30	D45~D40	D55~D50	---	D55~D50

Relationship between input data and output voltage

The figure below shows the relationship between the input data and the output voltage with the polarity. The range of V1~V5 is for positive polarity, and V6 ~ V10 for negative polarity. Please refer to the following page to get the relative resistor value and voltage calculation method.

Gamma correction diagram


Remark: $AVDD-0.1 \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$; $V6 \geq V7 \geq V8 \geq V9 \geq V10 \geq AVSS+0.1V$

Gamma correction resistor ratio

	Name	Resistor	Name	Resistor	
V1, V10 →	R0	800	R32	100	← V3, V8
	R1	750	R33	100	
	R2	700	R34	100	
	R3	650	R35	100	
	R4	600	R36	100	
	R5	550	R37	100	
	R6	550	R38	100	
	R7	500	R39	100	
	R8	500	R40	100	
	R9	400	R41	100	
	R10	400	R42	100	
	R11	350	R43	100	
	R12	350	R44	100	
	R13	350	R45	100	
	R14	300	R46	100	
V2, V9 →	R15	300	R47	100	← V4, V7
	R16	300	R48	100	
	R17	250	R49	100	
	R18	250	R50	100	
	R19	250	R51	100	
	R20	200	R52	100	
	R21	200	R53	150	
	R22	200	R54	150	
	R23	150	R55	150	
	R24	150	R56	200	
	R25	150	R57	200	
	R26	150	R58	250	
	R27	100	R59	250	
	R28	100	R60	300	
	R29	100	R61	500	
	R30	100	R62	800	← V5, V6
V3, V8 →	R31	100			

Total impedance, $R_n=R_0 \sim R_{62}$, equals 15.85K

Output Voltage VS Input Data

Data	Output Voltage (Positive polarity)	Output Voltage (Negative polarity)
00H	V1	V10
01H	$V2 + (V1 - V2) \times 7250/8050$	$V10 + (V9 - V10) \times 800/8050$
02H	$V2 + (V1 - V2) \times 6500/8050$	$V10 + (V9 - V10) \times 1550/8050$
03H	$V2 + (V1 - V2) \times 5800/8050$	$V10 + (V9 - V10) \times 2250/8050$
04H	$V2 + (V1 - V2) \times 5150/8050$	$V10 + (V9 - V10) \times 2900/8050$
05H	$V2 + (V1 - V2) \times 4550/8050$	$V10 + (V9 - V10) \times 3500/8050$
06H	$V2 + (V1 - V2) \times 4000/8050$	$V10 + (V9 - V10) \times 4050/8050$
07H	$V2 + (V1 - V2) \times 3450/8050$	$V10 + (V9 - V10) \times 4600/8050$
08H	$V2 + (V1 - V2) \times 2950/8050$	$V10 + (V9 - V10) \times 5100/8050$
09H	$V2 + (V1 - V2) \times 2450/8050$	$V10 + (V9 - V10) \times 5600/8050$
0AH	$V2 + (V1 - V2) \times 2050/8050$	$V10 + (V9 - V10) \times 6000/8050$
0BH	$V2 + (V1 - V2) \times 1650/8050$	$V10 + (V9 - V10) \times 6400/8050$
0CH	$V2 + (V1 - V2) \times 1300/8050$	$V10 + (V9 - V10) \times 6750/8050$
0DH	$V2 + (V1 - V2) \times 950/8050$	$V10 + (V9 - V10) \times 7100/8050$
0EH	$V2 + (V1 - V2) \times 600/8050$	$V10 + (V9 - V10) \times 7450/8050$
0FH	$V2 + (V1 - V2) \times 300/8050$	$V10 + (V9 - V10) \times 7750/8050$
10H	V2	V9
11H	$V3 + (V2 - V3) \times 2450/2750$	$V9 + (V8 - V9) \times 300/2750$
12H	$V3 + (V2 - V3) \times 2200/2750$	$V9 + (V8 - V9) \times 550/2750$
13H	$V3 + (V2 - V3) \times 1950/2750$	$V9 + (V8 - V9) \times 800/2750$
14H	$V3 + (V2 - V3) \times 1700/2750$	$V9 + (V8 - V9) \times 1050/2750$
15H	$V3 + (V2 - V3) \times 1500/2750$	$V9 + (V8 - V9) \times 1250/2750$
16H	$V3 + (V2 - V3) \times 1300/2750$	$V9 + (V8 - V9) \times 1450/2750$
17H	$V3 + (V2 - V3) \times 1100/2750$	$V9 + (V8 - V9) \times 1650/2750$
18H	$V3 + (V2 - V3) \times 950/2750$	$V9 + (V8 - V9) \times 1800/2750$
19H	$V3 + (V2 - V3) \times 800/2750$	$V9 + (V8 - V9) \times 1950/2750$
1AH	$V3 + (V2 - V3) \times 650/2750$	$V9 + (V8 - V9) \times 2100/2750$
1BH	$V3 + (V2 - V3) \times 500/2750$	$V9 + (V8 - V9) \times 2250/2750$
1CH	$V3 + (V2 - V3) \times 400/2750$	$V9 + (V8 - V9) \times 2350/2750$
1DH	$V3 + (V2 - V3) \times 300/2750$	$V9 + (V8 - V9) \times 2450/2750$
1EH	$V3 + (V2 - V3) \times 200/2750$	$V9 + (V8 - V9) \times 2550/2750$
1FH	$V3 + (V2 - V3) \times 100/2750$	$V9 + (V8 - V9) \times 2650/2750$
20H	V3	V8
21H	$V4 + (V3 - V4) \times 1500/1600$	$V8 + (V7 - V8) \times 100/1600$
22H	$V4 + (V3 - V4) \times 1400/1600$	$V8 + (V7 - V8) \times 200/1600$
23H	$V4 + (V3 - V4) \times 1300/1600$	$V8 + (V7 - V8) \times 300/1600$
24H	$V4 + (V3 - V4) \times 1200/1600$	$V8 + (V7 - V8) \times 400/1600$
25H	$V4 + (V3 - V4) \times 1100/1600$	$V8 + (V7 - V8) \times 500/1600$
26H	$V4 + (V3 - V4) \times 1000/1600$	$V8 + (V7 - V8) \times 600/1600$
27H	$V4 + (V3 - V4) \times 900/1600$	$V8 + (V7 - V8) \times 700/1600$
28H	$V4 + (V3 - V4) \times 800/1600$	$V8 + (V7 - V8) \times 800/1600$

29H	$V4 + (V3 - V4) \times 700/1600$	$V8 + (V7 - V8) \times 900/1600$
2AH	$V4 + (V3 - V4) \times 600/1600$	$V8 + (V7 - V8) \times 1000/1600$
2BH	$V4 + (V3 - V4) \times 500/1600$	$V8 + (V7 - V8) \times 1100/1600$
2CH	$V4 + (V3 - V4) \times 400/1600$	$V8 + (V7 - V8) \times 1200/1600$
2DH	$V4 + (V3 - V4) \times 300/1600$	$V8 + (V7 - V8) \times 1300/1600$
2EH	$V4 + (V3 - V4) \times 200/1600$	$V8 + (V7 - V8) \times 1400/1600$
2FH	$V4 + (V3 - V4) \times 100/1600$	$V8 + (V7 - V8) \times 1500/1600$

Output Voltage VS Input Data (continued)

Data	Output Voltage (Positive polarity)	Output Voltage (Negative polarity)
30H	V4	V7
31H	$V5 + (V4 - V5) \times 3350/3450$	$V7 + (V6 - V7) \times 100/3450$
32H	$V5 + (V4 - V5) \times 3250/3450$	$V7 + (V6 - V7) \times 200/3450$
33H	$V5 + (V4 - V5) \times 3150/3450$	$V7 + (V6 - V7) \times 300/3450$
34H	$V5 + (V4 - V5) \times 3050/3450$	$V7 + (V6 - V7) \times 400/3450$
35H	$V5 + (V4 - V5) \times 2950/3450$	$V7 + (V6 - V7) \times 500/3450$
36H	$V5 + (V4 - V5) \times 2800/3450$	$V7 + (V6 - V7) \times 650/3450$
37H	$V5 + (V4 - V5) \times 2650/3450$	$V7 + (V6 - V7) \times 800/3450$
38H	$V5 + (V4 - V5) \times 2500/3450$	$V7 + (V6 - V7) \times 950/3450$
39H	$V5 + (V4 - V5) \times 2300/3450$	$V7 + (V6 - V7) \times 1150/3450$
3AH	$V5 + (V4 - V5) \times 2100/3450$	$V7 + (V6 - V7) \times 1350/3450$
3BH	$V5 + (V4 - V5) \times 1850/3450$	$V7 + (V6 - V7) \times 1600/3450$
3CH	$V5 + (V4 - V5) \times 1600/3450$	$V7 + (V6 - V7) \times 1850/3450$
3DH	$V5 + (V4 - V5) \times 1300/3450$	$V7 + (V6 - V7) \times 2150/3450$
3EH	$V5 + (V4 - V5) \times 800/3450$	$V7 + (V6 - V7) \times 2650/3450$
3FH	V5	V6

Absolute Maximum Ratings*

Digital supply voltage, Vcc	-0.5V to 5V
Analog supply voltage, AVDD	-0.5V to +12V
Supply voltage, V1~ V5	0.4AVDD ~AVDD+0.3
Supply voltage, V6 ~ V10	-0.3 ~ 0.6AVDD
Digital input voltage	-0.5V to Vcc+0.5V
Output voltage, DIO1 & DIO2	-0.5V to Vcc+0.5V
Output voltage, OUT1~OUT384	-0.5V to AVDD+0.5V
Storage temperature	-55°C to 125°C
Operating temperature	-10°C to 75°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or under any other conditions above those indicated in the operational sections of this specification are not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics (V_{CC} =2.7~3.6V , AV_{DD}=10V, AV_{SS}=GND=0V, T_A=-10°C~75°C)

(For the digital circuit)

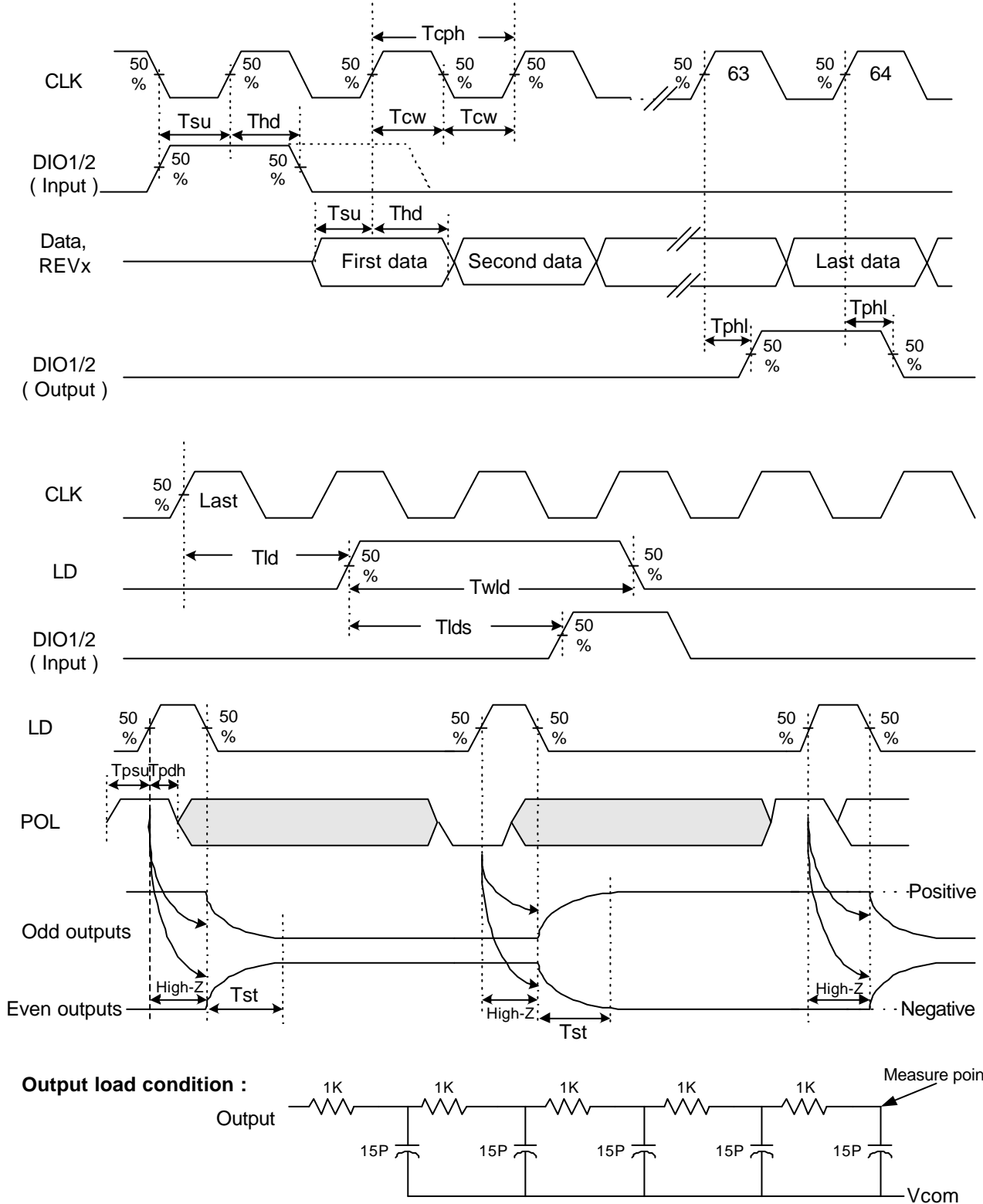
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	Vcc	2.7	3.3	3.6	V	Digital power
Low Level Input Voltage	Vil	0	-	0.3xVcc	V	For the digital circuit
High Level Input Voltage	Vih	0.7xVcc	-	Vcc	V	For the digital circuit
High Level Output Voltage	Voh	Vcc-0.4	-	-	V	DIO1, DIO2, Ioh=1mA
Low Level Output Voltage	Vol	GND	-	GND+0.4	V	DIO1, DIO2, Iol=-1mA
Input Leakage Current	Ii	-	-	±1	A	For the digital circuit
Digital Stand-by Current	Ist	-	10	50	A	All operating is stopped
Digital Operating Current	Icc	-	1.5	3	mA	Fclk=45 MHz, FLD=50KHz
Input Loading 1	Ci1	-	-	6	pF	DIO1/2, V1~V10 exclusive
Input Loading 2	Ci2	-	-	10	pF	DIO1/2

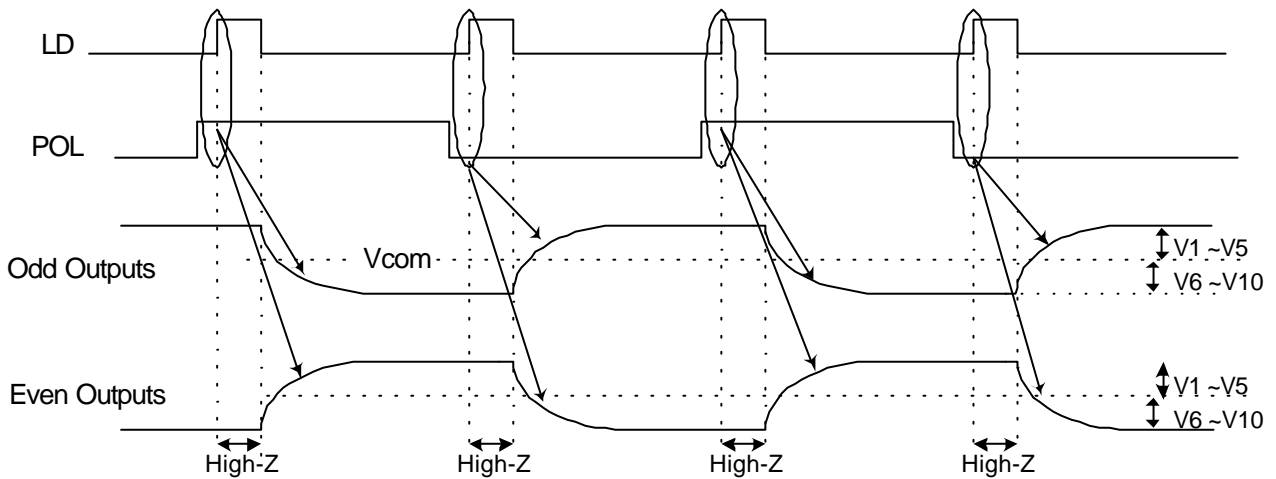
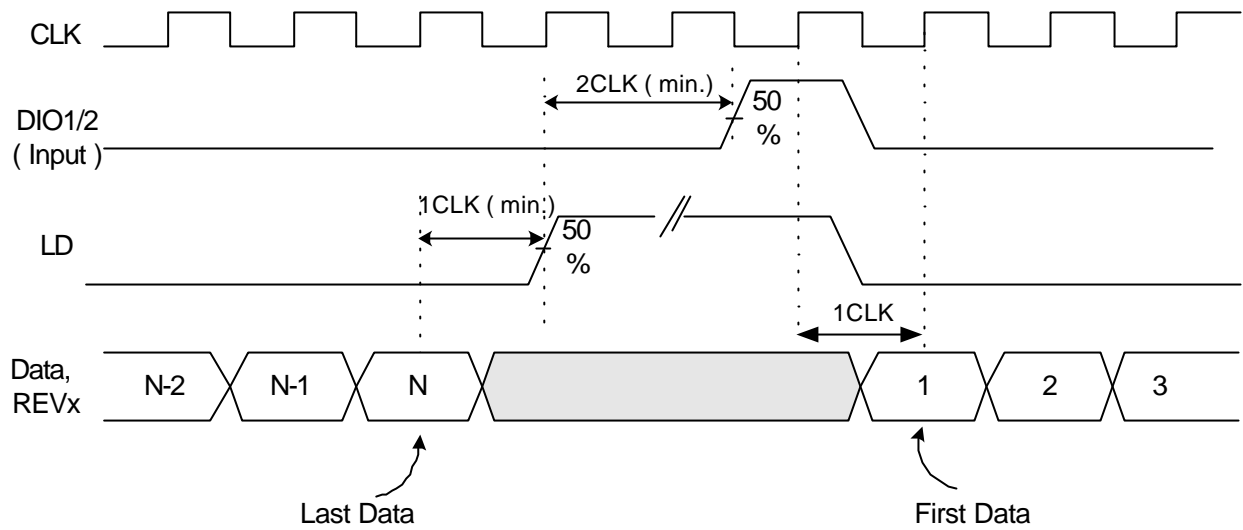
(For the analog circuit)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	AVDD	6.5	8.4	10	V	For the analog circuit power
Input level of V1 ~ V5	Vref	0.4AVDD	-	AVDD-0.1	V	Gamma correction voltage
Input level of V6 ~ V10	Vref	0.1	-	0.6AVDD	V	Gamma correction voltage
Voltage Output Swing Deviation between Pins	Vdp	-30	±20	+30	mV	Vo=0.1V ~ 0.8V & AVDD-0.8 ~ AVDD-0.1V
		-25	±10	+25	mV	Vo=0.8V ~ 1.2V & AVDD-1.2 ~ AVDD-0.8V
		-10	±7	+10	mV	Vo=1.2V ~ AVDD-1.2V
Output Voltage deviation	Vod	-20	-	+20	mV	
Voltage Output Offset between Chips	Voc	-10	-	+10	mV	
Dynamic Range of Output	Vdr	0.1	-	AVDD-0.1	V	OUT1 ~ OUT384
Sinking Current of Outputs	IOL	-	-180	-150	A	OUT1 ~ OUT384; Vo=0.1V V.S 1.0V AVDD=10V
Driving Current of Outputs	IOH	150	200	-	A	OUT1 ~ OUT384; Vo=9.9V V.S 9V AVDD=10V
Impedance of Gamma Correction	Ri	0.8*Rn	Rn	1.4*Rn	ohm	Rn=15850 ohm, from V1~V5 & V6~V10
Analog Stand-by Current	Isc	-	4	5.5	mA	No load, Fclk=33MHz, FLD=50KHz AVDD=8.4V, OUT=4.2V
Analog Operating Current	Ioc	-	7	10	mA	No load, Fclk=33MHz, FLD=50KHz AVDD=8.4V, V1=8V, V10=0.2V, Black-white line

AC Electrical Characteristics ($V_{CC}=2.7\sim 3.3V$, $AV_{DD}=6.5\sim 10V$, $AV_{SS}=GND=0V$, $T_A=-10\sim 75^{\circ}C$)

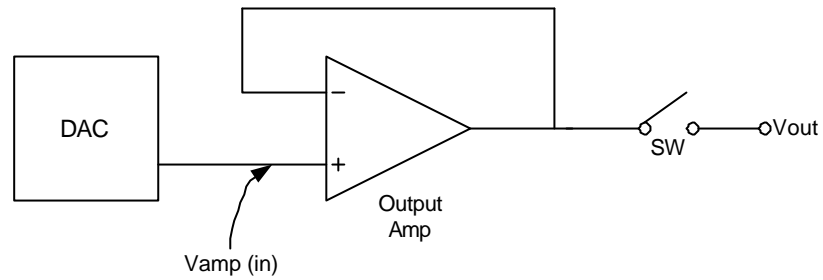
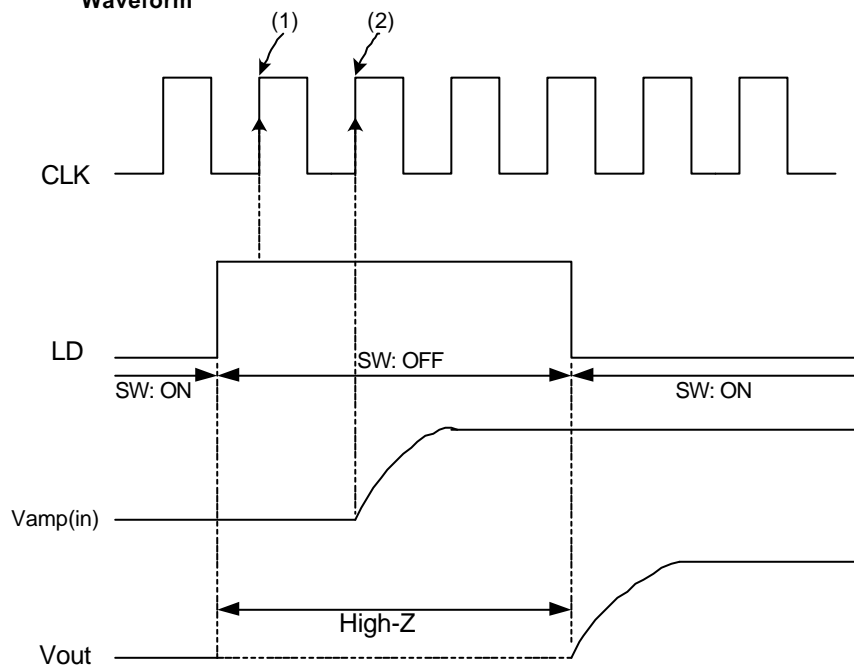
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
CLK frequency	Fclk	-	45	55	MHz	$V_{CC}=3.0V\sim 3.6V$
CLK frequency	Fclk1	-	-	45	MHz	$V_{CC}=2.7V\sim 3.0V$
CLK pulse width	Tcw	6	-	-	ns	
Data set-up time	Tsu	4	-	-	ns	D00 ~ D55, REVx and DIO1/2 to CLK
Data hold time	Thd	2	-	-	ns	D00 ~ D55, REVx and DIO1/2 to CLK
Propagation delay of DIO2/1	Tphl	6	10	15	ns	CL=25pF (Output)
Time that the last data to LD	Tld	1	-	-	Tcph	
Pulse width of LD	Twld	2	-	-	Tcph	
Time that LD to DIO1/2	Tlds	2	-	-	Tcph	
POL set-up time	Tpsu	6	-	-	ns	POL to LD
POL hold time	Tphd	6	-	-	ns	POL to LD
Output stable time	Tst	-	-	5	us	90% target voltage ,CL=75pF, R=5K ohm,AVDD=8.4V 6 bit precision ,CL=75pF, R=5K ohm,AVDD=8.4V
		-	-	8		
Output loading	CL	-	-	150	pF	For OUT1 ~ OUT384

Timing Diagram


Function operation


Application notice: relationship between LD, CLK, and output waveform

The output voltage is written to the LCD panel, and synchronized with the LD falling edge.

Output Circuit Block Diagram

Output Circuit Timing Waveform


- Remarks**
1. LD = "L" : SW = ON
LD = "H" : SW = OFF
 2. LD = "H" is acknowledged at timing (1)
 3. The display data latch is completed at timing (2) and the input voltage (Vamp(in) : gray-scale level voltage) of the output amplifier changes.