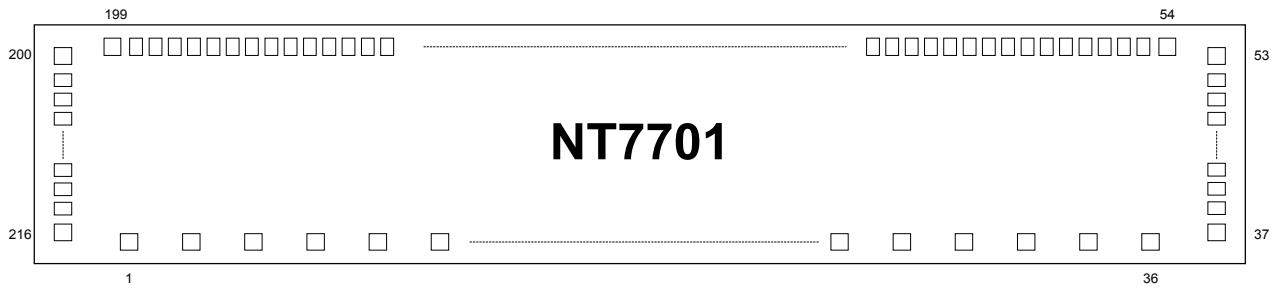
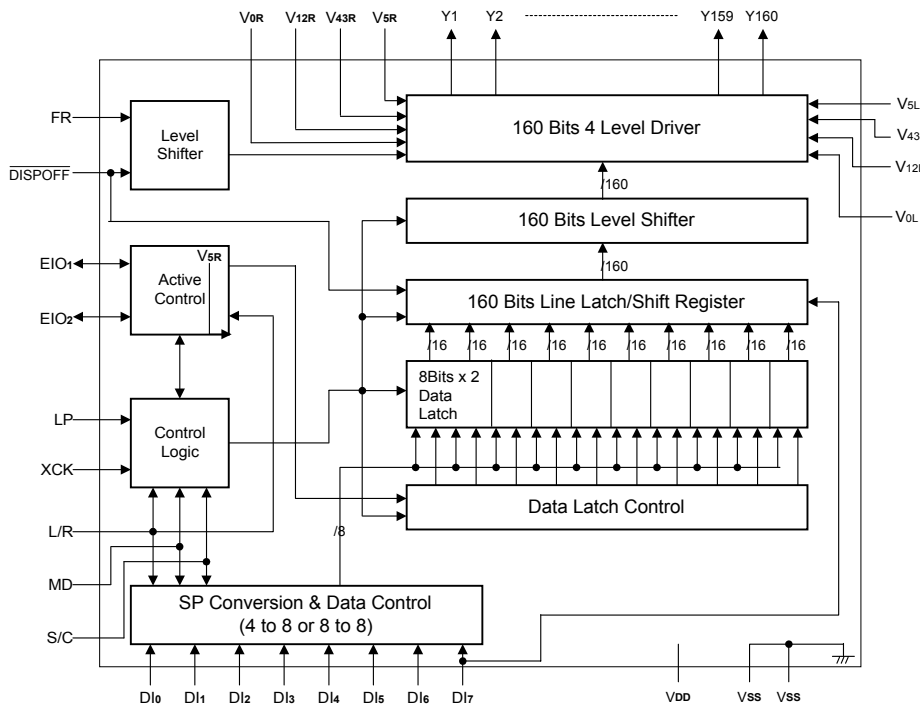


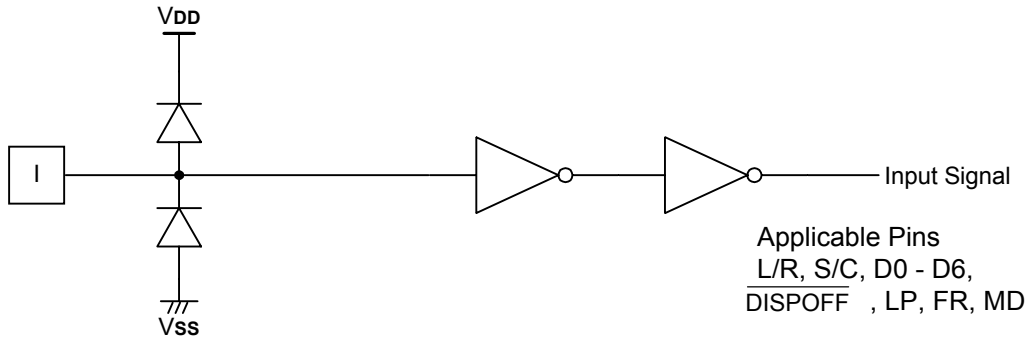
Pad Configuration

Block Diagram


Pin Description

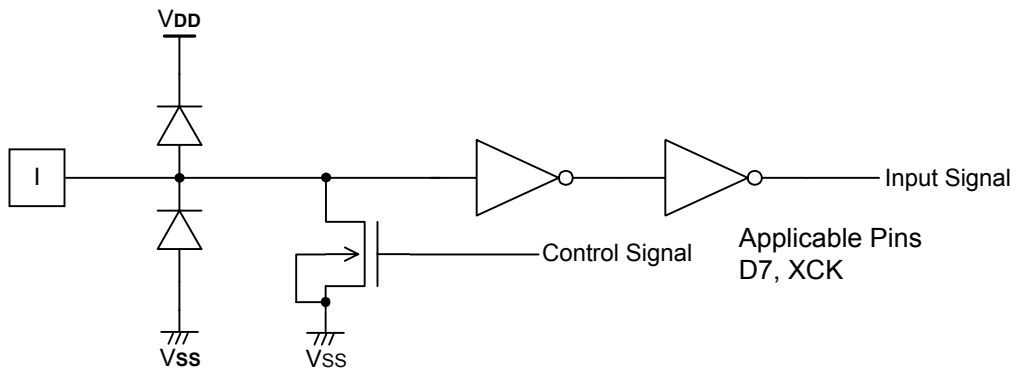
Pin No.	Designation	I/O	Description
1	V _{0L}	P	Power supply for LCD driver
2	V _{12L}	P	Power supply for LCD driver
3	V _{43L}	P	Power supply for LCD driver
4	V _{5L}	P	Power supply for LCD driver
5	V _{SS}	P	Ground (0V), these two pads must be connected to each other
6	L/R	I	Display data shift direction selection
7	V _{DD}	P	Power supply for the logic system (+2.5 to +5.5V)
8	S/C	I	Segment mode / common mode selection
9	EIO ₂	I/O	Input / output for chip select or data of shift register
10 - 16	D ₀ - D ₆	I	Display data input for segment mode
17	D ₇	I	Display data input for Segment mode / Dual mode data input
18	XCK	I	Display data shift clock input for segment mode
19	$\overline{\text{DISPOFF}}$	I	Control input for deselect output level
20	LP	I	Latch pulse input/shift clock input for the shift register
21	EIO ₁	I/O	Input / output for chip select or data of the shift register
22	FR	I	AC-converting signal input for LCD driver waveform
23	MD	I	Mode selection input
24	TEST1	I	Test pin, no connection for user
25	TEST2	I	Test pin, no connection for user
26	V _{SS}	P	Ground (0V), these two pads must be connected to each other
27	V _{5R}	P	Power supply for LCD driver
28	V _{43R}	P	Power supply for LCD driver
29	V _{12R}	P	Power supply for LCD driver
30	V _{0R}	P	Power supply for LCD driver
31 - 190	Y ₁ - Y ₁₆₀	O	LCD driver output

Pad Description

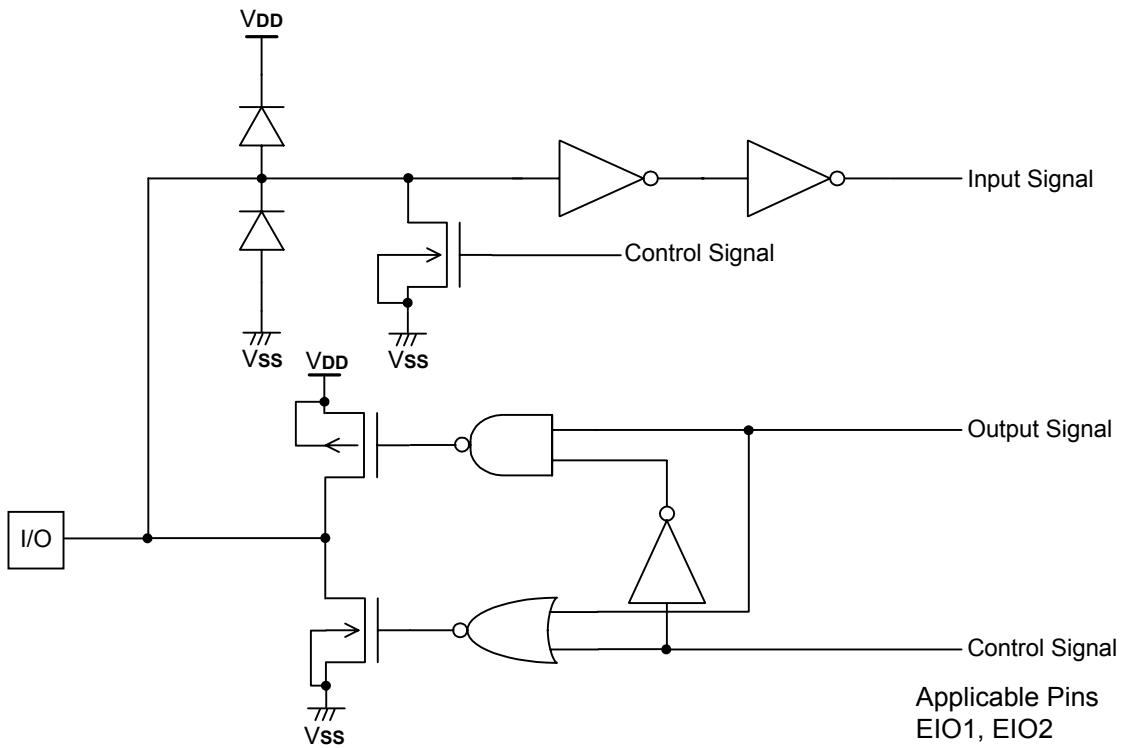
Pad No.	Designation	I/O	Description
1, 2	L/R	I	Display data shift direction selection
3, 4	VDD	P	Power supply for the logic system (+2.5 to + 5.5V)
5, 6	S/C	I	Segment mode/common mode selection
7, 8	EIO2	I/O	Input/output for chip select or data of shift register
9,10 - 21, 22	D0 - D6	I	Display data input for segment mode
23, 24	D7	I	Display data input for Segment mode / Dual mode data input
25, 26	XCK	I	Display data shift clock input for segment mode
27, 28	$\overline{\text{DISPOFF}}$	I	Control input for deselect output level
29, 30	LP	I	Latch pulse input / shift clock input for the shift register
31, 32	EIO1	I/O	Input/output for chip select or data of the shift register
33, 34	FR	I	AC-converting signal input for LCD driver waveform
35, 36	MD	I	Mode selection input
37, 38,	VSS	P	Ground (0V), these two pads must be connected to each other
39, 40	V5R	P	Power supply for LCD driver
41, 42	V43R	P	Power supply for LCD driver
43, 44	V12R	P	Power supply for LCD driver
45, 46	V0R	P	Power supply for LCD driver
47 - 206	Y1 - Y160	O	LCD driver output
207, 208	V0L	P	Power supply for LCD driver
209, 210	V12L	P	Power supply for LCD driver
211, 212	V43L	P	Power supply for LCD driver
213, 214	V5L	P	Power supply for LCD driver
215, 216	VSS	P	Ground (0V), these two pads must be connected to each other

Input / Output Circuits


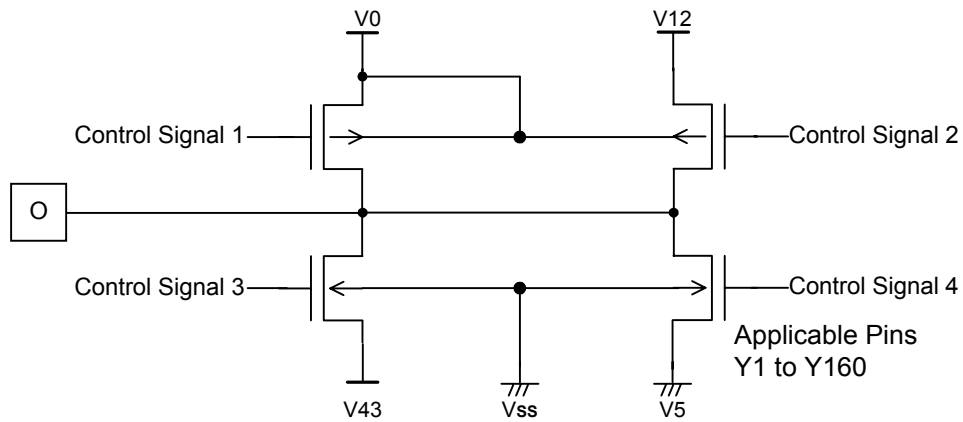
Input Circuit (1)



Input Circuit (2)



Input / Output Circuit



LCD Driver Output circuit

Pad Description

Segment mode

Symbol	Function
VDD	Logic system power supply pin connects to +2.5 to +5.5V
VSS	Ground pin connects to 0V
VOR, VOL V12R, V12L V43R, V43L V5R, V5L	Power supply pin for LCD driver voltage bias <ul style="list-style-type: none"> ● Normally, the bias voltage used is set by a resistor divider ● Ensure that the voltages are set such that $V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$ ● To further reduce the differences between the output waveforms of the LCD driver output pins Y1 and Y160, externally connect ViR and ViL (I = 0, 12, 43)
D0 - D7	Input pin for display data <ul style="list-style-type: none"> ● In 4-bit parallel input mode, input data into the 4 pins D0 - D3. Connect D4 - D7 to VSS or VDD ● In 8-bit parallel input mode, input data into the 8 pins D0 - D7
XCK	Clock input pin for taking display data <ul style="list-style-type: none"> ● Data is read on the falling edge of the clock pulse
LP	Latch pulse input pin for display data <ul style="list-style-type: none"> ● Data is latched on the falling edge of the clock pulse
L/R	Direction selection pin for reading display data <ul style="list-style-type: none"> ● When set to VSS level "L", data is read sequentially from Y160 to Y1 ● When set to VDD level "H", data is read sequentially from Y1 to Y160
$\overline{\text{DISPOFF}}$	Control input pin for output deselect level <ul style="list-style-type: none"> ● The input signal is level-shifted from logic voltage level to LCD driver voltage level, and controls LCD driver circuit ● When set to VSS level "L", the LCD driver output pins (Y1 - Y160) are set to level V5 ● While $\overline{\text{DISPOFF}}$ is set to "L", the contents of the line latch are reset, but the display data in the data latch are read regardless of the condition of $\overline{\text{DISPOFF}}$. When the $\overline{\text{DISPOFF}}$ function is canceled, the driver outputs deselect level (V12 or V43), then outputs the contents of the data latch onto the next falling edge of the LP. <p>That time, if $\overline{\text{DISPOFF}}$ removal time can not keep regulation what is shown AC characteristics, can not output the reading data correctly</p>
FR	AC signal input for LCD driving waveform <ul style="list-style-type: none"> ● The input signal is level-shifted from the logic voltage level to the driver voltage level, and controls LCD driver circuit ● Normally inputs a frame inversion signal <p>The LCD driver output pin's output voltage level can be set to the line latch output signal and the FR signal</p>
MD	Mode selection pin <ul style="list-style-type: none"> ● When set to VSS level "L", 4-bit parallel input mode is set ● When set to VDD level "H", 8-bit parallel input mode is set

Segment mode continued

Symbol	Function
S/C	Segment mode/common mode selection pin <ul style="list-style-type: none"> ● When set to VDD level "H", segment mode is set. ● When set to VSS level "L", common mode is set.
EIO1, EIO2	Input/output pin for chip selection <ul style="list-style-type: none"> ● When L/R input is at VSS level "L", EIO1 is set for output, and EIO2 is set for input. ● When L/R input is at VDD level "H", EIO1 is set for input, and EIO2 is set for output. ● During output, it is set to "H" while LP* XCK is "H" and after 160-bits of data have been read, it is set to "L" for one cycle (from falling edge to falling edge of XCK), after which it returns to "H" ● During input, after the LP signal is input, the chip is selected while EI is set to "L". After 160-bits of data have been read, the chip is deselected
Y1 - Y160	LCD driver output pins These corresponding directly to each bit of the data latch, one level (V0, V12, V43, or V5) is selected and output

Common mode

Symbol	Function
VDD	Logic system power supply pin connects to +2.5 to +5.5V
VSS	Ground pin connects to 0V
V0R, V0L V12R, V12L V43R, V43L V5R, V5L	Power supply pin for LCD driver voltage bias. <ul style="list-style-type: none"> ● Normally, the bias voltage used is set by a resistor divider ● Ensure that the voltages are set such that $VSS \leq V5 < V43 < V12 < V0$ ● To further reduce the differences between the output waveforms of the LCD driver output pins Y1 and Y160, externally connect ViR and ViL (I = 0, 12, 43)
EIO1	Bi-directional shift register shift data input/output pin <ul style="list-style-type: none"> ● Is an Output pin when L/R is at VSS level "L" and an input pin when L/R is at VDD level "H" ● When EIO1 is used as an input pin, it will be pulled-down ● When EIO1 is used as an output pin, it won't be pulled-down
EIO2	Bi-directional shift register shift data input/output pin <ul style="list-style-type: none"> ● Is an Input pin when L/R is at VSS level "L" and an output pin when L/R is at VDD level "H" ● When EIO2 is used as an input pin, it will be pulled-down ● When EIO2 is used as an output pin, it won't be pulled-down
LP	Bi-directional shift register shift clock pulse input pin <ul style="list-style-type: none"> ● Data is shifted on the falling edge of the clock pulse
L/R	Bi-directional shift register shift direction selection pin <ul style="list-style-type: none"> ● Data is shifted from Y160 to Y1 when it is set to VSS level "L", and data is shifted from Y1 to Y160 when it is set to VDD level "H"

Common mode continued

Symbol	Function
$\overline{\text{DISPOFF}}$	Control input pin for output deselect level <ul style="list-style-type: none"> ● The input signal is level-shifted from the logic voltage level to the LCD driver voltage level and it controls the LCD driver circuit ● When set to V_{SS} level "L", the LCD driver output pins (Y1 - Y160) are set to level V5 ● While set to "L", the contents of the shift register are reset and not reading data. When the $\overline{\text{DISPOFF}}$ function is canceled, the driver outputs deselect level (V12 or V34), and the shift data is read on the falling edge of the LP. That time, if $\overline{\text{DISPOFF}}$ removal time can not keep regulation what is shown AC characteristics, the shift data is not reading correctly
FR	AC signal input for LCD driving waveform <ul style="list-style-type: none"> ● The input signal is level-shifted from the logic voltage level to the LCD driver voltage level, and controls the LCD driver circuit ● Normally, inputs a frame inversion signal The LCD driver output pin's output voltage level can be set using the shift register output signal and the FR signal
MD	Mode selection pin <ul style="list-style-type: none"> ● When set to V_{SS} level "L", Single Mode operation is selected. When set to V_{DD} level "H", Dual Mode operation is selected
D7	Dual Mode data input pin <ul style="list-style-type: none"> ● According to the data shift direction of the data shift register, data can be input starting from the 81st bit When the chip is used as Dual Mode, D7 will be pulled-down When the chip is used as Single Mode, D7 won't be pulled-down
S/C	Segment mode/common mode selection pin <ul style="list-style-type: none"> ● When set to V_{SS} level "L", common mode is set
D0 - D6	Not used <ul style="list-style-type: none"> ● Connect D0-D6 to V_{SS} or V_{DD}. Avoiding floating
XCK	Not used <ul style="list-style-type: none"> ● XCK is pulled-down in common mode, so connect to V_{SS} or open
Y1 - Y160	LCD driver output pins <ul style="list-style-type: none"> ● These corresponding directly Corresponding directly to each bit of the shift register, one level (V0, V12, V43, or V5) is selected and output

Functional Description

1. Block description

1.1. Active Control

In the case of segment mode, controls the selection or deselection of the chip. Following a LP signal input, and after the select signal is input, a select signal is generated internally until 160 bits of data have been read in. Once data input has been completed, a select signal for cascade connection is output, and the chip is deselected.

In the case of common mode, controls the input/output data of bidirectional pins.

1.2. SP Conversion & Data Control

In the case of segment mode, keep input data which are 2 clocks of XCK at 4-bit parallel mode into latch circuit, or keep input data which are 1 clock of XCK at 8-bit parallel mode into latch circuit, after that they are put on the internal data bus 8 bits at a time.

1.3. Data Latch Control

In the case of the segment mode, it selects the state of the data latch, which reads in the data bus signals. The shift direction is controlled by the control logic and for every 16 bits of data read in, the selection signal shifts one bit, based on the state of the control circuit.

1.4. Data Latch

In the case of the segment mode, it latches the data on the data bus. The latched state of each LCD driver output pin is controlled by the control logic and the data latch control 160 bits of data are read in 20 sets of 8 bits.

1.5. Line Latch / Shift Register

In the case of the segment mode, all 160 bits which have been read into the data latch, are simultaneously latched on to the falling edge of the LP signal, and output to the level shift block.

In the case of the common mode, shifts data from the data input pin on to the falling edge of the LP signal.

1.6. Level Shifter

The logic voltage signal is level-shifted to the LCD driver voltage level, and output to the driver block.

1.7. 4-Level Driver

It drives the LCD driver output pins from the line latch/shift register data, selecting one of 4 levels (V_0 , V_{12} , V_{43} , V_{ss}) based on the S/C, FR and $\overline{\text{DISPOFF}}$ signals.

1.8. Control Logic

It controls the operation of each block. In the case of the segment mode, when an LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block. Once the selection signal has been output, operation of the data latch and data transmission are controlled, 160 bits of data are read in, and the chip is deselected.

In the case of the common mode, it controls the direction of the data shift.

2. LCD Driver Output Voltage Level

The relationship amongst the data bus signal, AC converted signal FR and LCD driver output voltage is as shown in the table below:

2.1. Segment Mode

FR	Latch Data	$\overline{\text{DISPOFF}}$	Driver Output Voltage Level (Y1 - Y160)
L	L	H	V43
L	H	H	V5
H	L	H	V12
H	H	H	V0
X	X	L	V5

Here, $V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$, H: VDD (+2.5 to +5.5V), L: VSS (0V), X: Don't care

2.2. Common Mode

FR	Latch Data	$\overline{\text{DISPOFF}}$	Driver Output Voltage Level (Y1 - Y160)
L	L	H	V43
L	H	H	V0
H	L	H	V12
H	H	H	V5
X	X	L	V5

Here, $V_{SS} \leq V_5 < V_{43} < V_{12} < V_0$, H: VDD (+2.5 to +5.5V), L: VSS (0V), X: Don't care

Note: There are two kinds of power supply (logic level voltage, LCD driver voltage) for the LCD driver. Please supply regular voltage, which assigned by specification for each power pin.

That time "Don't care" should be fixed to "H" or "L", avoiding floating.

3. Relationship between the Display Data and Driver Output Pins
3.1. Segment Mode:

(a) 4-bit Parallel Mode

MD	L/R	EIO1	EIO2	Data Input	Number of Clock						
					40clock	39clock	38clock	~	3clock	2clock	1clock
L	L	Output	Input	D0	Y1	Y5	Y9	~	Y149	Y153	Y157
				D1	Y2	Y6	Y10	~	Y150	Y154	Y158
				D2	Y3	Y7	Y11	~	Y151	Y155	Y159
				D3	Y4	Y8	Y12	~	Y152	Y156	Y160
L	H	Input	Output	D0	Y160	Y156	Y152	~	Y12	Y8	Y4
				D1	Y159	Y155	Y151	~	Y11	Y7	Y3
				D2	Y158	Y154	Y150	~	Y10	Y6	Y2
				D3	Y157	Y153	Y149	~	Y9	Y5	Y1

(b) 8-bit Parallel Mode

MD	L/R	EIO1	EIO2	Data Input	Number of Clock						
					20clock	19clock	18clock	~	3clock	2clock	1clock
H	L	Output	Input	D0	Y1	Y9	Y17	~	Y137	Y145	Y153
				D1	Y2	Y10	Y18	~	Y138	Y146	Y154
				D2	Y3	Y11	Y19	~	Y139	Y147	Y155
				D3	Y4	Y12	Y20	~	Y140	Y148	Y156
				D4	Y5	Y13	Y21	~	Y141	Y149	Y157
				D5	Y6	Y14	Y22	~	Y142	Y150	Y158
				D6	Y7	Y15	Y23	~	Y143	Y151	Y159
				D7	Y8	Y16	Y24	~	Y144	Y152	Y160
H	H	Input	Output	D0	Y160	Y152	Y144	~	Y24	Y16	Y8
				D1	Y159	Y151	Y143	~	Y23	Y15	Y7
				D2	Y158	Y150	Y142	~	Y22	Y14	Y6
				D3	Y157	Y149	Y141	~	Y21	Y13	Y5
				D4	Y156	Y148	Y140	~	Y20	Y12	Y4
				D5	Y155	Y147	Y139	~	Y19	Y11	Y3
				D6	Y154	Y146	Y138	~	Y18	Y10	Y2
				D7	Y153	Y145	Y137	~	Y17	Y9	Y1

3.2. Common Mode

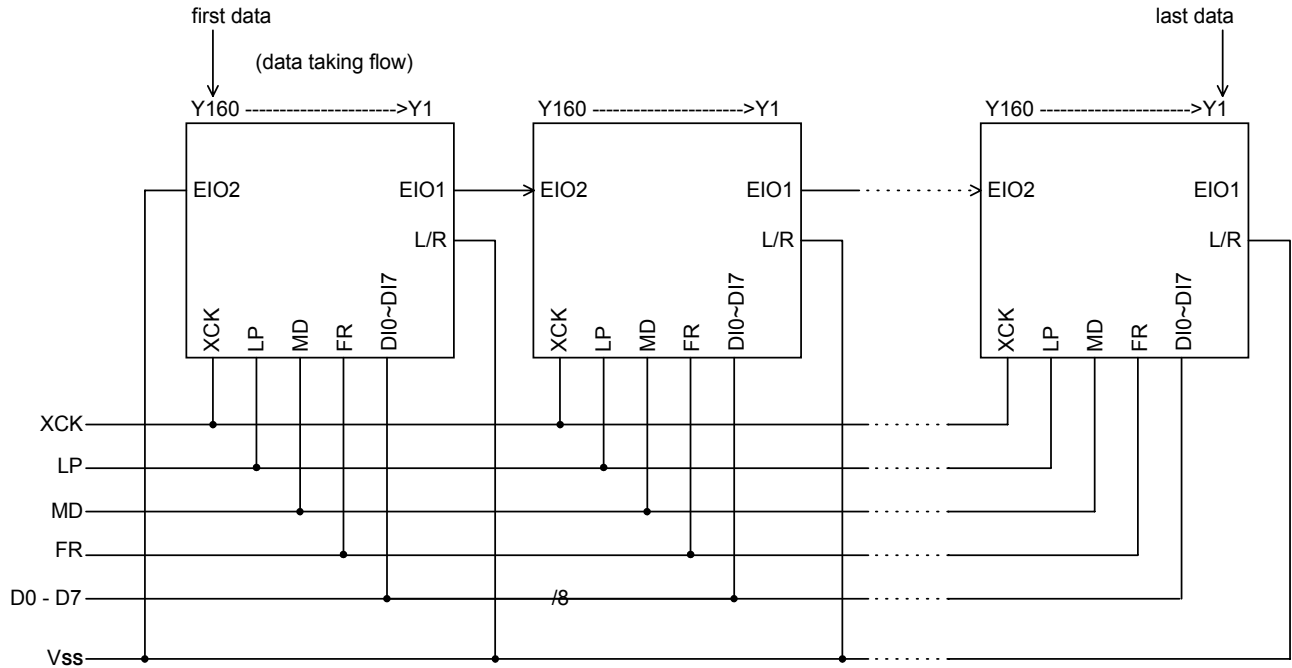
MD	L/R	Data Transfer Direction	EIO1	EIO2	D7
L (Single)	L (shift to left)	Y160 to Y1	Output	Input	X
	H (shift to right)	Y1 to Y160	Input	Output	X
H (Dual)	L (shift to left)	Y160 to Y81 Y80 to Y1	Output	Input	Input
	H (shift to right)	Y1 to Y80 Y81 to Y160	Input	Output	Input

Here, L: V_{SS} (0V), H: V_{DD} (+2.5V to +5.5V), X: Don't care

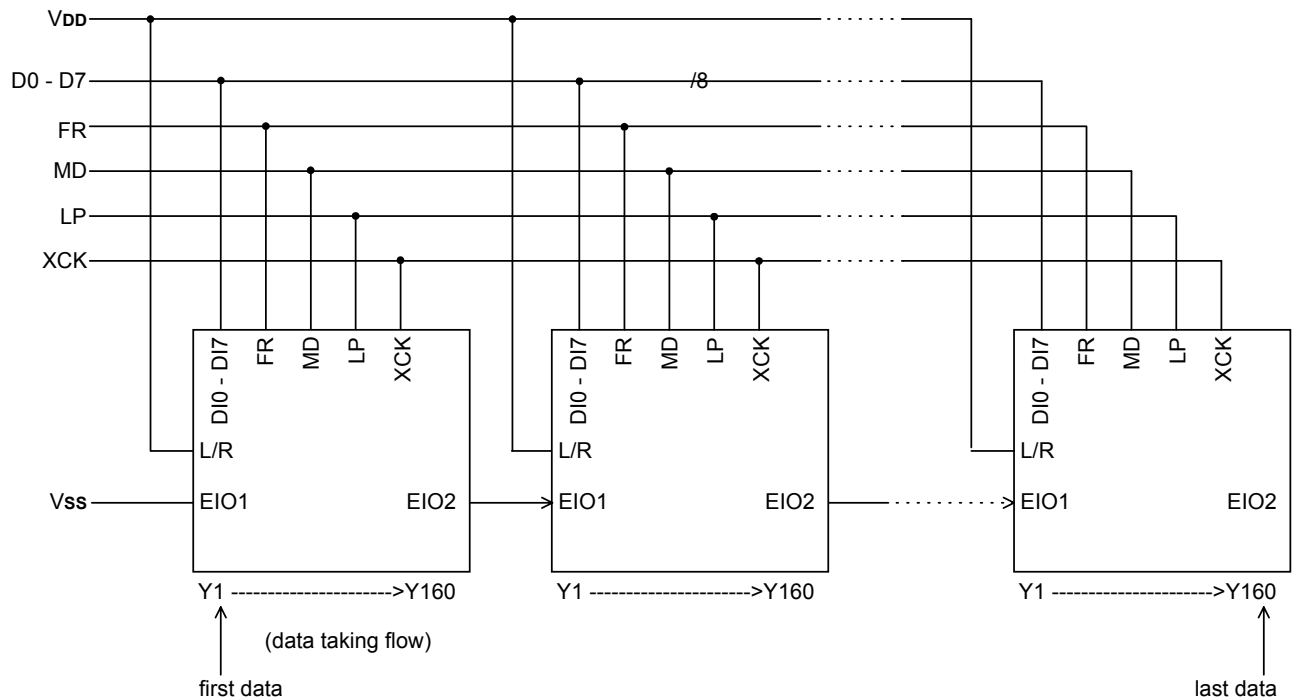
Note: "Don't care" should be fixed to "H" or "L", avoiding floating.

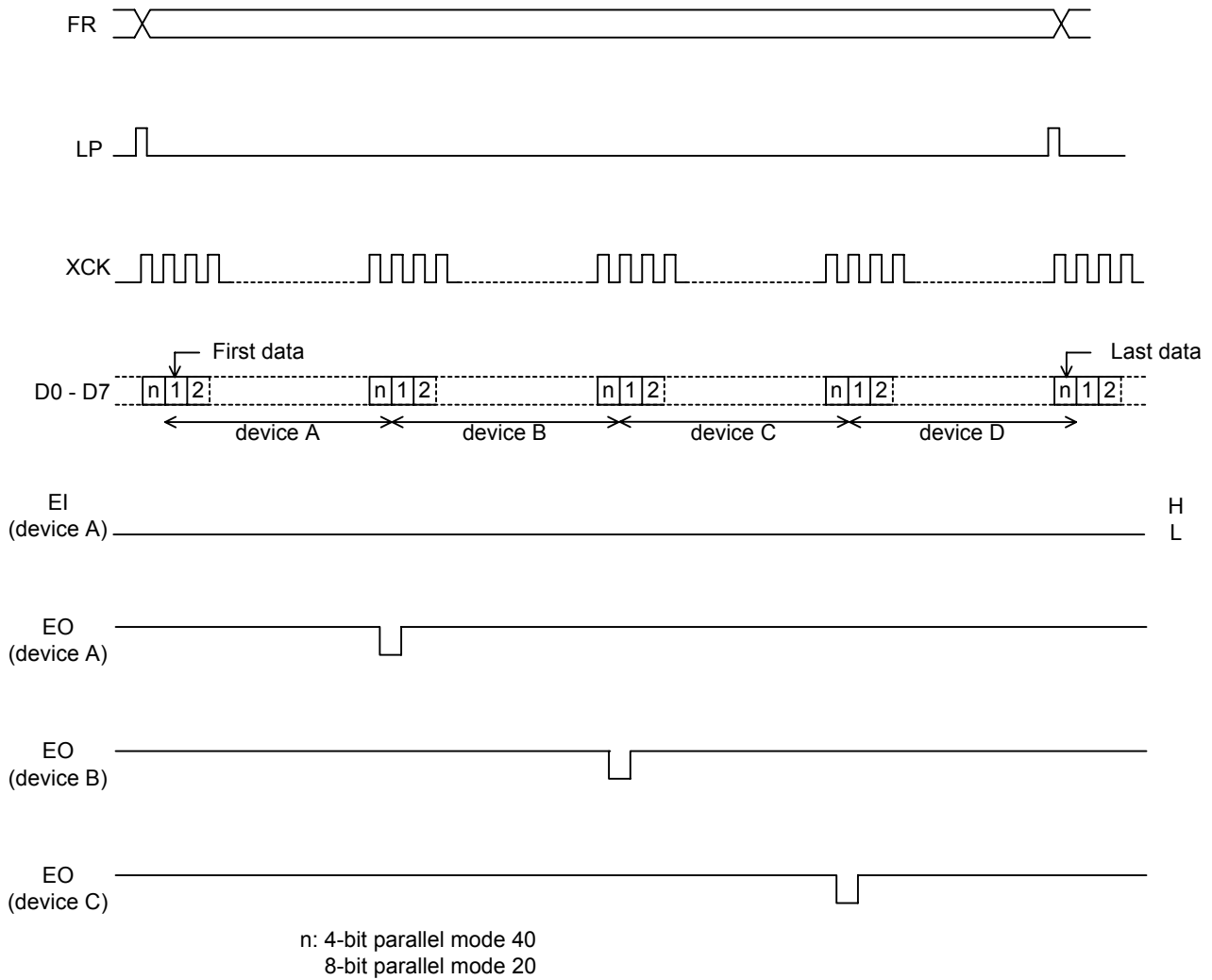
4. Connection Examples of Segment Drivers

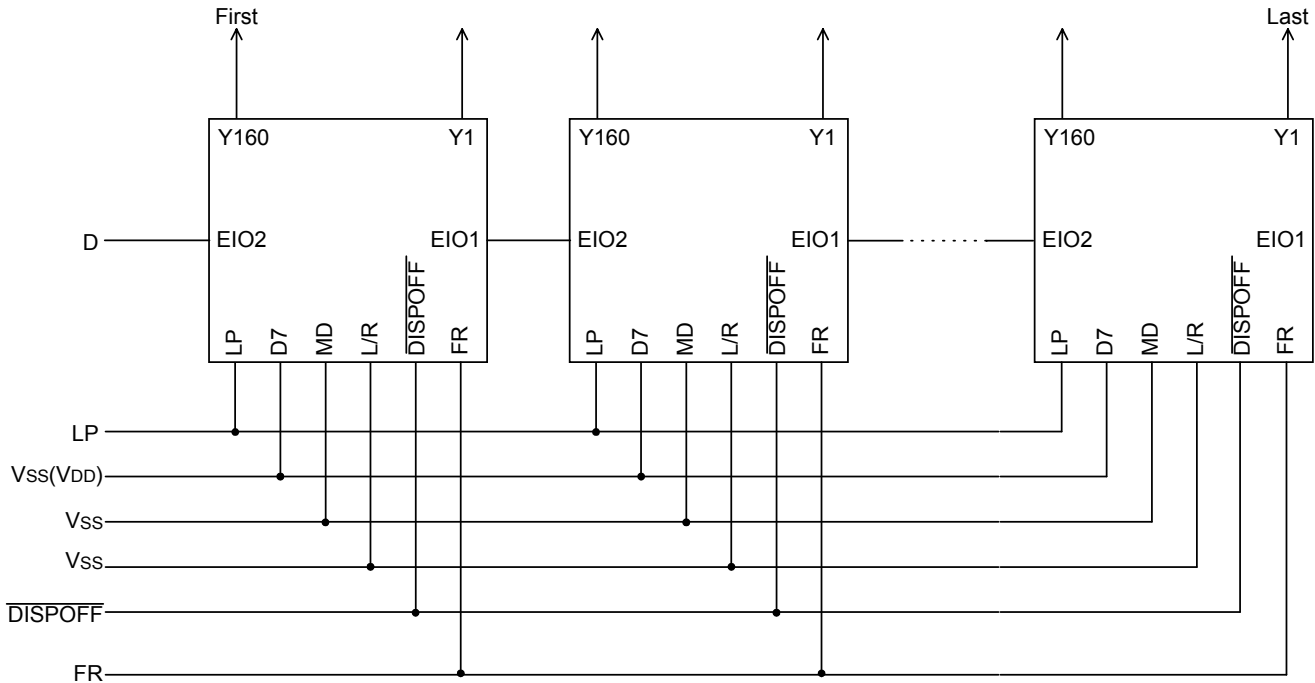
4.1. Case of L/R = "L"



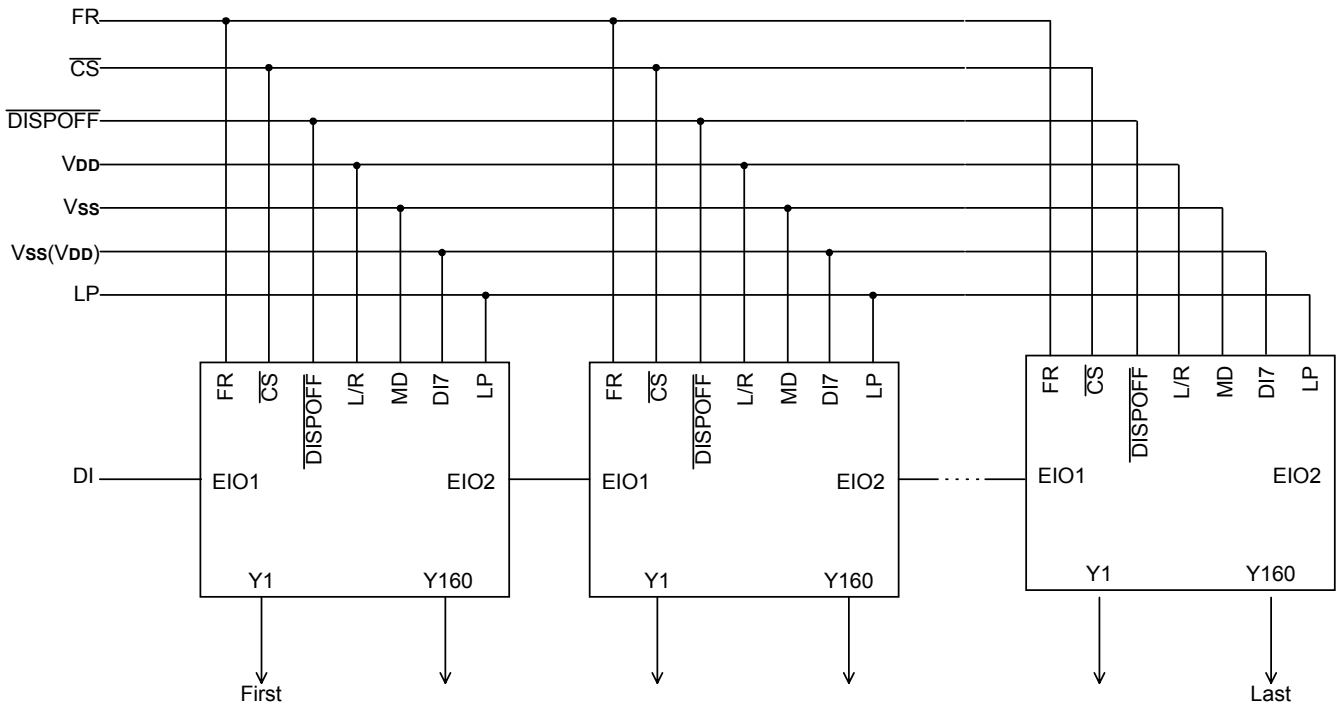
4.2 Case of L/R = "H"



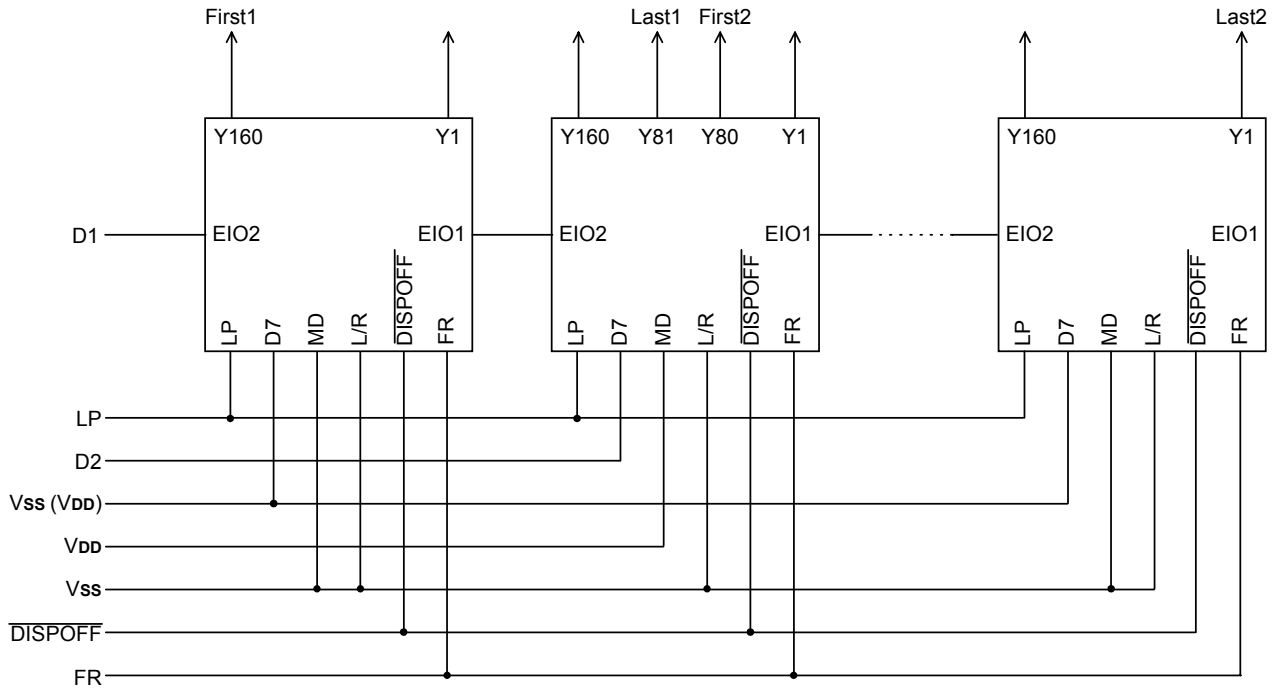
5. Timing Waveform of 4-Device Cascade Connection of Segment Drivers.


6. Connection Examples for Common Drivers


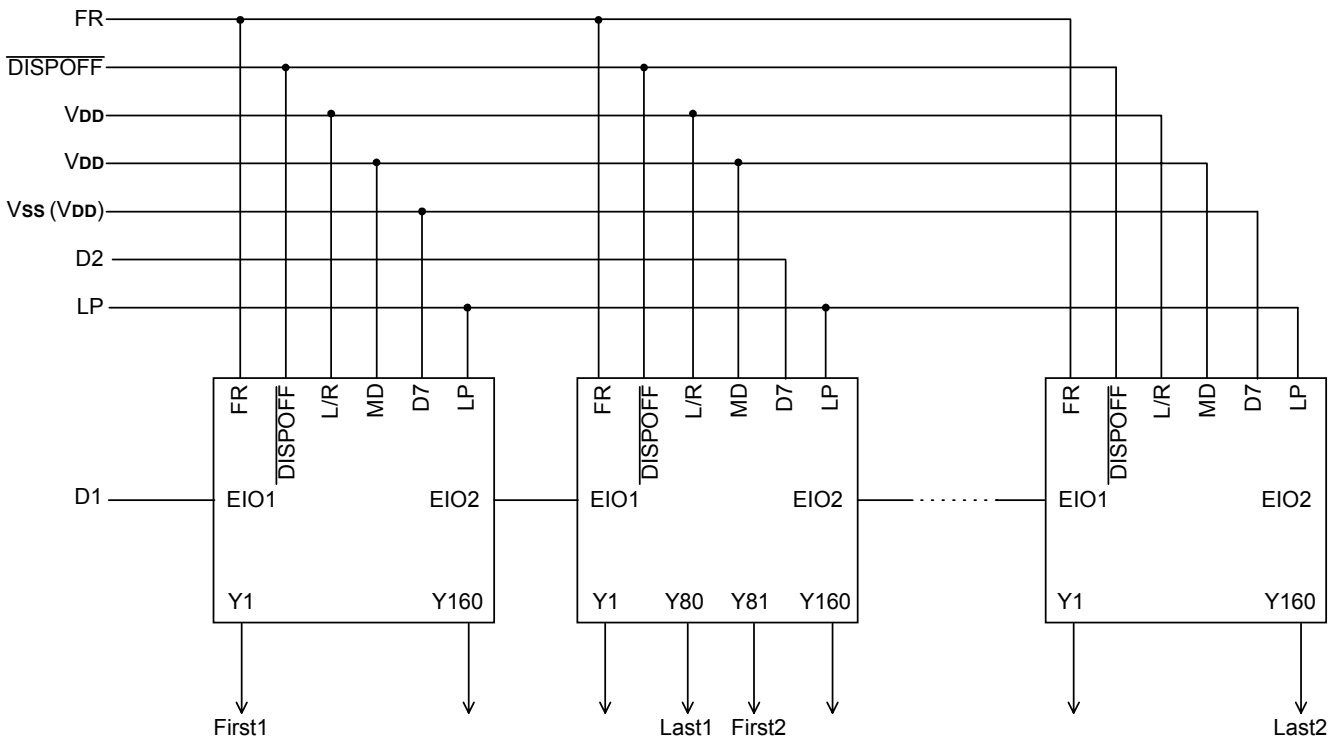
Single Mode (Shifting towards the left)



Single Mode (Shifting towards the right)



Dual mode (Shifting towards the left)



Dual mode (Shifting towards the right)

7. Precaution

Be careful when connecting or disconnecting the power

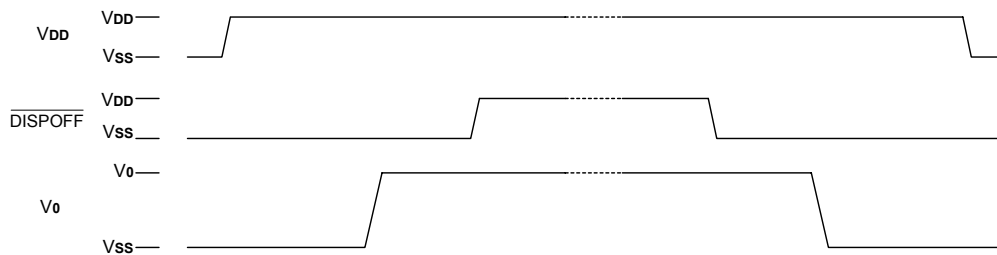
This LSI has a high-voltage LCD driver, so it may be permanently damaged by a high current, which may occur, if a voltage is supplied to the LCD driver power supply while the logic system power supply is floating.

The details are as follows:

- When connecting the power supply, connect the LCD driver power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD driver power.
- We recommend that you connect a serial resistor (50-100Ω) or fuse to the LCD driver power V_0 of the system as a current limiting device. Also, set a suitable value for the resistor in consideration of the LCD display grade.

In addition, when connecting the logic power supply, the logic condition of the LSI inside is insecure. Therefore connect the LCD driver power supply after resetting logic condition of this LSI inside on $\overline{\text{DISPOFF}}$ function. After that, the $\overline{\text{DISPOFF}}$ cancel the function after the LCD driver power supply has become stable. Furthermore, when disconnecting the power, set the LCD driver output pins to level V_{SS} on the $\overline{\text{DISPOFF}}$ function. After that, disconnect the logic system power after disconnecting the LCD driver power.

When connecting the power supply, follow the recommended sequence shown.



Absolute Maximum Rating*

DC Supply Voltage V_{DD}	-0.3V to +7.0V
DC Supply Voltage V_0	-0.3V to +30V
Input Voltage	-0.3V to V_{DD} +0.3V
Operating Ambient Temperature	-30°C to +85°C
Storage Temperature	-45°C to +125°C

***Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics
DC Characteristics

Segment Mode ($V_{SS} = V_S = 0V$, $V_{DD} = 2.5 - 5.5V$, $V_0 = 15$ to 30 V, and $T_A = -30$ to +85°C, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition	
Operating Voltage	V_{DD}	2.5	-	5.5	V		
Operating Voltage	V_0	15	-	30	V		
Input high voltage	V_{IH}	0.8 V_{DD}	-	-	V	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2 and $\overline{DISPOFF}$ pins	
Input low voltage	V_{IL}	-	-	0.2 V_{DD}	V		
Output high voltage	V_{OH}	$V_{DD} - 0.4$	-	-	V	EIO1, EIO2 pins, $I_{OH} = -0.4mA$	
Output low voltage	V_{OL}	-	-	+0.4	V	EIO1, EIO2 pins, $I_{OL} = +0.4mA$	
Input leakage current 1	I_{IH}	-	-	+1	μA	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2 and $\overline{DISPOFF}$ pins, $V_I = V_{DD}$	
Input leakage current 2	I_{IL}	-	-	-1	μA	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2 and $\overline{DISPOFF}$ pins, $V_I = V_{SS}$	
Output resistance	R_{ON}	-	1.0	1.5	$k\Omega$	$V_0 = +30.0V$	Y1 - Y160 pins, $ \Delta V_{ON} = 0.5V$
		-	1.5	2.0		$V_0 = +20.0V$	
Stand-by current	I_{SB}	-	-	5	μA	V_{SS} pin, Note 1	
Consumed current (1) (Deselection)	I_{DD1}	-	-	2.0	mA	V_{DD} pin, Note 2	
Consumed current (2) (Selection)	I_{DD2}	-	-	8.0	mA	V_{DD} pin, Note 3	
Consumed current	I_0	-	-	1.0	mA	V_0 pin, Note 4	

Note:

- $V_{DD} = +5.0V$, $V_0 = +30V$, $V_I = V_{SS}$
- $V_{DD} = +5.0V$, $V_0 = +30V$, $f_{XCK} = 14MHz$, No-load, $EI = V_{DD}$
The input data is turned over by the data taking clock (4-bit parallel input mode)
- $V_{DD} = +5.0V$, $V_0 = +30V$, $f_{XCK} = 14MHz$, No-load. $EI = V_{SS}$
The input data is turned over by the data taking clock (4-bit parallel input mode)
- $V_{DD} = +5.0V$, $V_0 = +30V$, $f_{XCK} = 14MHz$, $f_{LP} = 41.6kHz$. $f_{FR} = 80 Hz$, No-load
The input data is turned over by the data taking clock (4-bit parallel-input mode)

Common Mode ($V_{SS} = V_S = 0V$, $V_{DD} = 2.5 - 5.5V$, $V_0 = 15$ to $30V$, and $T_A = -30$ to $+85^\circ C$, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition	
Operating Voltage	V_{DD}	2.5	-	5.5	V		
Operating Voltage	V_0	15	-	30	V		
Input high voltage	V_{IH}	$0.8 V_{DD}$	-	-	V	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2 and $\overline{DISPOFF}$ pins	
Input low voltage	V_{IL}	-	-	$0.2 V_{DD}$	V		
Output high voltage	V_{OH}	$V_{DD} - 0.4$	-	-	V	EIO1, EIO2 pins, $I_{OH} = -0.4mA$	
Output low voltage	V_{OL}	-	-	+0.4	V	EIO1, EIO2 pins, $I_{OL} = +0.4mA$	
Input leakage current 1	I_{IH}	-	-	+10.0	μA	D0 - 6, LP, L/R, FR, MD, S/C and $\overline{DISPOFF}$ pins, $V_I = V_{DD}$	
Input leakage current 2	I_{IL}	-	-	-10.0	μA	D0 - 7, XCK, LP, L/R, FR, MD, S/C, EIO1, EIO2 and $\overline{DISPOFF}$ pins, $V_I = V_{SS}$	
Output resistance	R_{ON}	-	1.0	1.5	$k\Omega$	$V_0 = +30.0V$	Y1 - Y160 pins, $ \Delta V_{ON} = 0.5V$
		-	1.5	2.0		$V_0 = +20.0V$	
Stand-by current	I_{SB}	-	-	50	μA	V_{SS} pin, Note 1	
Consumed current (1)	I_{DD}	-	-	80	μA	V_{DD} pin, Note 2	
Consumed current (2)	I_0	-	-	160	μA	V_0 pin, Note 2	

Note:

- $V_{DD} = +5.0V$, $V_0 = +30V$, $f_{LP} = 0 - 41.6kHz$
- $V_{DD} = +5.0V$, $V_0 = +30V$, $f_{LP} = 41.6kHz$, $f_{FR} = 80Hz$, case of 1/480 duty operation, No-load

AC Characteristics

 Segment Mode 1 ($V_{SS} = V_5 = 0V$, $V_{DD} = 4.5 - 5.5V$, $V_0 = 15$ to 30 , and $T_A = -30$ to $+85^\circ C$, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	twck	71	-		ns	tr, tf \leq 10ns, Note 1
Shift clock "H" pulse width	twckH	23	-		ns	
Shift clock "L" pulse width	twckL	23	-		ns	
Data setup time	tDS	10	-		ns	
Data hold time	tDH	20	-		ns	
Latch pulse "H" pulse width	twLPH	23	-		ns	
Shift clock rise to Latch pulse rise time	tLD	0	-		ns	
Shift clock fall to Latch pulse fall time	tSL	25	-		ns	
Latch pulse rise to Shift clock rise time	tLS	25	-		ns	
Latch pulse fall to Shift clock rise time	tLH	25	-		ns	
Input signal rise time	tr		-	50	ns	Note 2
Input signal fall time	tf		-	50	ns	Note 2
Enable setup time	ts	21	-		ns	
$\overline{\text{DISPOFF}}$ Removal time	tSD	100	-		ns	
$\overline{\text{DISPOFF}}$ enable pulse width	twDL	1.2	-		μs	
Output delay time (1)	td		-	40	ns	CL = 15pF
Output delay time (2)	t _{pd1} , t _{pd2}		-	1.2	μs	CL = 15pF
Output delay time (3)	t _{pd3}		-	1.2	μs	CL = 15pF

Note

1. Take the cascade connection into consideration.
2. $(T_{ck} - tw_{ckH} - tw_{ckL})/2$ is the maximum in the case of high speed operation.

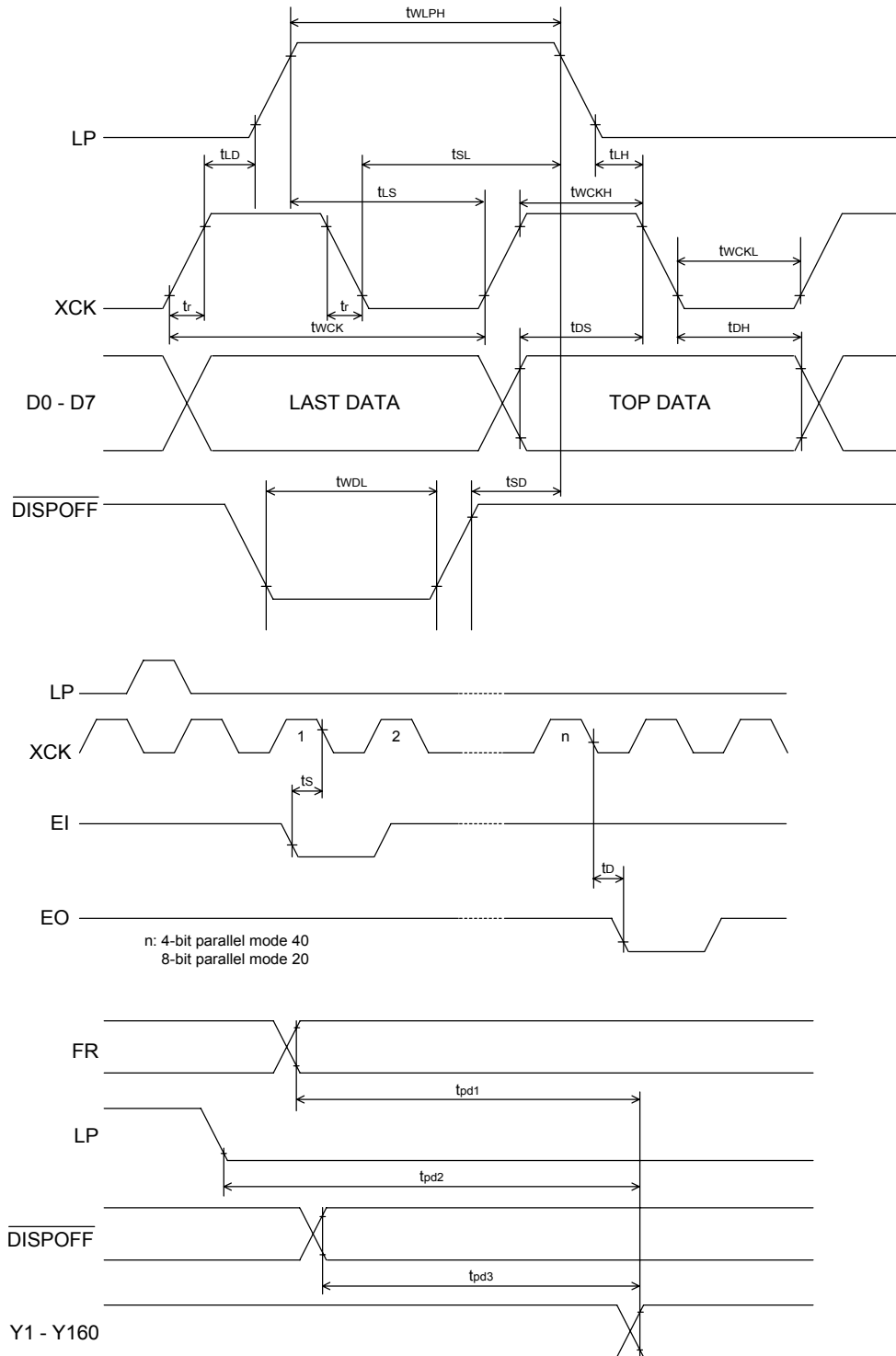
Segment Mode 2 ($V_{SS} = V_S = 0V$, $V_{DD} = 2.5 - 4.5V$, $V_0 = 15$ to 30 , and $T_A = -30$ to $+85^\circ C$, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	twck	125	-		ns	$t_r, t_f \leq 11ns$, Note 1
Shift clock "H" pulse width	twckH	51	-		ns	
Shift clock "L" pulse width	twckL	51	-		ns	
Data setup time	tDS	30	-		ns	
Data hole time	tDH	40	-		ns	
Latch pulse "H" pulse width	twLPH	51	-		ns	
Shift clock rise to Latch pulse rise time	tLD	0	-		ns	
Shift clock fall to Latch pulse fall time	tSL	51	-		ns	
Latch pulse rise to Shift clock rise time	tLS	51	-		ns	
Latch pulse fall to Shift clock fall time	tLH	51	-		ns	
Input signal rise time	t _r		-	50	ns	Note 2
Input signal fall time	t _f		-	50	ns	Note 2
Enable setup time	t _s	36	-		ns	
$\overline{\text{DISPOFF}}$ Removal time	t _{SD}	100	-		ns	
$\overline{\text{DISPOFF}}$ enable pulse width	t _{WDL}	1.2	-		μs	
Output delay time (1)	t _d		-	78	ns	CL = 15pF
Output delay time (2)	t _{pd1} , t _{pd2}		-	1.2	μs	CL = 15pF
Output delay time (3)	t _{pd3}		-	1.2	μs	CL = 15pF

Note

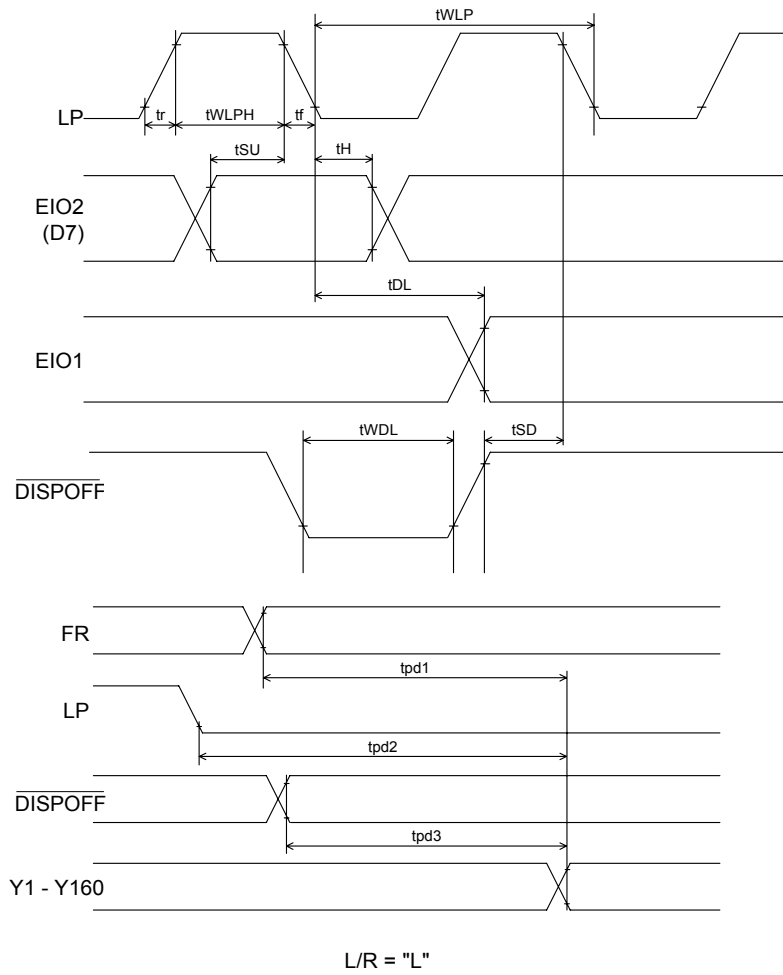
1. Take the cascade connection into consideration.
2. $(t_{CK} - twckH - twckL)/2$ is the maximum in the case of high speed operation.

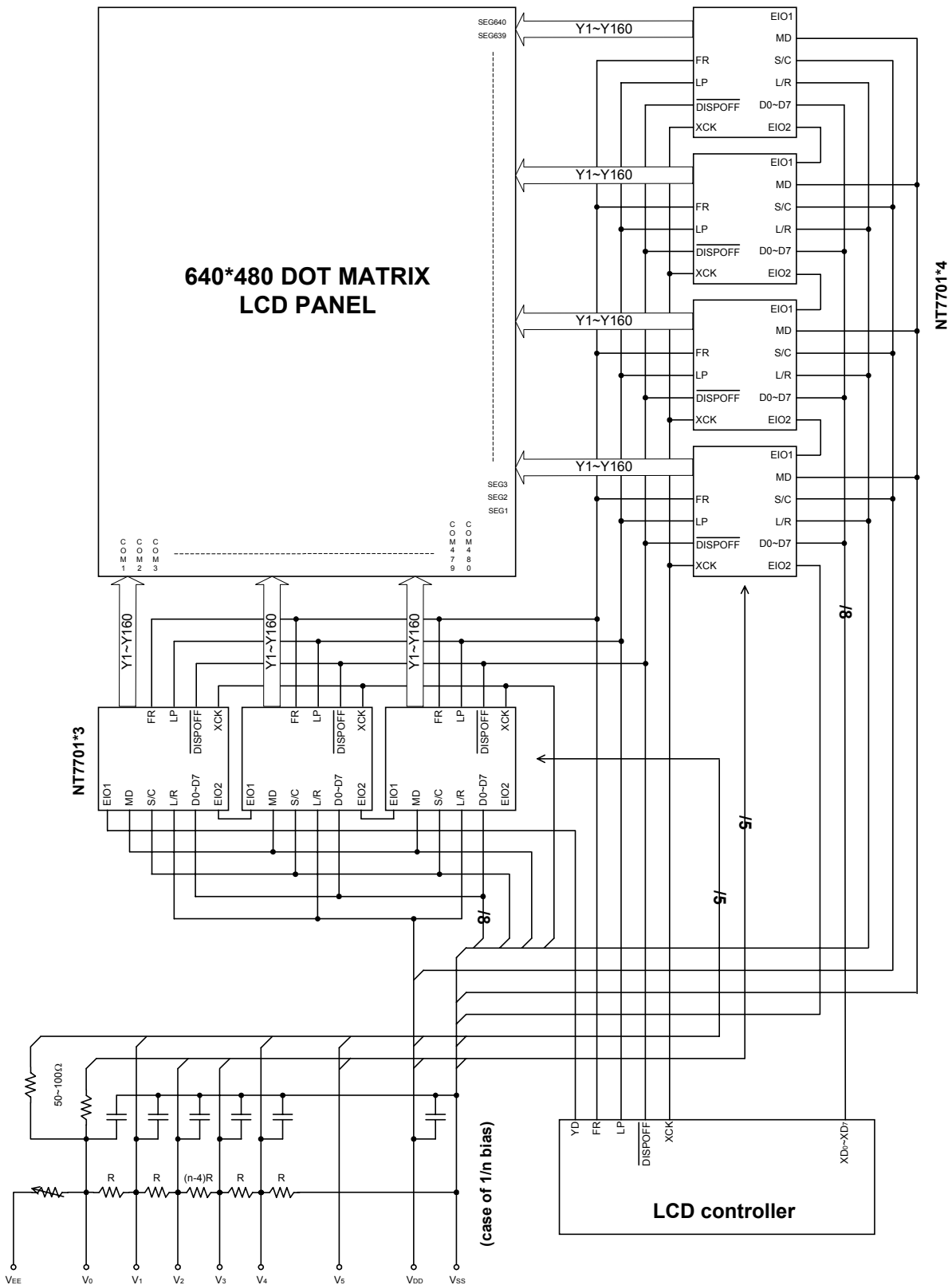
Timing waveform of the Segment Mode

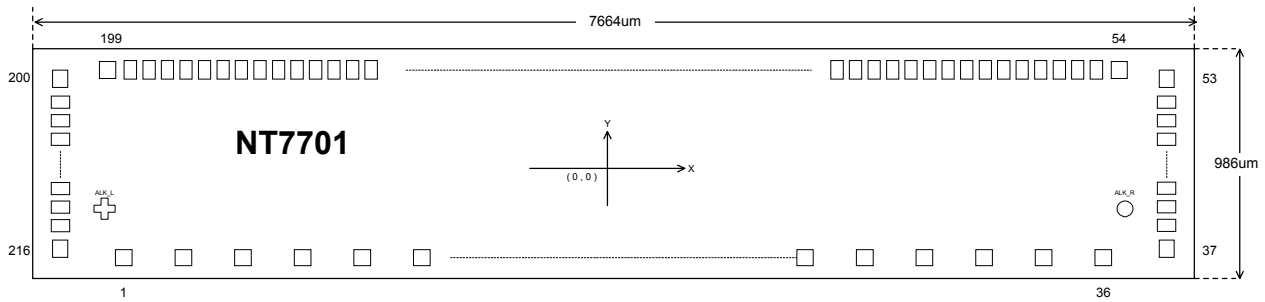


Common Mode ($V_{SS} = V_S = 0V$, $V_{DD} = 2.5 - 5.5V$, $V_0 = 15$ to $30V$ and $T_A = -30$ to $+85^\circ C$, unless otherwise noted)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Shift clock period	tWLP	250	-	-	ns	$t_r, t_f \leq 20ns$
Shift clock "H" pulse width	tWLPH	15	-	-	ns	$V_{DD} = +5.0V \pm 10\%$
		30	-	-	ns	$V_{DD} = +2.5 - +4.5V$
Data setup time	tSU	30	-	-	ns	
Data hole time	tH	50	-	-	ns	
Input signal rise time	t _r		-	50	ns	
Input signal fall time	t _f		-	50	ns	
$\overline{DISPOFF}$ Removal time	tSD	100	-	-	ns	
$\overline{DISPOFF}$ enable pulse width	tWDL	1.2	-	-	μs	
Output delay time (1)	tDL	-	-	200	ns	$C_L = 15pF$
Output delay time (2)	t _{pd1} , t _{pd2}	-	-	1.2	μs	$C_L = 15pF$
Output delay time (3)	t _{pd3}	-	-	1.2	μs	$C_L = 15pF$

Timing Characteristics of Common Mode


Application Circuit (for reference only)


Bonding Diagram

Pad Location

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	LR	-3600	-440	31	EIO1	2160	-440
2	LR	-3440	-440	32	EIO1	2320	-440
3	VDD	-3280	-440	33	FR	2480	-440
4	VDD	-3120	-440	34	FR	2640	-440
5	SC	-2000	-440	35	MD	2800	-440
6	SC	-1840	-440	36	MD	2960	-440
7	EIO2	-1680	-440	37	GND	3779	-410
8	EIO2	-1520	-440	38	GND	3779	-350
9	D0	-1360	-440	39	V5R	3779	-300
10	D0	-1200	-440	40	V5R	3779	-250
11	D1	-1040	-440	41	V43R	3779	-200
12	D1	-880	-440	42	V43R	3779	-150
13	D2	-720	-440	43	V12R	3779	-100
14	D2	-560	-440	44	V12R	3779	-50
15	D3	-400	-440	45	V0R	3779	0
16	D3	-240	-440	46	V0R	3779	50
17	D4	-80	-440	47	Y1	3779	100
18	D4	80	-440	48	Y2	3779	150
19	D5	240	-440	49	Y3	3779	200
20	D5	400	-440	50	Y4	3779	250
21	D6	560	-440	51	Y5	3779	300
22	D6	720	-440	52	Y6	3779	350
23	D7	880	-440	53	Y7	3779	410
24	D7	1040	-440	54	Y8	3635	440
25	XCK	1200	-440	55	Y9	3575	440
26	XCK	1360	-440	56	Y10	3525	440
27	$\overline{\text{DISPOFF}}$	1520	-440	57	Y11	3475	440
28	$\overline{\text{DISPOFF}}$	1680	-440	58	Y12	3425	440
29	LP	1840	-440	59	Y13	3375	440
30	LP	2000	-440	60	Y14	3325	440

Pad Location (continued)

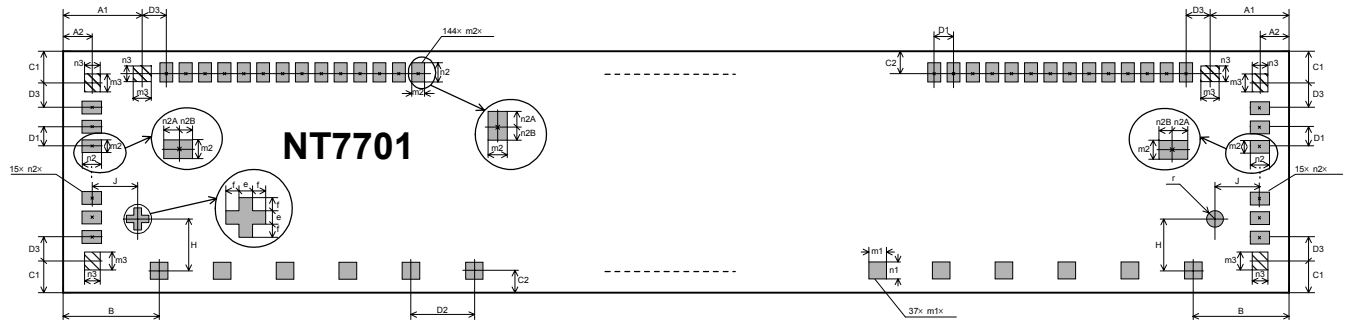
Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
61	Y15	3275	440	101	Y55	1275	440
62	Y16	3225	440	102	Y56	1225	440
63	Y17	3175	440	103	Y57	1175	440
64	Y18	3125	440	104	Y58	1125	440
65	Y19	3075	440	105	Y59	1075	440
66	Y20	3025	440	106	Y60	1025	440
67	Y21	2975	440	107	Y61	975	440
68	Y22	2925	440	108	Y62	925	440
69	Y23	2875	440	109	Y63	875	440
70	Y24	2825	440	110	Y64	825	440
71	Y25	2775	440	111	Y65	775	440
72	Y26	2725	440	112	Y66	725	440
73	Y27	2675	440	113	Y67	675	440
74	Y28	2625	440	114	Y68	625	440
75	Y29	2575	440	115	Y69	575	440
76	Y30	2525	440	116	Y70	525	440
77	Y31	2475	440	117	Y71	475	440
78	Y32	2425	440	118	Y72	425	440
79	Y33	2375	440	119	Y73	375	440
80	Y34	2325	440	120	Y74	325	440
81	Y35	2275	440	121	Y75	275	440
82	Y36	2225	440	122	Y76	225	440
83	Y37	2175	440	123	Y77	175	440
84	Y38	2125	440	124	Y78	125	440
85	Y39	2075	440	125	Y79	75	440
86	Y40	2025	440	126	Y80	25	440
87	Y41	1975	440	127	Y81	-25	440
88	Y42	1925	440	128	Y82	-75	440
89	Y43	1875	440	129	Y83	-125	440
90	Y44	1825	440	130	Y84	-175	440
91	Y45	1775	440	131	Y85	-225	440
92	Y46	1725	440	132	Y86	-275	440
93	Y47	1675	440	133	Y87	-325	440
94	Y48	1625	440	134	Y88	-375	440
95	Y49	1575	440	135	Y89	-425	440
96	Y50	1525	440	136	Y90	-475	440
97	Y51	1475	440	137	Y91	-525	440
98	Y52	1425	440	139	Y92	-575	440
99	Y53	1375	440	139	Y93	-625	440
100	Y54	1325	440	140	Y94	-675	440

Pad Location (continued)

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
141	Y95	-725	440	181	Y135	-2725	440
142	Y96	-775	440	182	Y136	-2775	440
143	Y97	-825	440	183	Y137	-2825	440
144	Y98	-875	440	184	Y138	-2875	440
145	Y99	-925	440	185	Y139	-2925	440
146	Y100	-975	440	186	Y140	-2975	440
147	Y101	-1025	440	187	Y141	-3025	440
148	Y102	-1075	440	188	Y142	-3075	440
149	Y103	-1125	440	189	Y143	-3125	440
150	Y104	-1175	440	190	Y144	-3175	440
151	Y105	-1225	440	191	Y145	-3225	440
152	Y106	-1275	440	192	Y146	-3275	440
153	Y107	-1325	440	193	Y147	-3325	440
154	Y108	-1375	440	194	Y148	-3375	440
155	Y109	-1425	440	195	Y149	-3425	440
156	Y110	-1475	440	196	Y150	-3475	440
157	Y111	-1525	440	197	Y151	-3525	440
158	Y112	-1575	440	198	Y152	-3575	440
159	Y113	-1625	440	199	Y153	-3635	440
160	Y114	-1675	440	200	Y154	-3779	410
161	Y115	-1725	440	201	Y155	-3779	350
162	Y116	-1775	440	202	Y156	-3779	300
163	Y117	-1825	440	203	Y157	-3779	250
164	Y118	-1875	440	204	Y158	-3779	200
165	Y119	-1925	440	205	Y159	-3779	150
166	Y120	-1975	440	206	Y160	-3779	100
167	Y121	-2025	440	207	V0L	-3779	50
168	Y122	-2075	440	208	V0L	-3779	0
169	Y123	-2125	440	209	V12L	-3779	-50
170	Y124	-2175	440	210	V12L	-3779	-100
171	Y125	-2225	440	211	V43L	-3779	-150
172	Y126	-2275	440	212	V43L	-3779	-200
173	Y127	-2325	440	213	V5L	-3779	-250
174	Y128	-2375	440	214	V5L	-3779	-300
175	Y129	-2425	440	215	GND	-3779	-350
176	Y130	-2475	440	216	GND	-3779	-410
177	Y131	-2525	440		ALK_L	-3438	-323
178	Y132	-2575	440		ALK_R	3438	-323
179	Y133	-2625	440				
180	Y134	-2675	440				

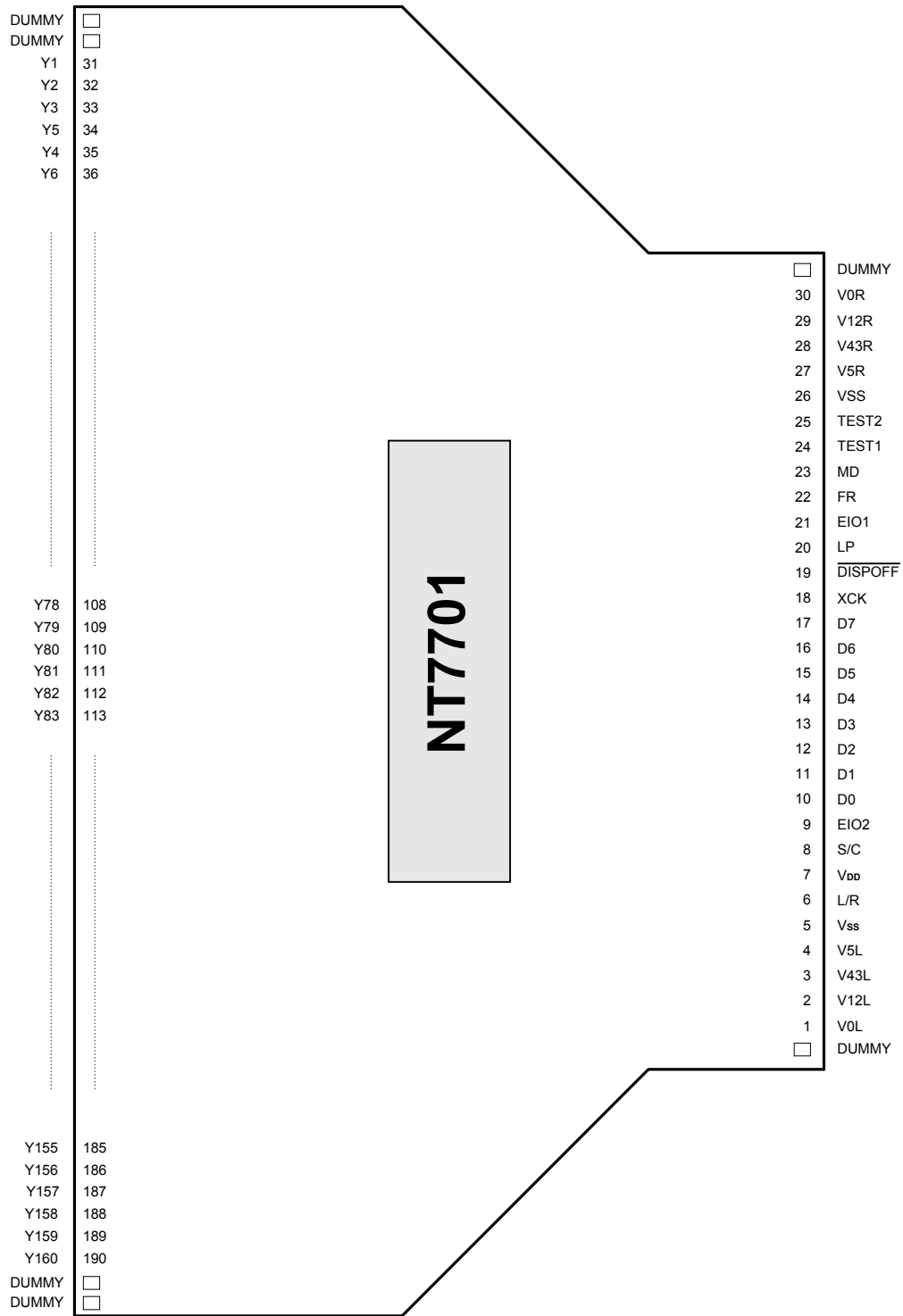
Dummy Pad Location (Total: 10 pin)

NO	X	Y	NO	X	Y	NO	X	Y	NO	X	Y
0	-2960	-440	3	-2480	-440	6	3120	-440	9	3600	-440
1	-2800	-440	4	-2320	-440	7	3280	-440			
2	-2640	-440	5	-2160	-440	8	3440	-440			

Package Information

Chip Outline Dimensions

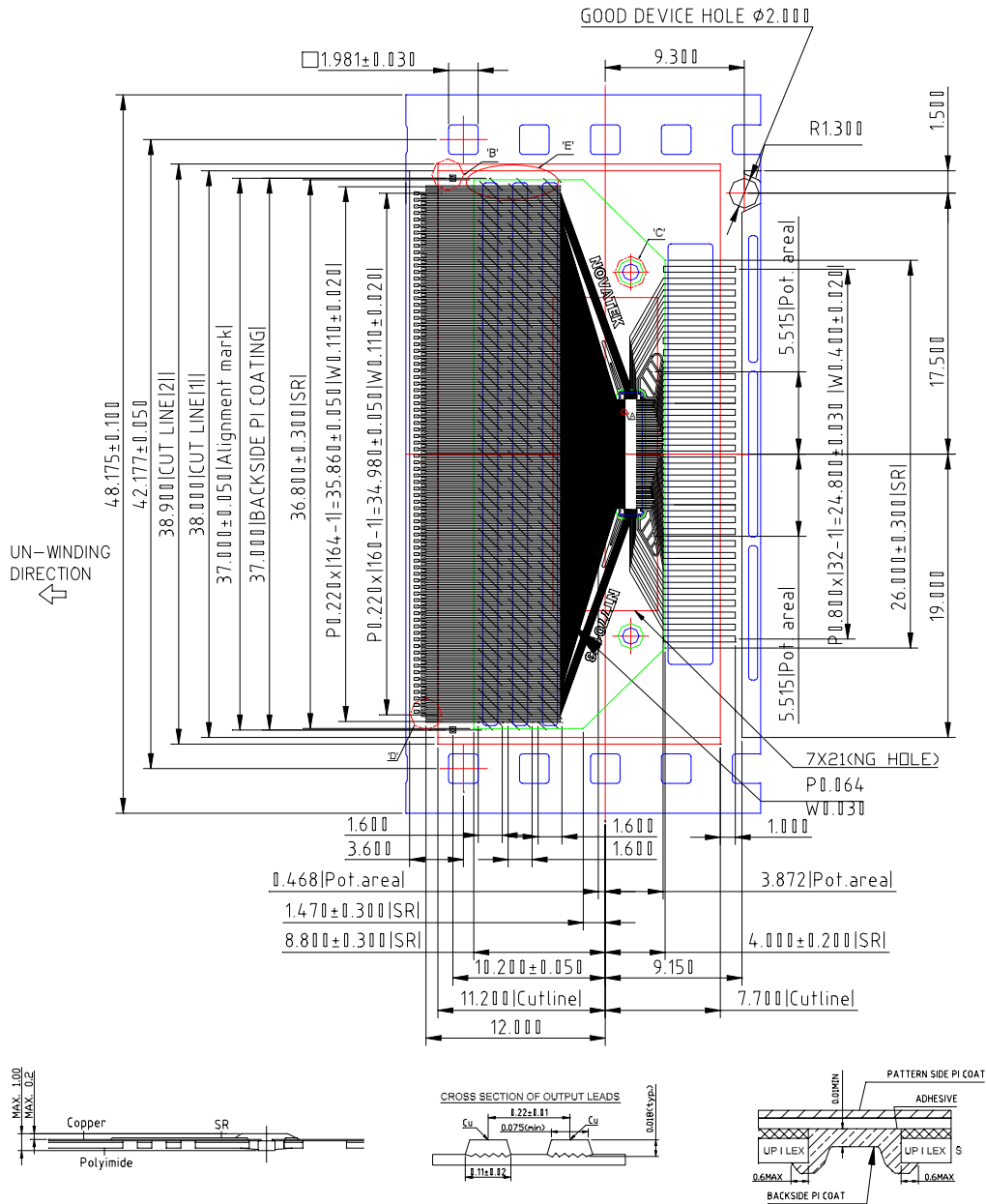
 unit: μm

Symbol	Dimensions in μm	Symbol	Dimensions in μm
A1	197	n1	56
A2	53	n2	67
B	232	n2A	35
C1	83	n2B	32
C2	53	n3	60
D1	50	r	35
D2	160	e	24
D3	60	f	23
m1	54	H	120
m2	32	J	202
m3	52		

TCP Pin Layout


(COPPER SIDE VIEW)

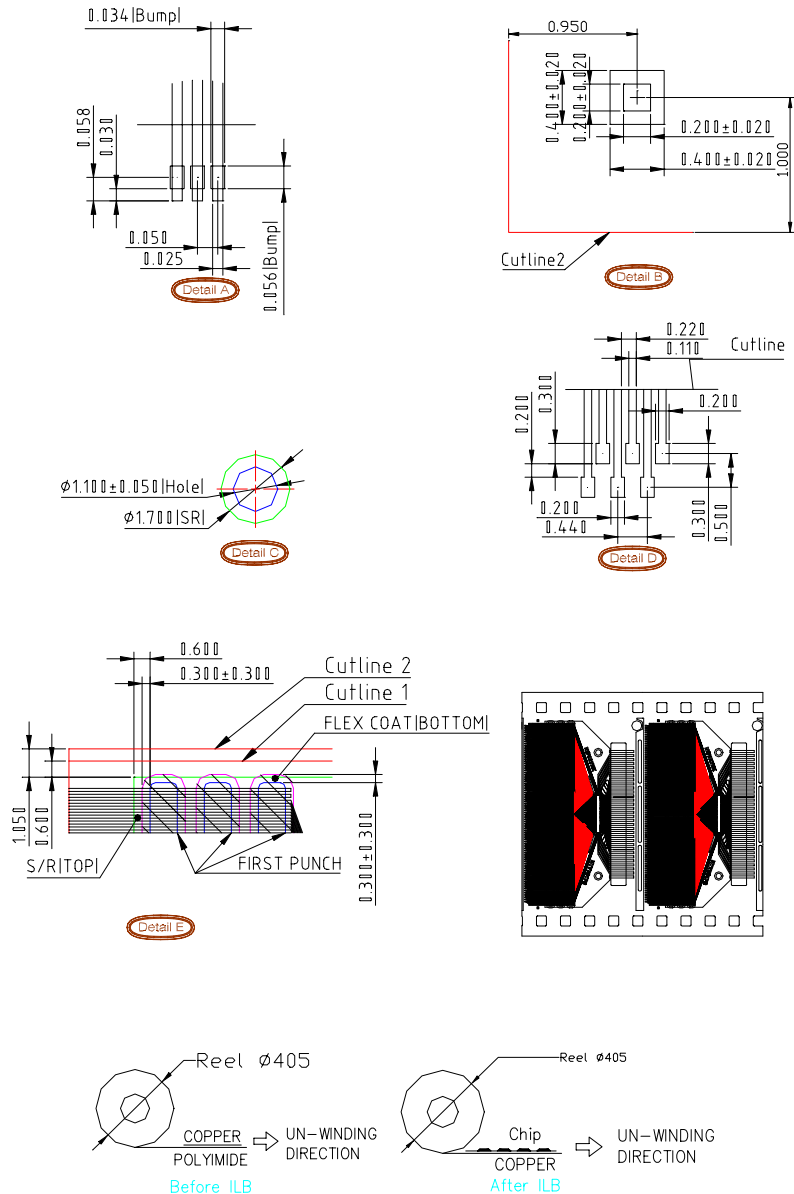
External view of TCP pins



NOTE:

1. GENERAL TOLERANCE ± 0.050 mm
2. ALL CHAMFER IS R0.200mm
3. MATERIAL

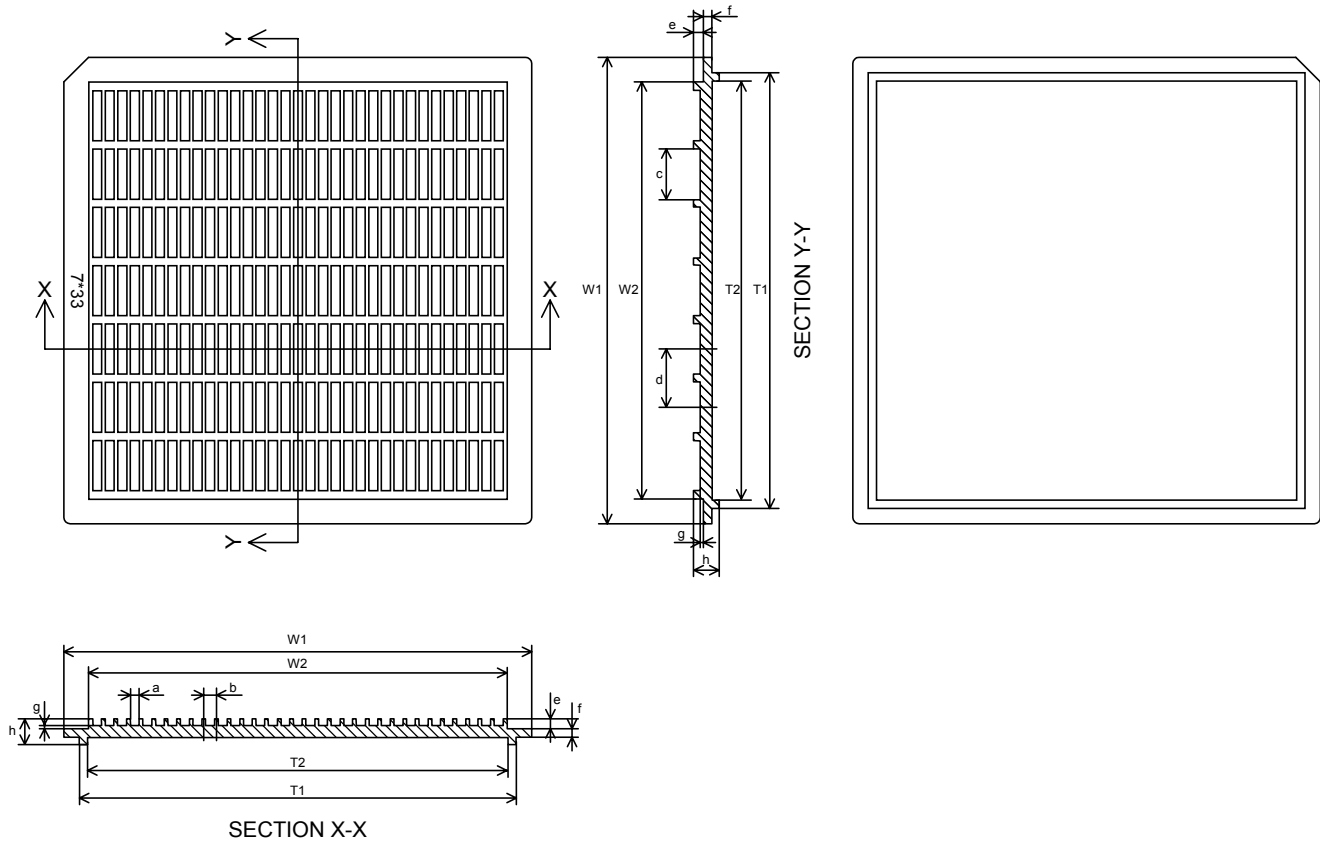
Polyimide: UPILEX-S	75 ± 6 μ m
Adhesive: TORAY #7100	12 ± 3 μ m
Copper: FQ-VLP	18 ± 5 μ m
Plating Sn:	0.21 ± 0.05 μ m
Solder Resist: AE-70-M11	26 ± 14 μ m
Flex Coating: FS-100L	MIN 10 μ m
Space Tape Material Polyester (PET)	
Leader Tape Material Polyester (PET)	
PKG Reel Size:	405 mm
- 4.5 SPROCKET HOLES (23.75MM) FOR 1 TAPESITE


Cautions concerning storage:

- When storing the product, it is recommended that it be left in its shipping package. After the seal of the packing bag has been broken, store the products in a nitrogen atmosphere.
- Storage conditions :

Storage state	Storage conditions
unopened (less than 90 days)	Temperature: 5 to 30°C ; humidity: 80%RH or less
After seal of broken (less than 30 days)	Room temperature, dry nitrogen atmosphere

- Don't store in a location exposed to corrosive gas or excessive dust.
- Don't store in a location exposed to direct sunlight of subject to sharp changes in temperature.
- Don't store the product such that it is subjected to an excessive load weight, such as by stacking.
- Deterioration of the plating may occur after long-term storage, so special care is required. It is recommended that the products be inspected before use.

Tray Information


Symbol	Dimensions in mm	Symbol	Dimensions in mm
a	1.46	g	0.84
b	2.04	h	4.20
c	8.16	W1	76.0
d	9.50	W2	68.0
e	1.60	T1	71.0
f	1.40	T2	68.3

Ordering Information

Part No.	Package
NT7701H-BDT	Au bump on chip tray
NT7701H-TABF3	TCP Form

Product Spec. Change Notice

NT7701 Specification Revision History		
Version	Content	Date
2.0	<ul style="list-style-type: none">• Chip size modified (Due to scribe-line modified, change 7720 μ m x 1030 μ m to 7664 μ m x 986 μ m , Page 27)• Gold bump size modified (Page 31)	Jul. 2002
1.0	Formal version release	Oct. 2000