ELECTRONICS, INC.
44 FARRAND STREET
BLOOMFIELD, NJ 07003
(973) 748–5089

# NTE2053
# Integrated Circuit
# 8–Bit MPU Compatible A/D Converter

**Description:**

The NTE2053 is a CMOS 8–bit successive approximation Analog to Digital converter in a 20–Lead DIP type package which uses a differential potentiometric ladder – similar to the 256R products. This device is designed to allow operation with the NSC800 and INS8080A derivative control bus, and TRI–STATE® output latches directly drive the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

A new differential analog voltage input allows increasing the common–mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any similar analog voltage span to the full 8 bits of resolution.

**Features:**

- Compatible With 8080 MPU Derivatives – No Interfacing Logic Needed – Access Time: 135ns
- Easy Interface to all Microprocessors, or Operates “Stand Alone”
- Differential Analog Voltage Inputs
- Logic Inputs and Outputs Meet Both MOS and TTL Voltage Level Specifications
- Works With 2.5V (NTE952) Voltage Reference
- On–Chip Clock Generator
- 0V to 5V Analog Input Voltage Range with Single 5V Supply
- No Zero Adjust Required
- Operates Ratiometrically or with 5V, 2.5V, or Analog Span Adjusts Voltage Reference

**Absolute Maximum Ratings:** (Note 1, Note 2)

Supply Voltage (Note 3), $V_{CC}$ . . . . . 6.5V
Voltage at Logic Control Inputs . . . . . –0.3V to +18V
Voltage at All Other Inputs and Outputs . . . . . –0.3V to $V_{CC}$ +0.3V
Storage Temperature Range, $T_{stg}$ . . . . . –65° to +150°C
Power Dissipation ($T_A$ = +25°C), $P_D$ . . . . . 875mW
Lead Temperature (During Soldering, 10sec), $T_L$ . . . . . +300°C

**Recommended Operating Conditions:** (Note 1, Note 2)

Operating Temperature Range, $T_A$ . . . . . 0° to +70°C
Supply Voltage Range, $V_{CC}$ . . . . . 4.5V to 6.3V

Note 1. Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.
Note 2. All voltage are measured with respect to GND, unless otherwise specified. The separate A GND point should always be wired to the D GND.
Note 3. A zener diode exists, internally, from $V_{CC}$ to GND and has a typical breakdown voltage of 7V.

**Electrical Characteristics:** ($V_{CC}$ = 5V, $T_A$ = 0° to +70°C, $f_{CLK}$ = 640kHz unless otherwise specified)

| Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Total Unadjusted Error (Note 4) | $V_{REF}/2$ = 2.500V | – | – | $\pm^1/_2$ | LSB |
| $V_{REF}/2$ Input Resistance | | 2.5 | 8.0 | – | kΩ |
| Analog Input Voltage Range | V(+) or V(–), Note 5 | GND–0.05 | – | $V_{CC}$+0.05 | V |
| DC Common–Mode Error | Over Analog Input Voltage Range | – | $\pm^1/_{16}$ | $\pm^1/_8$ | LSB |
| Power Supply Sensitivity | $V_{CC}$ = 5V ±10% Over Allowed $V_{IN}(+)$ and $V_{IN}(–)$ Voltage Range, Note 5 | | $\pm^1/_{16}$ | $\pm^1/_8$ | LSB |

Note 4. The NTE2053 A/D does not require a zero adjust.

Note 5. For $V_{IN}(–) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on–chip diodes are tied to each analog input which will forward conduct for analog input voltages one diode drop belwo GND or one diode drop greater than the $V_{CC}$ supply. Be careful, during testing at low $V_{CC}$ levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct – especially at elevated temperatures, and cause errors for analog inputs near full–scale. The spec allows 50mV forward bias of either diode. This means that as long as the analog $V_{IN}$ does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over temperature variations, initial tolerance, and loading.

**AC Electrical Characteristics:** ($V_{CC}$ = 5V, $T_A$ = +25°C unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Conversion Time | $T_C$ | $f_{CLK}$ = 640kHz, Note 7 | 103 | – | 114 | µs |
| | | Note 6, Note 7 | 66 | – | 73 | $1/f_{CLK}$ |
| Clock Frequency | $f_{CLK}$ | $V_{CC}$ = 5V, Note 6 | 100 | 640 | 1460 | kHz |
| Clock Duty Cycle | | Note 6 | 40 | – | 60 | % |
| Conversion Rate in Free–Running Mode | CR | $\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ = 0V, $f_{CLK}$ = 640kHz | – | – | 8770 | conv/s |
| Width of $\overline{WR}$ Input (Start Pulse Width) | $t_{W(\overline{WR})L}$ | $\overline{CS}$ = 0, Note 8 | 100 | – | – | ns |
| Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid) | $t_{ACC}$ | $C_L$ = 100pF | – | 135 | 200 | ns |
| TRI–STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi–Z State) | $t_{1H}$, $t_{0H}$ | $C_L$ = 10pF, $R_L$ = 10k | – | 125 | 200 | ns |
| Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$ | $t_{WI}$, $t_{RI}$ | | – | 300 | 450 | ns |
| Input Capacitance of Logic Control Inputs | $C_{IN}$ | | – | 5 | 7.5 | pF |
| TRI–STATE Output Capacitance (Data Buffers) | $C_{OUT}$ | | – | 5 | 7.5 | pF |

Note 6. Accuracy is guaranteed at $f_{CLK}$ = 640kHz. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275ns.

Note 7. With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched.

Note 8. The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrary wide pulse width will hold the converter on a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse.

**Electrical Characteristics (Cont'd):** ($V_{CC}$ = 5V, $T_A$ = 0° to +70°C unless otherwise specified)

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Control Inputs** (Note: CLK IN (Pin4) is the input of a Schmitt trigger circuit and is therefore specified separately) | | | | | | |
| Logical "1" Input Voltage (Except Pin4 CLK IN) | $V_{IN}(1)$ | $V_{CC}$ = 5.25V | 2.0 | – | 15 | V |
| Logical "0" Input Voltage (Except Pin4 CLK IN) | $V_{IN}(0)$ | $V_{CC}$ = 4.75V | – | – | 0.8 | V |
| Logical "1" Input Current (All Inputs) | $I_{IN}(1)$ | $V_{IN}$ = 5V | – | 0.005 | 1 | µA |
| Logical "0" Input Current (All Inputs) | $I_{IN}(0)$ | $V_{IN}$ = 0V | –1 | –0.005 | – | µA |
| **CLOCK IN and CLOCK R** | | | | | | |
| CLK IN (Pin4) Positive Going Threshold Voltage | $V_T+$ | | 2.7 | 3.1 | 3.5 | V |
| CLK IN (Pin4) Negative Going Threshold Voltage | $V_T–$ | | 1.5 | 1.8 | 2.1 | V |
| CLK IN (Pin4) Hysteresis $(V_T+)–(V_T–)$ | $V_H$ | | 0.6 | 1.3 | 2.0 | V |
| Logical "0" CLK R Output Voltage | $V_{OUT}(0)$ | $V_{CC}$ = 4.75V, $I_O$ = 360µA | – | – | 0.4 | V |
| Logical "1" CLK R Output Voltage | $V_{OUT}(1)$ | $V_{CC}$ = 4.75V, $I_O$ = –360µA | 2.4 | – | – | V |
| **Data Outputs and $\overline{INTR}$** | | | | | | |
| Logical "0" Output Voltage Data Outputs | $V_{OUT}(0)$ | $V_{CC}$ = 4.75V, $I_{OUT}$ = 1.6mA | – | – | 0.4 | V |
| $\overline{INTR}$ Outputs | | $V_{CC}$ = 4.75V, $I_{OUT}$ = 1.0mA | – | – | 0.4 | V |
| Logical "1" Output Voltage | $V_{OUT}(1)$ | $V_{CC}$ = 4.75V, $I_O$ = –360µA | 2.4 | – | – | V |
| | | $V_{CC}$ = 4.75V, $I_O$ = –10µA | 4.5 | – | – | V |
| TRI–STATE Disable Output Leakage (All Data Buffers) | $I_{OUT}$ | $V_{OUT}$ = 0V | –3 | – | – | µA |
| | | $V_{OUT}$ = 5V | – | – | 3 | µA |
| Source Current | $I_{SOURCE}$ | $V_{OUT}$ Short to GND, $T_A$ = +25°C | 4.5 | 6.0 | – | mA |
| Sink Current | $I_{SINK}$ | $V_{OUT}$ Short to $V_{CC}$, $T_A$ = +25°C | 9.0 | 16 | – | mA |
| **Power Supply** | | | | | | |
| Supply Current (Includes Ladder Current) | $I_{CC}$ | $f_{CLK}$ = 640kHz, $V_{REF}/2$ = NC. $T_A$ = +25°C, $\overline{CS}$ = "1" | – | 1.1 | 1.8 | mA |

## Functional Description:

The NTE2053 contains a circuit equivalent to the 256R network. Analog switches are sequenced by successive approximation logic to match the analog difference input voltage [$V_{IN}(+) – V_{IN}(–)$] to a corresponding tap on the R network. The most significant bit is tested first and after 8 comparisons (64 clock cycles) a digital 8–bit binary code (1111 1111 = full–scale) is transferred to an output latch and then an interrupt is asserted ($\overline{INTR}$ makes a high–to–low transition). A conversion in process can be interrupted by issuing a second start command. The device may be operated in the free–running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ input with $\overline{CS}$ = 0. To insure start–up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power–up cycle.

On the high–to–low transition of the $\overline{WR}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low. the A/D will remain in a reset state. *Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low–to–high transition*.

**Functional Description (Cont'd):**

The converter is started by having $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip–flop (F/F) and the resulting "1" level resets the 8–bit shift register, resets the interrupt (INTR) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 8–bit shift register. Internal clock signals then transfer this "1" to the Q output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is reset and the 8–bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would momentarily be at a "1" level) and the 8–bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.

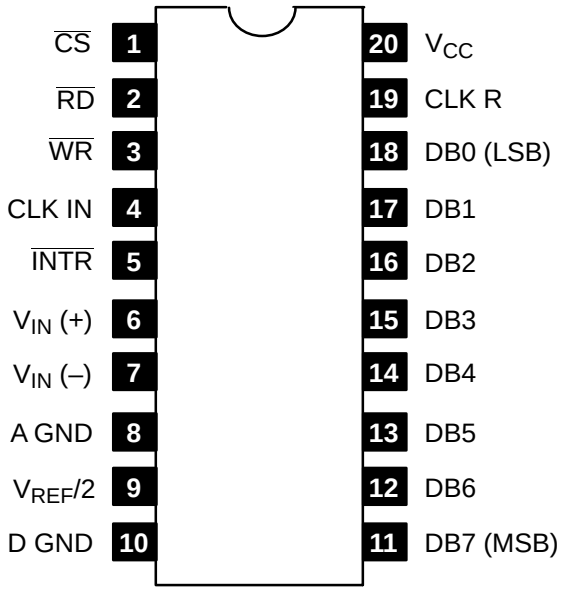
After the "1" is clocked through the 8–bit shift register (which completes the SAR search) it appears as the input to the D–type latch, LATCH 1. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the TRI–STATE output latches. When LATCH 1 is subsequently enabled, the Q output makes a high–to–low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{INTR}$ input signal.

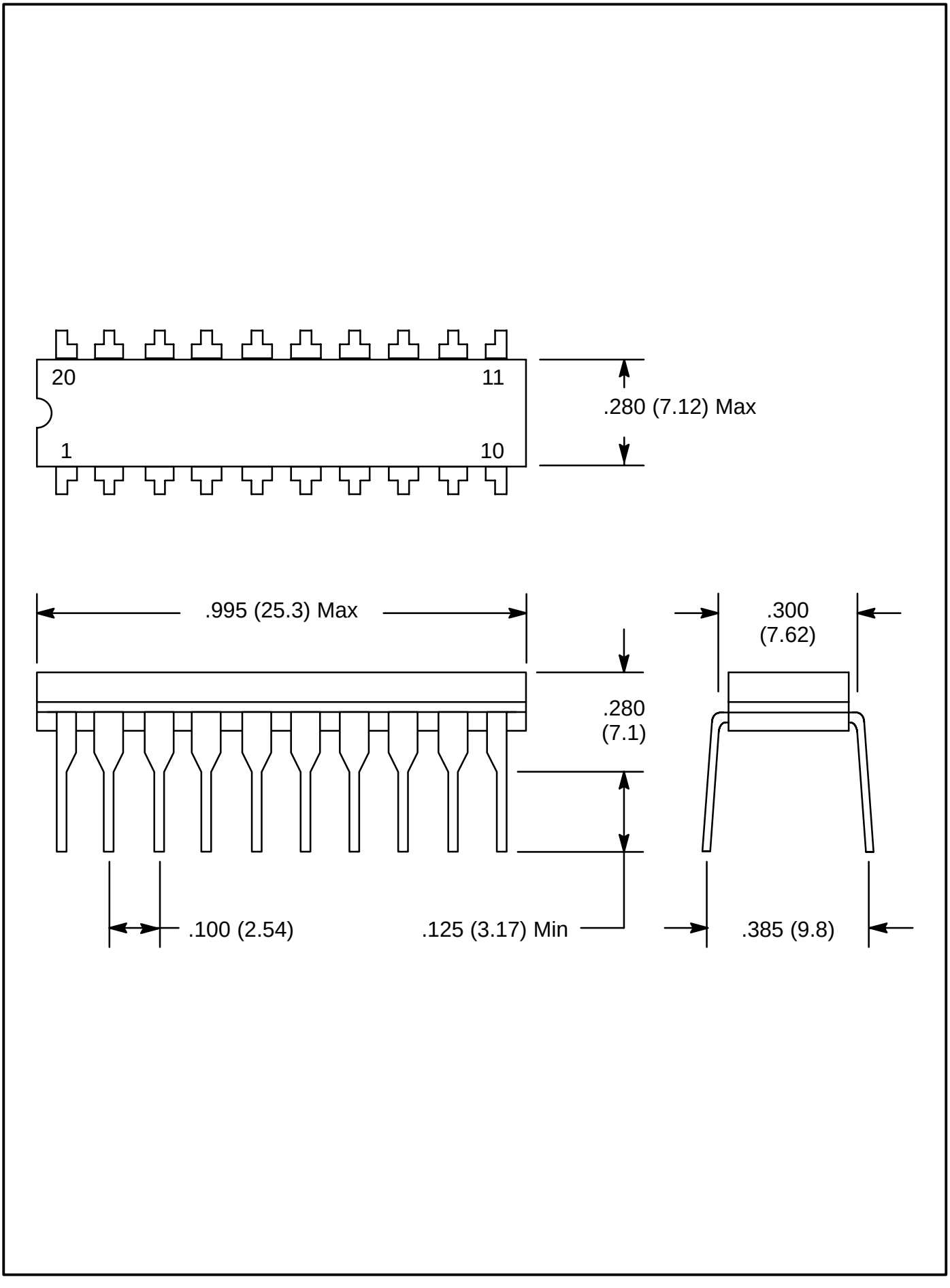
Note that the $\overline{SET}$ control of the INTR F/F remains low for 8 of the external clock periods (as the internal clocks run at $^1/_8$ of the frequency of the external clock). If the data output is continuously enabled ($\overline{CS}$ and $\overline{RD}$ both are held low), the $\overline{INTR}$ output will still signal the end of conversion (by a high–to–low transition), because the $\overline{SET}$ input can control the Q output of the INTR F/F even though the RESET input is constant at a "1" level in this operating mode. This $\overline{INTR}$ output will therefore stay low for the duration of the $\overline{SET}$ signal, which is 8 periods of the external clock frequency (assuming the A/D is not started during this interval).

When operating in the free–running or continuous conversion mode ($\overline{INTR}$ pin tied to $\overline{WR}$ and $\overline{CS}$ wired low), the START F/F is SET by the high–to–low transition of the $\overline{INTR}$ signal. This resets the SHIFT REGISTER which causes the input to the D–type latch, LATCH 1, to go low. As the latch enable input is still present, the $\overline{Q}$ output will go high, which then allows the INTR F/F to be RESET. This reduces the width of the resulting $\overline{INTR}$ output pulse to only a few propagation delays (approximately 300ns).

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the TRI–STATE output latches will be enables to provide the 8–bit digital outputs.

**Pin Connection Diagram**




20
11
1
10
.280 (7.12) Max
.995 (25.3) Max
.300
(7.62)
.280
(7.1)
.100 (2.54)
.125 (3.17) Min
.385 (9.8)