



ELECTRONICS, INC.
 44 FARRAND STREET
 BLOOMFIELD, NJ 07003
 (973) 748-5089

NTE2056 Integrated Circuit 8–Bit Multiplying Digital–to–Analog Converter

Description:

The NTE2056 is an 8–bit multiplying D–to–A converter in a 16–Lead DIP type package designed for use where the output current is a linear product of an eight–bit digital word and an analog input voltage.

Features:

- Fast Setting Time: 300ns Typ
- Non–Inverting Digital Inputs are MTTL and CMOS Compatible
- Output Voltage Swing: +0.4V to –5.0V
- High–Speed Multiplying Input: Slew Rate 4.0mA/μs
- Standard Supply Voltages: +5.0V and –5.0V to –15V

Applications:

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|--|------------------------------------|
| ● Tracking A–to–D Converters | ● Audio Digitizing and Decoding |
| ● Successive Approximation A–to–D Converters | ● Programmable Power Supplies |
| ● 2 1/2 Digit Panel Meters and DVM’s | ● Analog–Digital Multiplication |
| ● Waveform Synthesis | ● Digital–Digital Multiplication |
| ● Sample and Hold | ● Analog–Digital Division |
| ● Peak Detector | ● Digital Addition and Subtraction |
| ● Programmable Gain and Attenuation | ● Speech Compression and Expansion |
| ● CRT Character Generation | ● Stepping Motor Drive |

Absolute Maximum Ratings: ($T_A = +25^\circ\text{C}$ unless otherwise specified)

Power Supply Voltage	
V_{CC}	+5.5V
V_{EE}	–16.5V
Digital Input Voltage, V_5 thru V_{12}	0 to +5.5V
Applied Output Voltage, V_O	+0.5V, –5.2V
Reference Current, I_{14}	5mA
Reference Amplifier Inputs	
V_{14}	V_{CC}
V_{15}	V_{EE}
Operating Temperature Range, T_A	0° to +75°C
Storage Temperature Range, T_{stg}	–65° to +150°C

Electrical Characteristics: ($T_A = 0^\circ$ to $+75^\circ\text{C}$, $V_{CC} = +5\text{V}$, $V_{EE} = -15\text{V}$, $V_{ref}/R14 = 2\text{mA}$, All digital inputs at high logic level, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Relative Accuracy (Error relative to full scale I_O)	E_r	Note 1	–	–	± 0.78	%
Setting Time to within $\pm 1/2$ LSB (Includes t_{PLH})	t_S	$T_A = +25^\circ\text{C}$, Note 2	–	300	–	ns
Propagation Delay Time	t_{PLH} , t_{PHL}	$T_A = +25^\circ\text{C}$	–	30	100	ns
Output Full Scale Current Drift	TCI_O		–	–20	–	PPM/ $^\circ\text{C}$
Digital Input Logic Levels (MSB) High Level, Logic “1”	V_{IH}		2.0	–	–	V
Low Level, Logic “0”	V_{IL}		–	–	0.8	V
Digital Input Current (MSB) High Level	I_{IH}	$V_{IH} = 5\text{V}$	–	0	0.04	mA
Low Level	I_{IL}	$V_{IL} = 0.8\text{V}$	–	–0.4	–0.8	mA
Reference Input Bias Current (Pin15)	I_{15}		–	–1.0	–5.0	μA
Output Current Range	I_{OR}	$V_{EE} = -5\text{V}$	0	2.0	2.1	mA
		$V_{EE} = -15\text{V}$, $T_A = +25^\circ\text{C}$	0	2.0	4.2	mA
Output Current	I_O	$V_{ref} = 2.000\text{V}$, $R14 = 1000\Omega$	1.9	1.99	2.1	mA
	I_O (min)	All bits low	–	0	4.0	μA
Output Voltage Compliance	V_O	$E_r \leq 0.19\%$, $T_A = +25^\circ\text{C}$ Pin1 Grounded	–	–	–0.55, +0.4	V
		Pin1 Open, V_{EE} below -10V	–	–	–5.0, +0.4	V
Reference Current Slew Rate	$SR I_{ref}$		–	4.0	–	mA/ μs
Output Current Power Supply Sensitivity	PSRR(–)		–	0.5	2.7	$\mu\text{A}/\text{V}$
Power Supply Current	I_{CC}	All bits low	–	+13.5	+22.0	mA
	I_{EE}		–	–7.5	–13.0	mA
Power Supply Voltage Range	V_{CCR}	$T_A = +25^\circ\text{C}$	+4.5	+5.0	+5.5	V
	V_{EER}		–4.5	–15.0	–16.5	V
Power Dissipation All bits low	P_D	$V_{EE} = -5\text{V}$	–	105	170	mW
		$V_{EE} = -15\text{V}$	–	190	305	mW
		$V_{EE} = -5\text{V}$	–	90	–	mW
		$V_{EE} = -15\text{V}$	–	160	–	mW
All bits high						

Note 1. All current switches are tested to guarantee at least 50% of rated output current.

Note 2. All bits switched.

Pin Connection Diagram

