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NTE2062
Integrated Circuit
PMOS Digital Alarm Clock

Features:
- Single–Chip ED MOS LSI
- LED Direct Drive by Time–Sharing (Duplex)
- Wide Operating Voltage Range
- Alarm on a 24–Hour Basis
- Two Selections of Time Format:
  AM/PM 12–Hour Basis & 24–Hour Basis
- On–Chip CR Oscillator for Battery Backup
- 50Hz or 60Hz Reference Frequency
- Automatic Advance Capable:
  “Hours”, “Minutes”
- Sleep Timer:
  Max. 59 Minutes or 1Hour, 59 Minutes
- Repeatedly Usable Snooze
- Power Failure Indicator
- 900Hz Output for Alarm Tone

Functions:
- Real Time Display
- Alarm with Snooze
- Sleep Timer

Applications:
- Alarm Clock
- Clock Radio

Absolute Maximum Ratings: (V_{SS} = 0, T_A = +25°C unless otherwise specified)

Maximum Supply Voltage, V_{DD}max . . . . . –15 to +0.3V
Input Voltage, V_{IN}
  50/60Hz . . . . . –15 to +0.3V
  Other Than 50/60Hz . . . . . –15 to +0.3V
Output Voltage, V_{OUT} . . . . . –15 to +0.3V
Input Clamp Current, I_{IN} . . . . . –0.4 to +0.4mA
Allowable Power Dissipation (T_A = +70°C), $P_D$max 700mW
Operating Temperature Range, T_{opr} . . . . . –30° to +70°C
Storage Temperature Range, T_{stg} . . . . . –55° to +125°C

Allowable Operating Ranges: (V_{SS} = 0, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		–14	–	–7.5	V
Input “HIGH” Level Voltage	V_{IH}	50/60Hz Input	–1.0	–	–	V
		Other Than 50/60Hz Input	–1.5	–	–	V
Input “LOW” Level Voltage	V_{IL}	50/60Hz	–	–	V_{DD}+2	V
		Other Than 50/60Hz	–	–	V_{DD}+2	V
Input Voltage on 50/60Hz	$V_{AC–IN}$	Referenced to V_{SS}	V_{LED}	–	–	V

Electrical Characteristics: (V_{DD} = –12V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input "HIGH" Level Current	I_{IH}	$V_{IN} = V_{SS}$, 50/60Hz	–	–	10	µA
		$V_{IN} = V_{DD}$, Input Pins other than 50/60Hz	–	–	20	µA
Input "LOW" Level Current	I_{IL}	$V_{IN} = V_{DD}$, 50/60Hz	–	–	10	µA
		$V_{IN} = V_{DD}$, Input Pins other than 50/60Hz	–	–	10	µA
Output "HIGH" Level Current	I_{OH}	Alarm Out, Sleep Out, $V_{OH} = V_{SS}$–1V	5	–	–	mA
		10's Hr ag & de (24Hr Mode), $V_{OUT} = V_{SS}$–1V	36	–	–	mA
		Segment Outputs other than above, $V_{OUT} = V_{SS}$–1V	18	–	–	mA
Output Leakage Current	I_{OF}	Alarm Out, Sleep Out, $V_{OUT} = V_{DD}$	–	–	10	µA
		10's Hr ag & de (24Hr Mode), $V_{OUT} = V_{DD}$	–	–	20	µA
		Segment Outputs other than above, $V_{OUT} = V_{DD}$	–	–	20	µA
Power Failure Detect Voltage	V_{DD}		–7.5	–5.0	–	V
Current Dissipation	I_{CC}	Output: OFF, Input with Pull–Down Resistor: Open	–	5	7	mA
Stability of Oscillator for Backup	F_S	Typical value, 900Hz, V_{DD} = –9V ±10%	–10	–	+10	%
Accuracy of Oscillator for Backup	F_A	Typical value, 900Hz, V_{DD} = –9V ±10%	–10	–	+10	%

Operation Description:

50Hz/60Hz Input:

The On–Chip Schmitt Trigger circuit allows a simple RC filter at the input to remove possible line voltage transients. An internal pull–up resistor is provided.

CR Input: (Note 1)

When AC power–down occurs, the time counter enters the "hold" mode and the on–chip clock oscillator starts operating immediately. If there is no input at "50/60Hz input" during 3–clock period, this oscillator controls the time counter advance instead of "50/60Hz input". The values of CR determine the frequency of the on–chip clock oscillator. All segment outputs are off during backup operation. If the backup OSC is used at the power–down mode, "50/60Hz input" must be open or at V_{SS} level.

50/60Hz Select Input:

Connecting "50/60Hz select" to V_{SS} enables 50Hz operation. For 60Hz operating, "50/60Hz select" is left unconnected: Pull–down to V_{DD} is provided by the internal pull–down resistor.

Display Mode Select Input (Alarm Display/Sleep Display):

The internal pull–down resistor allows the use of 2 SPST (single–pole single–throw) switches to select 4 display modes listed in Table 1.

Table 1. Display Mode

Select Input		Display Mode	Digit No.1	Digit No. 2	Digit No. 3	Digit No. 4
Alarm	Sleep					
N.C.	N.C.	Time Display	10's Hour, AM/PM	Hour	10's Minute	Minute
V_{SS}	N.C.	Alarm Display	10's Hour, AM/PM	Hour	10's Minute	Minute
N.C.	V_{SS}	Sleep Display	Blanked	Hour	10's Minute	Minute
V_{SS}	V_{SS}	Seconds Display	Blanked	Minute	10's Second	Second

Note 1. If V_{SS} is applied to 2 input of "alarm display" and "sleep display" simultaneously, the seconds display mode is entered.

Operation Description (Cont'd):

Time Setting Input:

Two setting inputs for 'Hours' and 'Minutes' are provided. The application of V_{SS} causes the time setting in Table 2 to occur. An internal pull–down resistor each is provided.

Table 2. Setting Contents

Display Mode	Set Input	Functions
Time	Hour	'Hours' are incremented +1 immediately and advance at a 2Hz rate 1/4 to 3/4 seconds later.
	Minute	'Minutes' are incremented +1 immediately and advance at a 2Hz rate 1/4 to 3/4 seconds later.
	Both	Both operations shown above are preformed.
Seconds (Alarm & Sleep)	Hour (Note 2)	'Seconds' are cleared to [00].
	Minute	"Hold" mode.
	Both (Note 3)	'Hours" and 'Minutes' are reset to [0:00] (24–Hour basis) or [12:00] (12–Hour basis)
Alarm	Hour	'Hours' are incremented +1 immediately and advance at a 2Hz rate 1/4 to 3/4 seconds later.
	Minute	'Minutes' are incremented +1 immediately and advance at a 2Hz rate 1/4 to 3/4 seconds later.
	Both	'Hours" and 'Minutes' are reset to [0:00] (24–Hour basis) or [12:00] (12–Hour basis)
Sleep	–	The moment V_{DD} is applied to "Sleep Display", the sleep counter is set to [:59].
	Hour	The moment V_{DD} is applied to "Sleep Display" and "Hour Set" simultaneously, the sleep counter is set to [1:59].
	Minute	The sleep counter counts down at a 2Hz rate.
	Both	The sleep counter counts down at a 2Hz rate.

Note 2. When "Seconds" display is at 50 to 59, "Seconds" are reset to [00] and a carry occurs to increment "Minutes" +1.

Note 3. Once the reset mode or hold mode is entered, another function is locked until both "Hour Set" input and "Minute Set" inputs are released.

12/24–Hour Select Input:

Leaving this pin unconnected (V_{DD}) causes the 12–Hour basis to be selected; connecting this pin to V_{SS} causes the 24–Hour basis to be selected. An internal pull–down resistor is provided.

Power Failure Indicator:

If the power supply voltage drops and is applied again, all the on–segments flash and the power failure indication mode is entered. The power failure indication mode is released by applying V_{SS} to "Hour Set" or "Minute Set".

Alarm Operation and Alarm Output:

When the alarm set time is reached, the alarm signal is delivered. This signal continues to be delivered for 1 hour 59 minutes unless reset by "Alarm Off" or "Snooze Input". This signal is provided for the tone–signal of 900Hz with 50% duty of 2Hz gated. A simple LPF can be used to turn this alarm signal into DC signal as required.

Snooze Input:

By momentarily connecting this pin to V_{SS} at the alarm on–state, the alarm output is inhibited for 8 to 9 minutes, after which the alarm signal is delivered again. The snooze function can be used repeatedly for 1 hour 59 minutes. An internal pull–down resistor is provided. By connecting "Snooze Input" to V_{SS} at the alarm off–state, the sleep timer counter is reset to [0:00]. (The sleep timer is reset with one touch).

Operation Description (Cont'd):

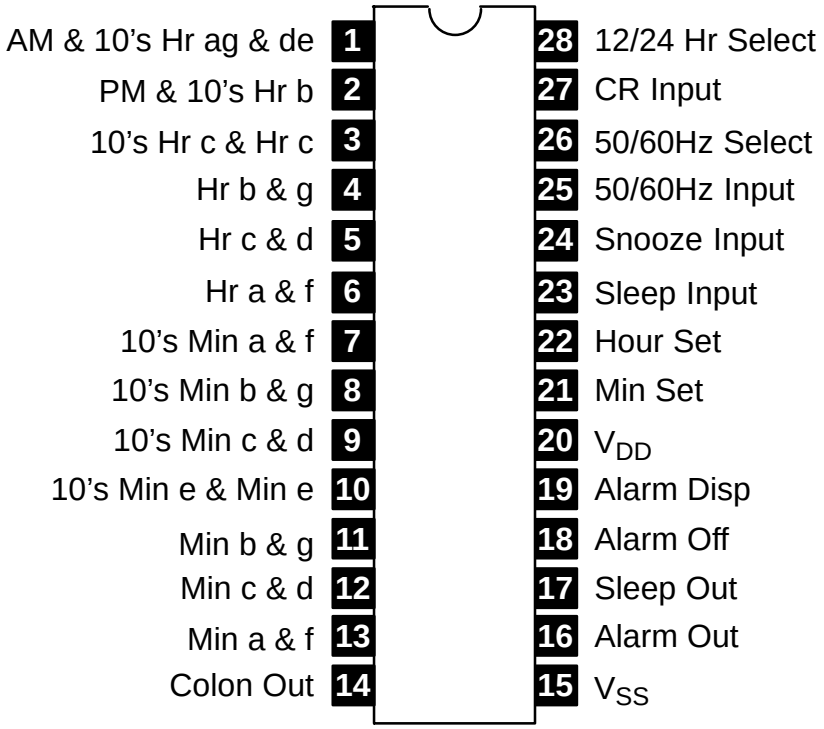
Alarm Off Input:

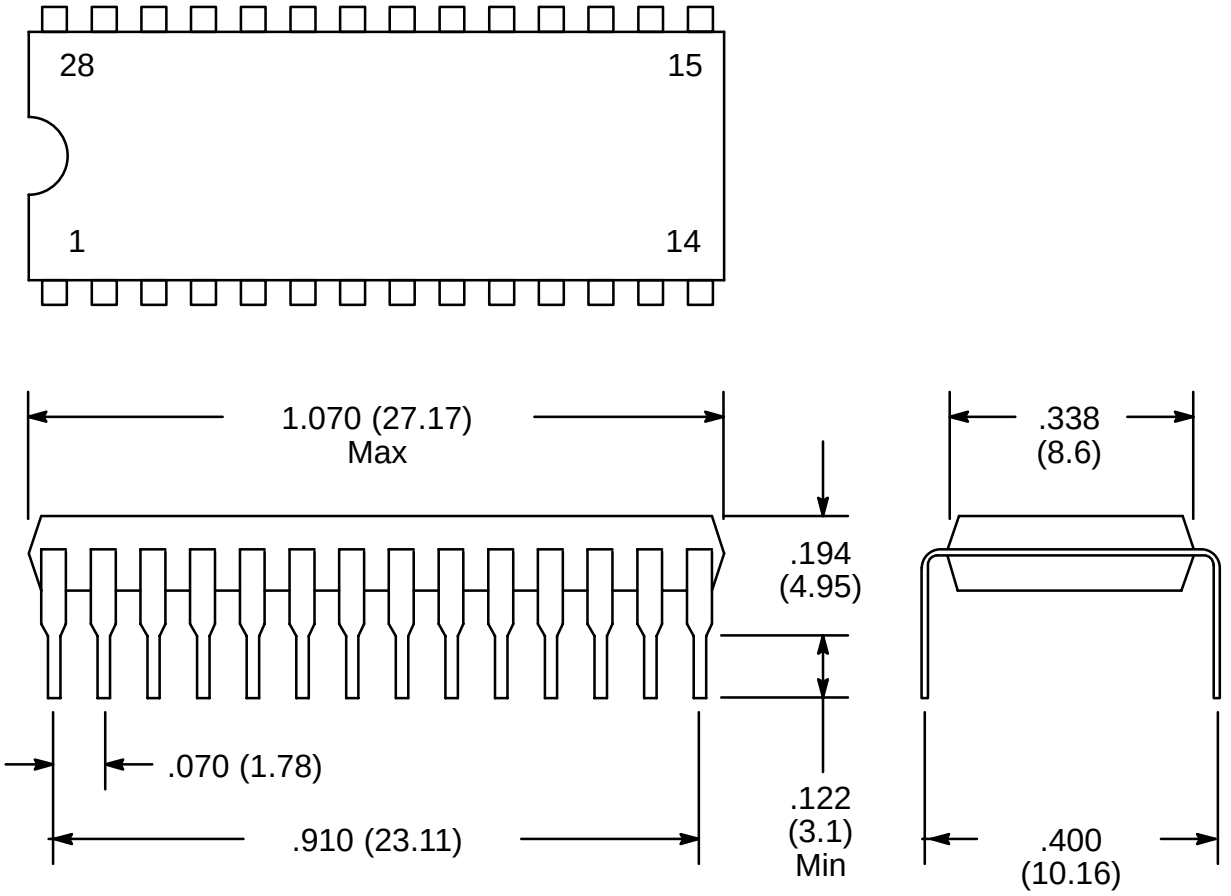
Connecting this input pin to V_{SS} inhibits the alarm output momentarily. An internal pull–down resistor is provided.

Sleep Timer and Sleep Output:

The sleep output can be used to keep the radio turned on for any period of time up to 59 minutes or 1 hour 59 minutes. Table 2 shows how to select the period (59 minutes or 1 hour 59 minutes). This sleep timer uses a down counter. When the counter contents reach [00], the output stops being delivered, turning off the radio. By connecting "Snooze Input" to V_{SS} at the sleep output on–state, the sleep output is inhibited.

Pin Connection Diagram




28
15
1
14
1.070 (27.17)
Max
.194
(4.95)
.070 (1.78)
.910 (23.11)
.122
(3.1)
Min
.338
(8.6)
.400
(10.16)