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NTE2102
Integrated Circuit
NMOS, 1K Static RAM (SRAM), 350ns

Description:

The NTE2101 is a high–speed 1024 x 1 bit static random access read/write memory in a 16–Lead DIP type package designed using N–Channel depletion mode silicon gate technology. Static storage cells eliminate the need for clock or refresh circuitry.

Low threshold silicon gate N–Channel technology allows complete DTL/TTL compatibility of all inputs and outputs as well as a single 5V supply. The separate chip enable input ($\overline{CE}$) controlling the output allows easy memory expansion by OR–tying individual devices to a data bus. Data in and data out have the same polarity.

Features:

- Single 5V Supply
- All Inputs and Outputs Directly DTL/TTL Compatible
- Static Operation – No Clocks or Refresh
- All Inputs Protected Against Static Charge
- 350ns Access Time

Absolute Maximum Ratings: (Note 1)

Voltage at Any Pin . . . . . 0.5V to +7V
Power Dissipation, P_D 1W
Storage Temperature Range, T_{stg} . . . . . –65° to +150°C
Lead Temperature (During Soldering, 10sec), T_L . . . . . +300°C

Note 1. “Absolute Maximum Ratings” are those values beyond which the device may be permanently damaged. They do not mean the device may be operated at these values.

Recommended Operating Conditions:

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		4.75	–	5.25	V
Operating Ambient Temperature	T_A		0	–	+70	°C
Input Low Voltage	V_{IL}		–0.5	–	0.8	V
Input High Voltage	V_{IH}		2.0	–	V_{CC}	V

DC Electrical Characteristics: (T_A = 0° to +70°C, V_{CC} = 5V ±5% unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Load Current	I_{LI}	V_{IN} = 0 to 5.25V	–	–	10	µA
Output Leakage Current, High	I_{LOH}	$\overline{CE}$ = 2V, V_{OUT} = 2.4V	–	–	5	µA
Output Leakage Current, Low	I_{LOL}	$\overline{CE}$ = 2V, V_{OUT} = 0.4V	–	–	–10	µA
Power Supply Current	I_{CC}	All Inputs = 5.25V, Data Output Open, T_A = +25°C	–	–	45	mA
Power Supply Amp	I_{CC}	All Inputs = 5.25V, Data Output Open, T_A = 0°C	–	–	50	mA
Output Low Voltage	V_{OL}	I_{OL} = 3.2mA	–	–	0.4	V
Output High Voltage	V_{OH}	I_{OH} = –200µA	2.4	–	–	V

AC Electrical Characteristics (With Standard Load): (T_A = 0° to +70°C, V_{CC} = 5V ±5% unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Read Cycle						
Read Cycle	t_{RC}		350	–	–	ns
Access Time	t_A		–	–	350	ns
Chip Enable to Output Time	t_{CO}		–	–	150	ns
Previous Read Data Valid with Respect to Address	t_{OH1}		40	–	–	ns
Previous Read Data Valid with Respect to Chip Enable	t_{OH2}		0	–	–	ns
Write Cycle						
Write Cycle	t_{WC}		350	–	–	ns
Address to Write Set–Up	t_{AW}		20	–	–	ns
Write Pulse Width	t_{WP}		150	–	–	ns
Write Recovery Time	t_{WR}		0	–	–	ns
Data Set–Up Time	t_{DW}		125	–	–	ns
Data Hold Time	t_{DH}		0	–	–	ns
Chip Enable to Write Set–Up	t_{CW}		150	–	–	ns

AC Electrical Characteristis: (T_A = +25°C, f = 1MHz unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Capacitance						
Input Capacitance	C_{IN}	All Inputs V_{IN} = 0V	–	3	5	pF
Output Capacitance	C_{OUT}	V_O = 0V	–	4	6	pF

Standby Characteristics: (T_A = 0° to +70°C, Note 2 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{CC} in Standby	V_{PD}		1.5	–	–	V
$\overline{CE}$ Bias in Standby	V_{CES}	$2 \le V_{PD} \le V_{CC}$max	2.0	–	–	V
		$1.5 \le V_{PD} \le 2$	V_{PD}	–	–	V

Note 2. Typical values at T_A = +25°C.

Standby Characteristics (Cont'd): (T_A = 0° to +70°C, Note 2 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Standby Current	I_{PD}	All Inputs = V_{PD} = 1.5V	–	–	28	mA
		All Inputs = V_{PD} = 2V	–	–	38	mA
Chip Deselect to Standby Time	t_{CP}		0	–	–	ns
Recovery Time	t_R	Note 3	t_{RC}	–	–	ns

Note 2. Typical values at T_A = +25°C.

Note 3. $t_R = t_{RC}$ = Read Cycle Time.

Pin Connection Diagram