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NTE3094
Optoisolator
Dual, High Speed, Open Collector NAND Gate

Description:

The NTE3094 consists of a pair of inverting optically coupled gates each with a GaAsP emitting diode and a unique integrated detector. The photons are collected in the detector by a photodiode and then amplified by a high gain linear amplifier that drives a Schottky clamped open collector output transistor. each circuit is temperature, current and voltage compensated.

This unique isolator design provides maximum DC and AC circuit isolation between input and output while achieving LSTTL/TTL circuit compatibility. The isolator operational parameters are guaranteed from 0° to +70°C, such that a minimum input current of 5mA will sink an eight gate fan–out (13mA) at the output with 5 volt V_{CC} applied to the detector. This isolation and coupling is achieved with a typical propagation delay of 57ns.

Features:

- LSTTL/TTL Compatible: 5V Supply
- Ultra High Speed
- Low Input Current Required
- High Common Mode Rejection
- 3000V DC Withstand Test Voltage
- Typical Data Rate 10M/Bit(s)

Absolute Maximum Ratings: (T_A = +25°C unless otherwise specified)

Input Diode (Each Channel)

Reverse Voltage, V_R 5V

Forward Current, I_F

Average 15mA

Peak (≤ 1ms Duration) 30mA

Output Transistor (Each Channel)

Supply Voltage (1 Minute Maximum), V_{CC} 7V

Output Voltage, V_O 7V

Output Current, I_O 16mA

Collector Power Dissipation, P_D 60mW

Total Device

Operating Temperature Range, T_{opr} . . . . . 0° to +70°C

Storage Temperature Range, T_{stg} . . . . . –55° to +125°C

Lead Temperature (During Soldering, 1.6mm below seating plane, 10sec Max), T_L . . . . . +260°C

Recommended Operating Conditions:

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Current, Low Level (Each Channel)	I_{FL}		0	–	250	µA
Input Current, High Level (Each Channel)	I_{FH}	Note 1	6.3	–	15	mA
Supply Voltage, Output	V_{CC}		4.5	–	5.5	V
Fan Out (TTL Load)	N		–	–	8	
Operating Temperature	T_A		0	–	70	°C

Note 1. 6.3mA condition permits at least 20% CTR degradation guardband. Initial switching threshold is 5mA or less.

Electrical Characteristics: (T_A = 0° to +70°C, Note 2 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High Level Output Current	I_{OH}	V_{CC} = 5.V, V_O = 5.5V, I_F = 250µA, Note 3	–	40	250	µA
Low Level Output Voltage	V_{OL}	V_{CC} = 5.5V, I_F = 5mA, $I_{OL(sinking)}$ = 13mA, Note 3	–	0.4	0.6	V
High Level Supply Current	I_{CCH}	V_{CC} = 5.V, I_F = 0, (Both Channels)	–	15	30	mA
Low Level Supply Current	I_{CCL}	V_{CC} = 5.V, I_F = 10mA, (Both Channels)	–	27	36	mA
Input–Output Insulation Leakage Current	I_{IO}	Relative Humidity = 45%, T_A = +25°C, t = 5s, V_{IO} = 3000V DC, Note 4	–	–	1.0	µA
Resistance	R_{IO}	V_{IO} = 500V, T_A = +25°C, Note 4	–	10^{12}	–	Ω
Capacitance	C_{IO}	f = 1MHz, T_A = +25°C, Note 4	–	0.6	–	pF
Input Forward Voltage	V_F	I_F = 10mA, T_A = +25°C, Note 3, Note 5	–	1.5	1.75	V
Input Reverse Breakdown Voltage	$V_{(BR)R}$	I_R = 10µA, T_A = +25°C	5	–	–	V
Input Capacitance	C_{IN}	V_F = 0, f = 1MHz, Note 3	–	60	–	pF
Current Transfer Ratio	CTR	I_F = 5mA, R_L = 100Ω, Note 6	–	700	–	%
Resistance (Input–Input)	R_{II}	V_{II} = 500V, Note 7	–	10^{11}	–	Ω
Capacitance (Input–Input)	C_{II}	f = 1MHz, Note 7	–	0.27	–	pF

Note 2. All typicals at T_A = +25°C, V_{CC} = 5V unless otherwise specified.

Note 3. Each channel.

Note 4. Measured between Pin1, Pin2, Pin3 and Pin4 shorted together and Pin5, Pin6, Pin7 and Pin8 shorted together.

Note 5. At 10mA, V_F decreases with increasing temperature at the rate of 1.6mV/°C.

Note 6. DC Current Transfer Ratio is defined as the ratio of the output collector current to the forward bias input current times 100%.

Note 7. Measured between Pin1 and Pin2 shorted together and Pin3 and Pin4 shorted together.

Switching Characteristics: (T_A = +25°C, V_{CC} = 5V unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Typ	Max	Unit
Propagation Delay Time	t_{PLH}	I_F = 7.5mA, R_L = 350Ω, C_L = 15pF	Note 8	–	57	75	ns
	t_{PHL}		Note 9	–	45	75	ns
Output Rise Time (10% to 90%)	t_r	I_F = 7.5mA, R_L = 350Ω, C_L = 15pF, Note 3		–	25	–	ns
Output Fall Time (90% to 10%)	t_f			–	35	–	ns
Common Mode Transient Immunity	CM_H	I_F = 0mA, $V_{O(min)}$ = 2V	V_{CM} = 10V_{P-P}, R_L = 350Ω	–	500	–	V/µs
	CM_L	I_F = 7.5mA, $V_{O(max)}$ = 0.8V		–	–500	–	V/µs

Note 3. Each channel.

Note 8. The t_{PLH} propagation delay is measured from the 3.75mA point on the trailing edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.

Note 9. The t_{PHL} propagation delay is measured from the 3.75mA point on the leading edge of the input pulse to the 1.5V point on the leading edge of the output pulse.

Note 10. Common mode transient immunity in Logic High level is the maximum tolerable (positive) dv cm/dt on the leading edge of the common mode pulse (V_{CM}) to assure that the output will remain in a Logic High state (i.e. V_O 2.0V). Common mode transient immunity in Logic Low level is the maximum tolerable (negative) dc cm/dt on the trailing edge of the common mode pulse signal (V_{CM}) to assure that the output will remain in a Logic Low state (i.e. V_O 0.8V).

Pin Connection Diagram