NEXFLASH® Technologies, Inc.

PRELIMINARY
SEPTEMBER 2002

NX26F640C

64M-BIT SERIAL FLASH MEMORY WITH 2-PIN NXS2 INTERFACE

Table of Contents

Table of Contents

FEATURES

- **64M-bit Serial Flash Memory**
- **Flash storage for systems with limited pins, space, and power**
  - Ideal for high density serial code-download
  - Data, voice and image storage
  - Battery-operated products
- **Nonvolatile Memory Technology**
  - Single transistor EEPROM memory
  - 16,384 sectors of 522 bytes each
  - Sector erase/write time of 10 ms/sector (typical)
  - Ten year data retention
- **2-pin NXS2 Serial Interface**
  - Simple clock and data interface
  - Easily interfaces to popular microcontrollers
  - Clock operation as fast as 16MHz
  - Cascade up to eight devices
- **Ultra-low Power for Battery-Operation**
  - Single 2.7-3.6V supply for Read, Erase/Write
  - 1 µA standby, 5 mA active (typical)
- **Special Features**
  - Two on-board 522-byte SRAM Buffers
  - Byte-level addressing
  - Configurable software write-protection
- **Package Options**
  - 32-pin TSOP (Type I)
  - Removable Cards and Modules

DESCRIPTION

The NX26F640C Serial Flash memory provide a storage solution for systems which are limited in power, pins, space, hardware and firmware resources. The NX26F640C is ideal for applications that store voice, images and data in a portable/mobile environment as well for down-loading code into controllers with embedded DRAM or SRAM. The NX26F640C operates on a single 2.7V-3.6V power supply for read and erase/write with typical current consumption as low as 5mA active and less than 1uA standby. The array is organized into 16,384 sectors of 522 bytes each. Sector erase/write speeds are as fast as 10ms. The 2-pin NXS2 serial interface is easily controlled by popular micro-controllers and can cascade up to eight devices on the same time signals. Special features include dual on-chip serial SRAM, byte-level addressing, hardware/software write protection and removable Serial Flash Module packaging option. Development is supported with the PC-based NexFlash Serial Flash Development Kit.

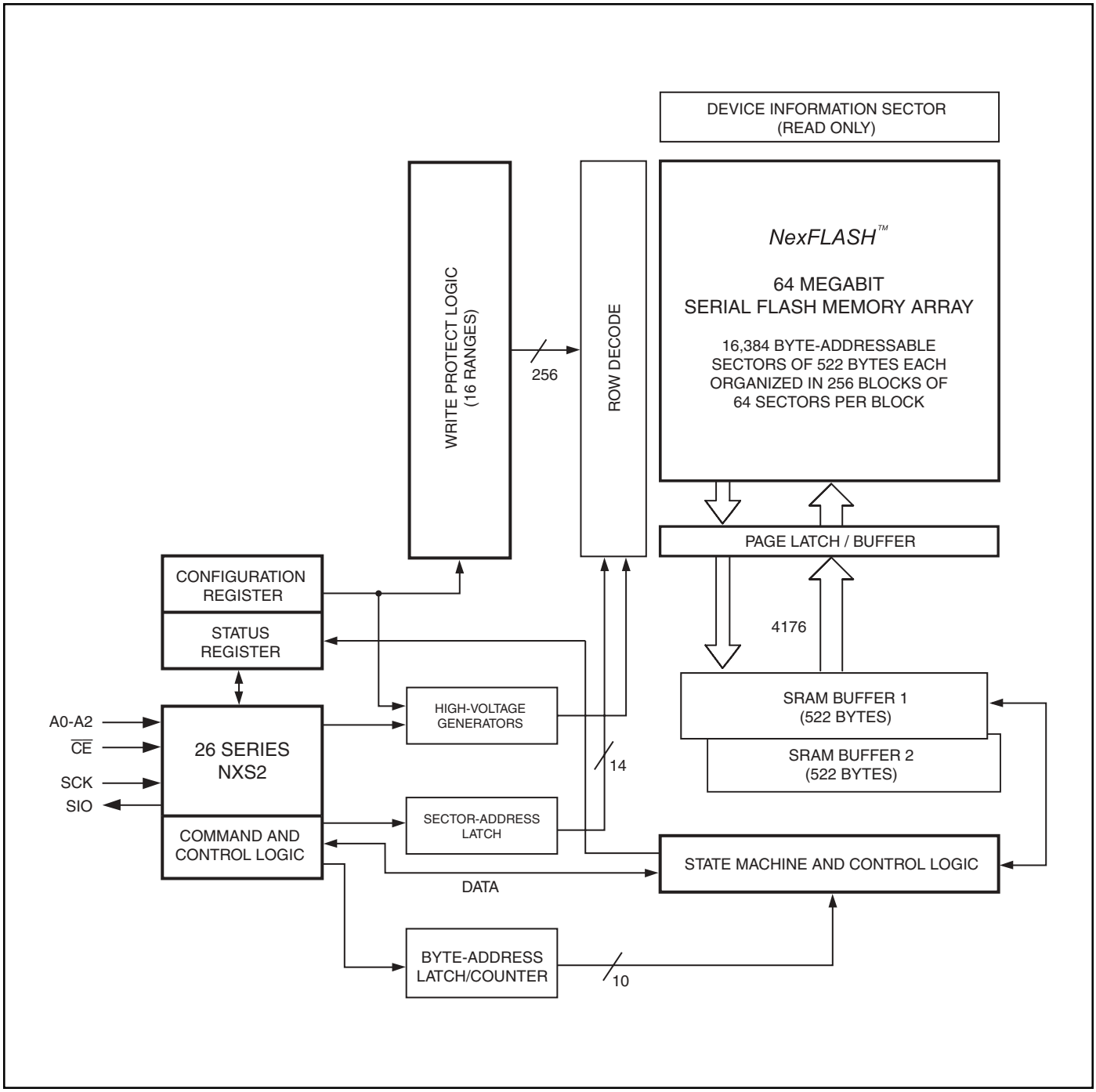


Figure 1. NX26F640C Architectural Block Diagram

Pin Descriptions

Pin Assignments
The NX26F640C is available in a 32-Pin TSOP, Type I (T Package) with an NXS2 Interface (figure 2).

Static Address (A0, A1, A2)
The static address bits allow up to 8 chips to be connected on the same SCK and SIO pins. The NXS2 protocol selects the chip to address in the first byte of the command bit stream by matching the Device Address Field (DA2..0) to the A2..A0 pins (figure 3).

Serial Data Input/Output (SIO)
The SIO pin transmits data into and out of the device with the SCK pin. All data transmitted to or from the chip is clocked relative to the rising edge of SCK.

Serial Clock Input (SCK)
All commands and data written to the SIO pin or read from the SIO pin are clocked relative to the rising edge of SCK. When the device is reset, the first low to high transition of the clock wakes the device up, the second low to high transition clocks the first command bit to the device on SIO. When the SIO line switches from an input to an output, the first transition of the clock switches the direction of the SIO line to an output.

Chip Enable (CE\)
The Chip Enable pin, when active (low), allows the device to decode the bit stream on the SCK and SIO pins. When the Chip Enable pin is not active (high), the device ignores any bit stream present on the SCK and SIO pins.

Power Supply Pins (Vcc and Gnd)
The NX26F160 supports a single power supply between 2.7V and 3.6V connected to the Vcc and Gnd pins.

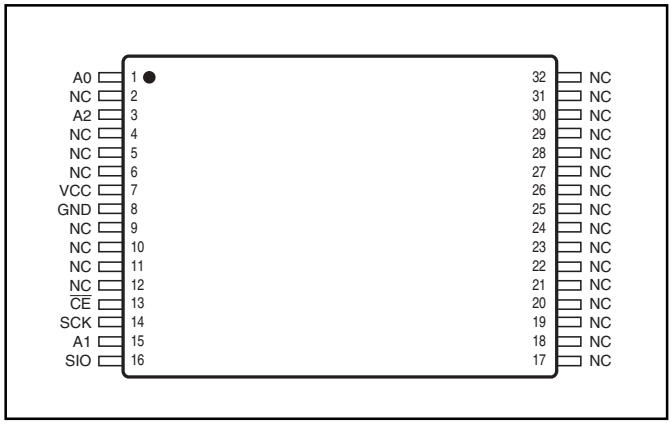


Figure 2. NX26F640C Pin Assignments
NXS2 Interface, 32-Pin TSOP, Type I (T Package)

Table 1. Pin Descriptions

A0, A1, A2	Device Address
SIO	Serial Data Input/Output
SCK	Serial Clock Input
$\overline{CE}$	Chip Enable
VCC	Power Supply
GND	Ground
NC	No Connect

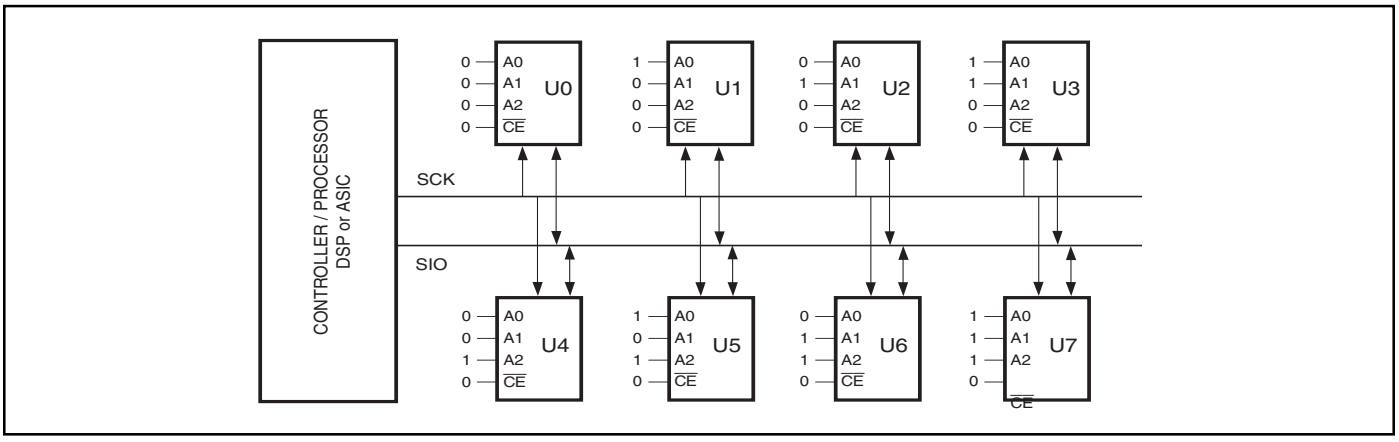


Figure 3. NX26F640 Used in a Multi-device Configuration with up to 8-Devices on the same two signals

Serial Flash Memory Array

The NX26F640C Serial Flash memory array is organized as 16,384 sectors of 522-bytes (4,176 bits) each, as shown in Figure 4. The block size of the device is 64 sectors, yielding 256 blocks for the NX26F640C.

The Serial Flash memory of the NX26F640C is byte-addressable for read operations. This allows a single byte, or specified sequence of bytes, to be read without having to clock an entire 522-byte sector out of the device. All data is read through one of two 522-byte SRAM buffers by using the Transfer Sector to SRAM and Read SRAM commands. Data can be written to the Flash memory array one sector (522-bytes) at a time through the Serial SRAM using a *Write to Sector* command or a *Transfer SRAM to Sector* command. No pre-erase is needed. Instead, the device incorporates an auto-erase-before-write feature that automatically erases the addressed sector at the beginning of the write operation. After completing the command the memory array will become busy while it is programming the specified non-volatile memory cells of that sector. This busy time will not exceed t_{WP} during which time the Flash array is unavailable for read or write access. The device can be tested to determine the array's availability using the Ready/Busy status that is available during most read commands, through the status register, or on the Ready/Busy pin.

Restricted Sector (-R) Devices

Restricted sector devices provide a more cost-effective alternative to standard devices that have 100% valid sectors. Restricted sector devices have a limited numbers of sectors (maximum of 64) that do not meet manufacturing criteria over the specified operating range. Restricted sector devices are factory-formatted with a list of the factory tested restricted sector addresses is stored in the device information sector which is assessable with command 15H. See Device Information Sector (DIS) specification. Please note that standard devices, with 100% valid sectors, are not formatted with the first byte set to C9H.

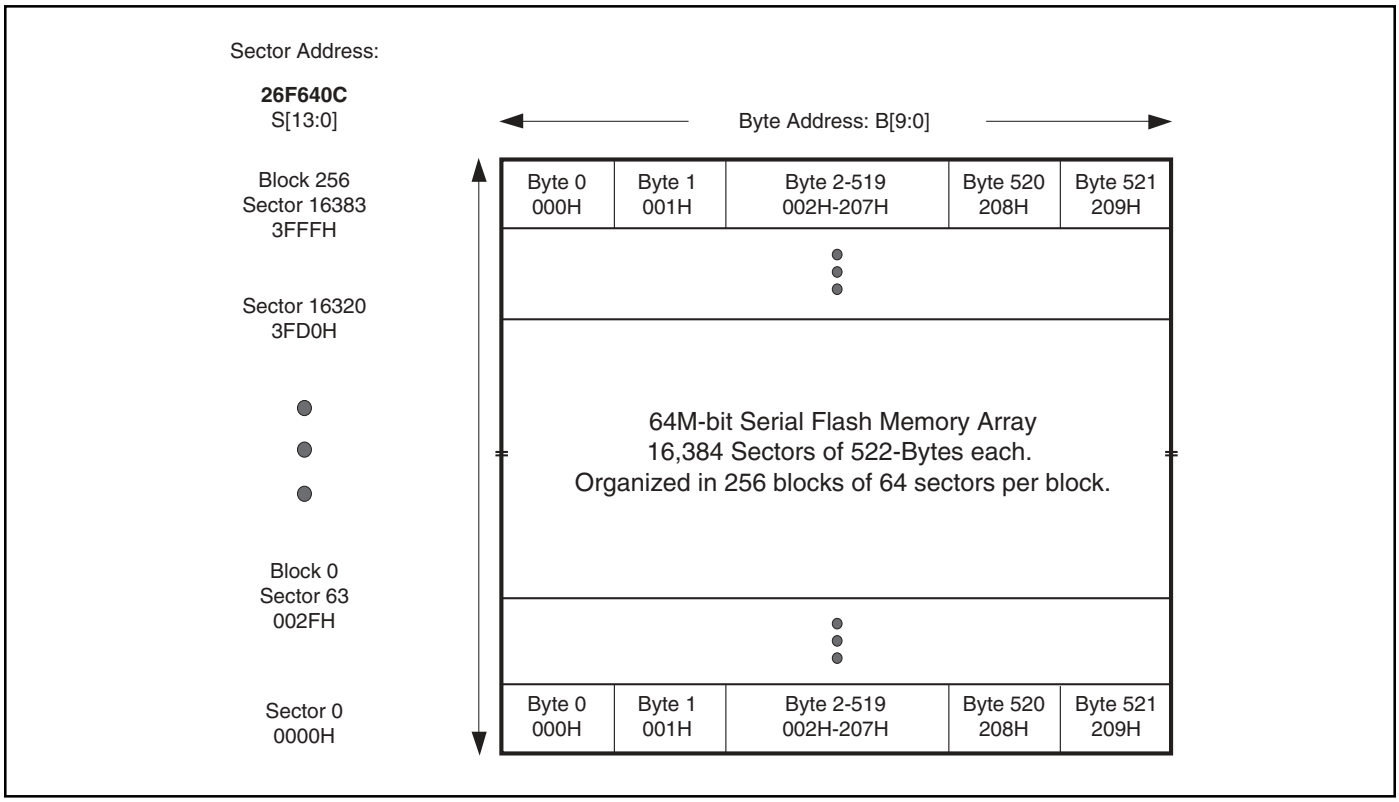


Figure 4. NX26F640C Serial Flash Memory Array

Serial SRAM

One of the most powerful features of the NX26F640C is the integrated dual Serial SRAMs. The main purpose of the Serial SRAMs is to serve as a buffer for sector data to be written into the Serial Flash memory array. Using the *Write to Sector* command, data is first shifted into the SRAM from the NXS2 bus. When the command sequence has been completed, the entire 522-bytes is written to the selected sector. See Erase/Write cycle timing (t_{WP}).

The SRAM is fully byte-addressable. Thus, the entire 522-bytes, a single byte, or a sequence of bytes can be read from, or written to the SRAM. This allows the SRAM to be used as a temporary work area for read-modify-write operations prior to a sector write.

The *Transfer Sector to SRAM* command allows the contents of a specified sector of Flash memory to be moved to the SRAM (see figure 5). This can be useful when only a portion of a sector needs to be altered. In this case the sector is first transferred to the SRAM, where modifications are made using the *Write to SRAM* command. Once modifications are completed, a *Transfer SRAM to Sector* command is used to update the sector.

Using the SRAM Independent of Flash Memory

The SRAM can be used independently of Flash memory operations for lookup tables, variable storage, or scratch pad purposes. If the Flash memory needs to be written to while SRAM is being used for a different purpose, the contents can be temporarily stored to a sector and then transferred back again when needed. The SRAM can be especially useful for RAM-limited microcontroller-based systems, eliminating the need for external SRAM and freeing pins for other purposes. It can also make it possible to use small pin-count microcontrollers, since only a few pins are needed for the interface instead of the 20-40 pins required for parallel bus-oriented Flash devices.

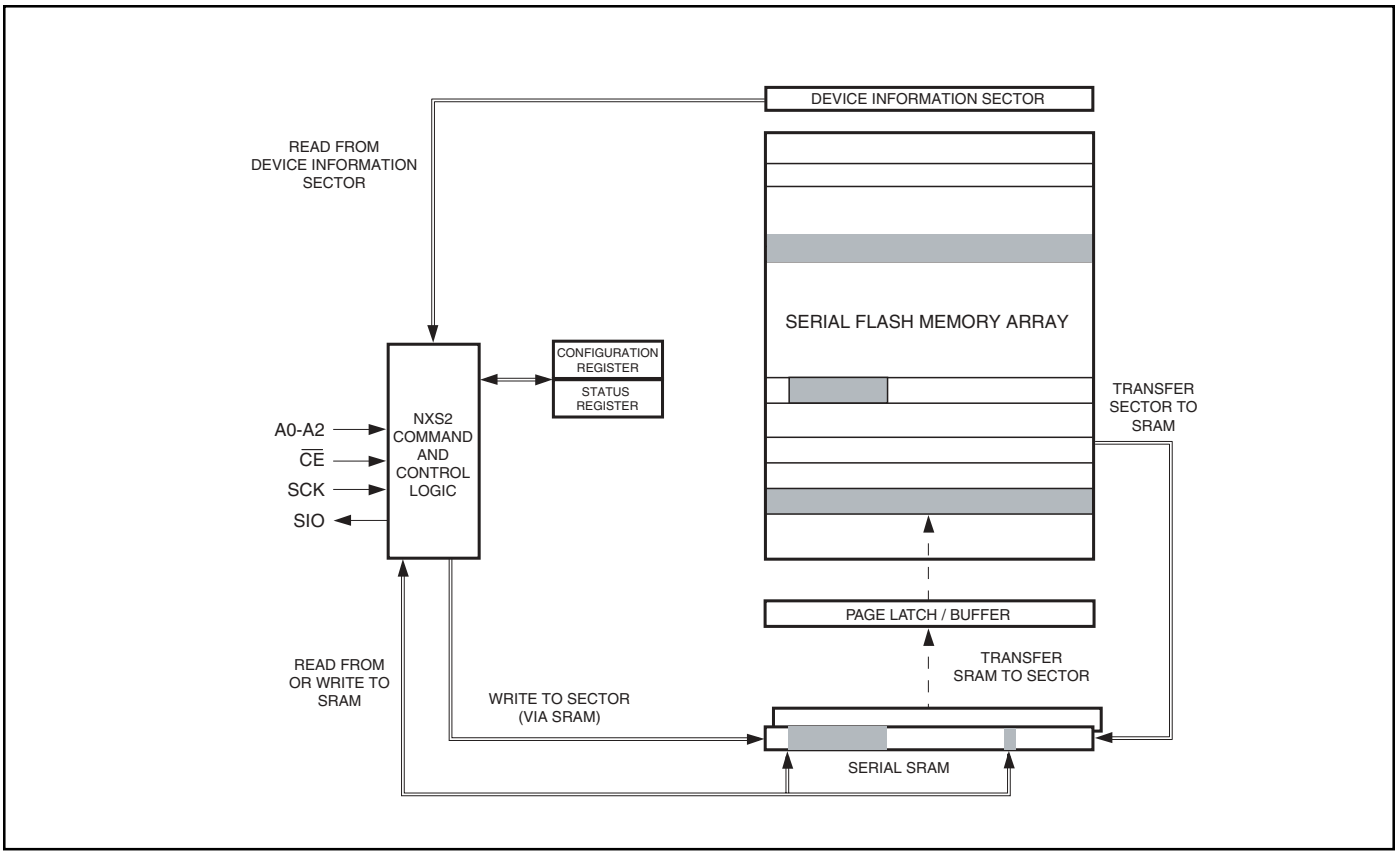


Figure 5. Command Relationships of the NXS2 Interface, Serial Flash Memory Array and SRAM

Write Protection

The NX26F640C provide advanced software and hardware write protection features. Software-controlled write protection of the entire array is handled using the *Write Enable and Write Disable* commands. Hardware write protection is possible using the Write Protect pin ($\overline{WP}$). Write-protecting a portion of Flash memory is accommodated by programming a write protect range in the configuration register.

Configuration Register

The Configuration Register stores the current configuration of the reset timing and write protect range (Figure 6). The configuration register is accessed using the *Write and Read Configuration Register* commands. The non-volatile configuration register will maintain its setting even when power is removed.

To avoid unnecessary programming of the configuration register, and to save time during power-up, the configuration register should be read upon power-up and compared to the intended setting before sending a Write Configuration Register command.

The factory default setting for the configuration register is CF8-CF0 is: 000001001 binary (write protect range = none, reset time is minimum 1.5µs maximum 5µs). When writing to the configuration register reserved bits should be 0. When reading, the settings of reserved bits should be ignored.

NXS2 Reset Timing (RST)
This bit determines the length of time for the timing parameter t_{RESET}. With RST reset (0), the timing of t_{RESET} should be minimum 1.5µs, maximum 5µs. With RST set (1), the timing of t_{RESET} should be minimum 5µs, maximum 10µs.

Write Protect Range and Direction, WR[3:0], WD
The write protect range and direction bits WR[3:0] and WD are located at configuration bits CF[7:4] and CF[3] respectively. The write protect range and direction bits select how the array is protected. They work in conjunction with the $\overline{WP}$ input pin, valid only if $\overline{WP}$ is inactive (high). WR[3:0] can select write protection of all sectors, none of the sectors, or specific sectors grouped in blocks of 64 (~32 KB). The WD bit specifies whether the protected block range starts from the first sector, address 0 (000H), or from the last sector (3FFF). Table 2 lists the write protect sector range for the devices. Once protected, all further writes to sectors within the range will be ignored. The factory default setting is with no write protected sectors, WR=[0,0,0,0] and WD=1.

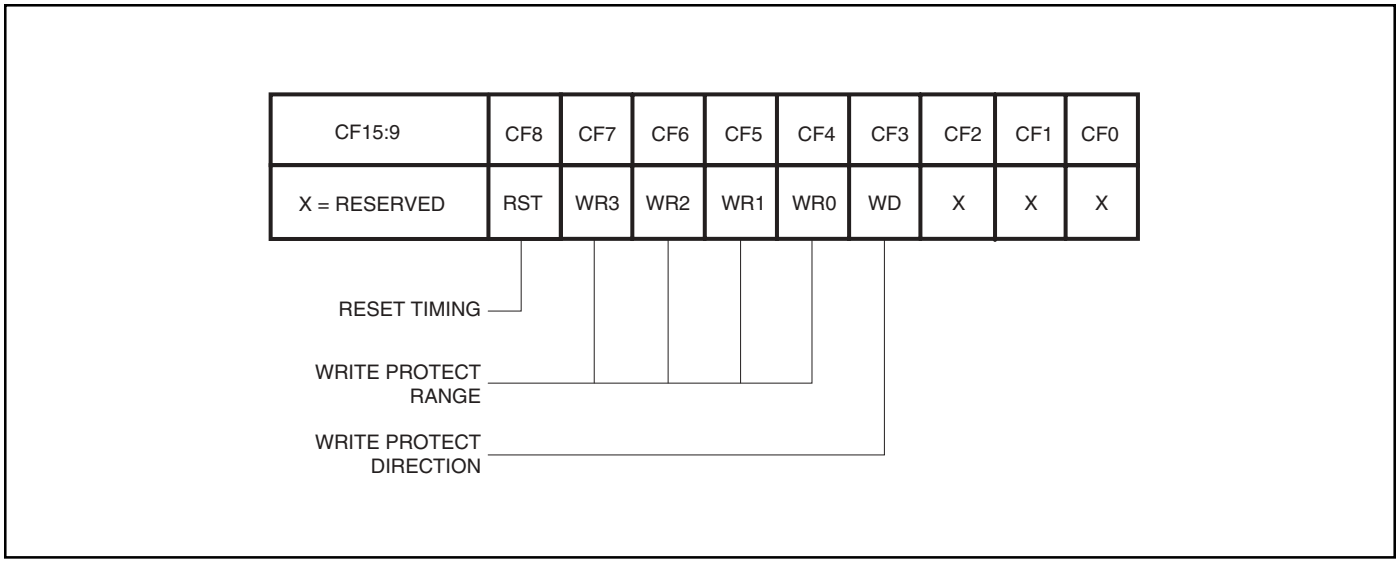


Figure 6. Configuration Register Bit Locations

Table 2. Write Protect Range Sector Selection

Write Protect Range Config. Bits				Write Protected Sectors (Hex)	
WR3	WR2	WR1	WR0	WD=0	WD=1
0	0	0	0	None	None
0	0	0	1	0000-003F	3FC0-3FFF
0	0	1	0	0000-007F	3F80-3FFF
0	0	1	1	0000-00BF	3F40-3FFF
0	1	0	0	0000-00FF	3F00-3FFF
0	1	0	1	0000-013F	3EC0-3FFF
0	1	1	0	0000-017F	3E80-3FFF
0	1	1	1	0000-01BF	3E40-3FFF
1	0	0	0	0000-01FF	3E00-3FFF
1	0	0	1	0000-023F	3DC0-3FFF
1	0	1	0	0000-027F	3D80-3FFF
1	0	1	1	0000-02BF	3D40-3FFF
1	1	0	0	0000-02FF	3D00-3FFF
1	1	0	1	0000-033F	3CC0-3FFF
1	1	1	0	0000-037F	3C80-3FFF
1	1	1	1	ALL	ALL

Status Register Bit Descriptions

The status register provides status of the Flash array's Ready/Busy condition (R/$\overline{B}$), transfers between the SRAM and program buffer (TR0 and TR1), Write-Enable/Disable (WE), Compare Not Equal (CNE), Power Detect (PD) and Data Integrity status (DI0 and DI1). The register can be read using the Read Status Register command (Figure 7).

Ready/Busy Status, BUSY

The BUSY status bit is located at bit ST[15] of the status register. Testing the BUSY bit is one of several ways to check Ready/Busy status of the array. At power-up the BUSY bit is reset to 0.

BUSY=1 The device is busy programming.
BUSY=0 The deivce is ready for further use.

SRAM Transfer, TR0 and TR1

The TR status bits are located at bit ST[13] and ST[14] of the status register. The bits provide status during the *Transfer Sector to SRAM, Transfer SRAM to SRAM,* and *Refresh Sector* commands. An active state 1 indicates the SRAM Array is not available for use. The device will also indicate a BUSY state while the TR bits are active. Upon power up the TR bits reset to 0.

TR=1 Transfer, or Refresh in Process.
TR=0 Transfer, or Refresh not in Process.

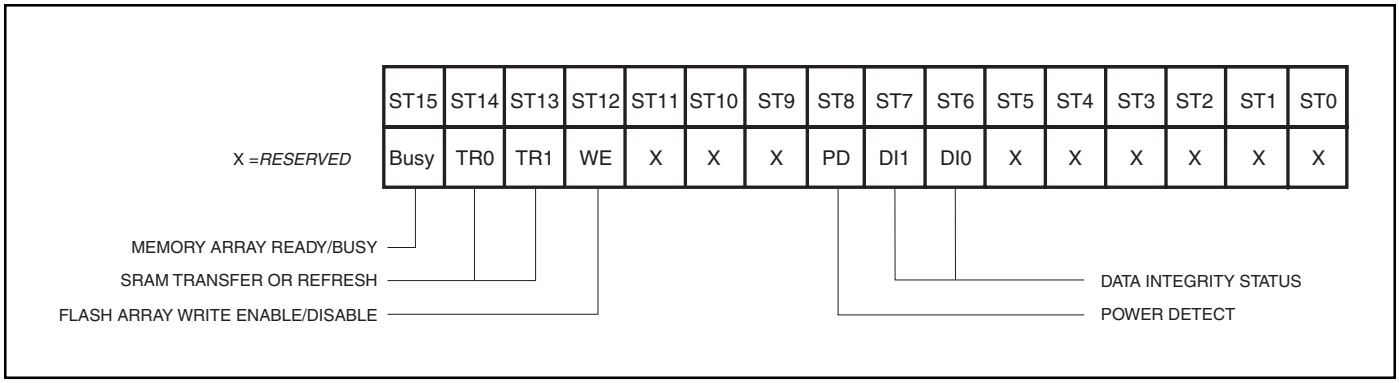


Figure 7. Status Register Bit Locations

Write Enable/Disable, WE

The WE status bit is located at bit ST[12] of the status register. The bit provides write protect status of global *Write Enable and Write Disable* commands. Upon power-up the WE bit resets to 0.

WE=1 Write Enabled, array can be written to.
WE=0 Write Disabled, array can not be written to.

Power Detect, PD

The Power Detect bit ST[8] works in conjunction with the Set Power Detection and Reset Power Detection Commands and is primarily used for removable media applications. The Set Power Detect Command must be issued before the PD bit can be used for power detection.

PD=0 Power has been removed
PD=1 Power has not been removed

Data Intergrity Status (DI1, DI0)

The Data Integrity status bits provide an indication of the data integrity of the last sector that was tranfered to the SRAM. The bits should be checked after every transfer sector to SRAM operation.

DII, DI0 = 00 Sector data valid
DII, DI0 = 01 Sector data valid
DII, DI0 = 10 Reserved
DII, DI0 = 11 Sector data error

If DI1 and DI0 = 00 or 01, data is valid and no action is required. If DI0 and DI1 = 11 a data read error has occurred. Possible cause for a data error might be excessive system noise, improper power supply levels during the read or write operation, or excessive erase/write cycles.

Contact NexFlash applications department for further information regarding handling data error status.

Command Set

The NX26F640C has a powerful command set that is fully controlled through the NXS2 bus. Command relationships are shown in Figure 5 and a list of commands and their associated address, status, clock, and data bytes are shown in the Command Set Table (next page). Flow diagrams for writing to a sector and reading from a sector are shown in Figures 8 and 9. Detailed clock timing of the Write to Sector using SRAM, Transfer Sector to SRAM and Read SRAM command sequences are shown in Figures 10, 11 and 12.

After power up, a device enters an idle state that will maintain until $\overline{CS}$ pin is asserted low. Chip reset is defined as a low to high transition of CS. Thus, to reset the chip at power on, a high to low to high transition is required. A command may start after a high to low transition of CS. When a command is started, CS needs to stay low for the duration of the command and data.

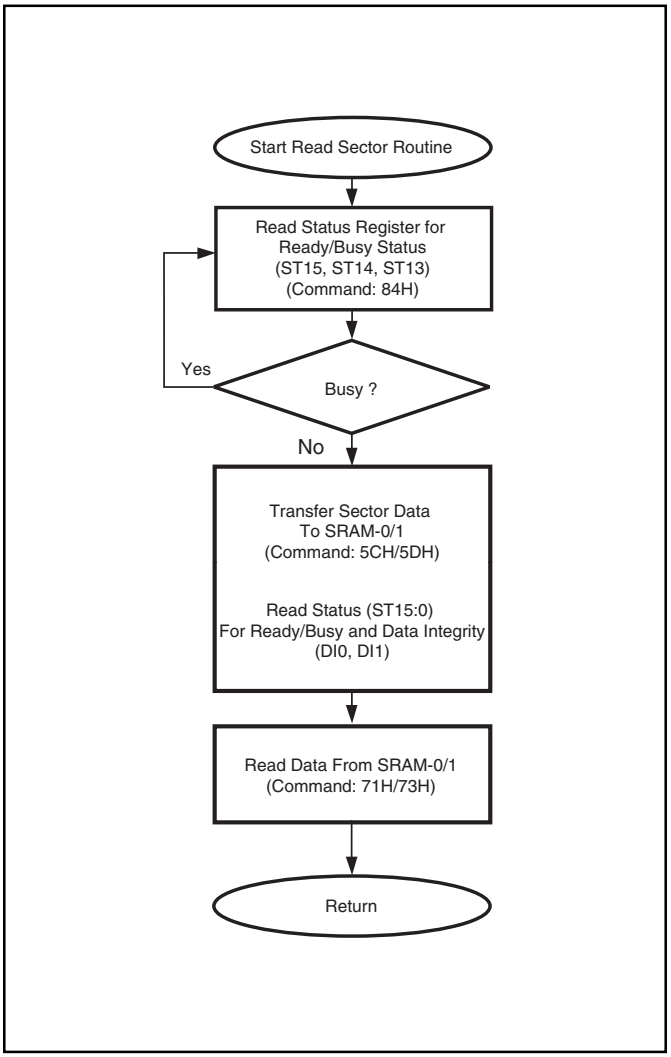


Figure 8. Read data from sector

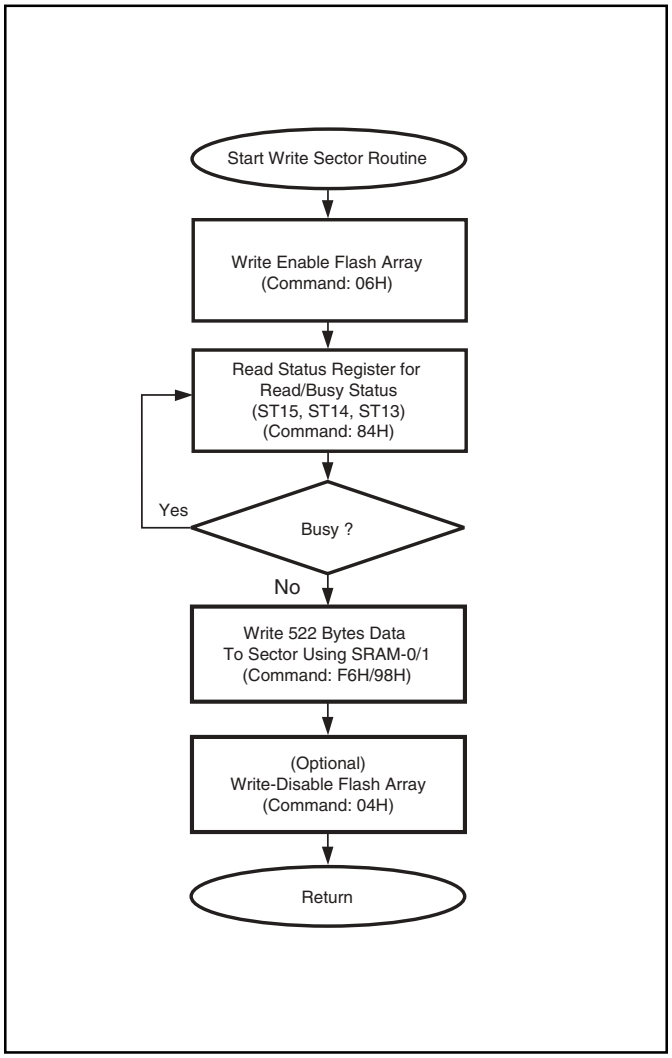


Figure 9. Write data to sector (Erase + Program)

Table 3: Command Set for the NX26F640C Serial Flash Memory [3]

Command Name	Byte 0[5]	Byte 1	Byte 2-3	Byte 4-5 or n-bytes		
Sector and SRAM Read Commands						
Transfer Sector to SRAM-0 [2]	DA7:0	5CH	SA15:0	0000H	0000H	ST15:0 [4]
Transfer Sector to SRAM-1 [2]	DA7:0	5DH	SA15:0	0000H	0000H	ST15:0 [4]
Read SRAM-0 [1]	DA7:0	71H	BA15:0	00H	Read Data	
Read SRAM-1 [1]	DA7:0	73H	BA15:0	00H	Read Data	
Sector and SRAM Write Commands						
Write Enable [1]	DA7:0	06H				
Write Disable [1]	DA7:0	04H				
Write Sector using SRAM-0 [2]	DA7:0	F6H	SA15:0	BA15:0	Write Data+00H	
Write Sector using SRAM-1 [2]	DA7:0	98H	SA15:0	BA15:0	Write Data+00H	
Write to SRAM-0 [1]	DA7:0	72H	BA15:0	Write Data+00H		
Write to SRAM-1 [1]	DA7:0	74H	BA15:0	Write Data+00H		
Transfer and Refresh Commands						
Transfer SRAM-0 to Sector [2]	DA7:0	F6H	SA15:0	0000H		
Transfer SRAM-1 to Sector [2]	DA7:0	98H	SA15:0	0000H		
Transfer SRAM-0 to SRAM-1 [2]	DA7:0	92H	0000H	0000H	0000H	
Transfer SRAM-1 to SRAM-0 [2]	DA7:0	55H	0000H	0000H	0000H	
Refresh Sector using SRAM-0 [2]	DA7:0	58H	SA15:0	0000H	0000H	
Refresh Sector using SRAM-1 [2]	DA7:0	59H	SA15:0	0000H	0000H	
Configuration and Status Commands						
Read Device Information Sector [2]	DA7:0	15H	0000H	BA15:0	0000H	Ready/Busy Read Data
Read Configuration Register [1]	DA7:0	8CH	CF15:0			
Write Configuration Register [1]	DA7:0	8AH	CF15:0	0000H		
Read Status Register [1]	DA7:0	84H	ST15:0			
Clear Power Down Bit [1]	DA7:0	09H				
Set Power Down Bit [1]	DA7:0	03H				

Notes:
1. Command may be used when device is busy
2. Command may not be used when device is busy
3. Additional commands such as Auto Increment and other commands offering compatibility with earlier generation NexFlash devices are available. Contact NexFlash for further information.
4. ST15:0 status repeats every 16 Clocks
5. Device address bits DA2:0 specify the device to be selected per the state of the A0, A1 and A2 pins. Bits DA7:3 Must be 0.

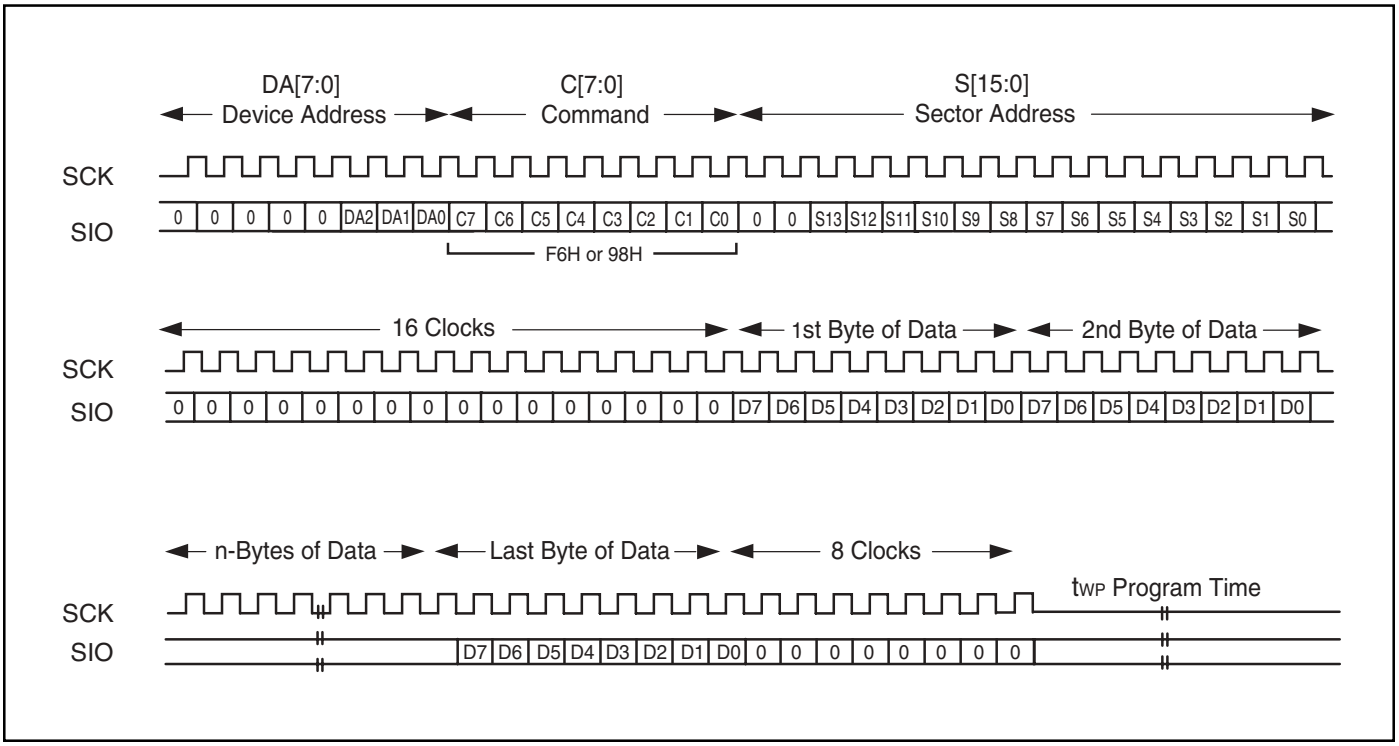


Figure 10. Write to Sector using SRAM Command Sequence

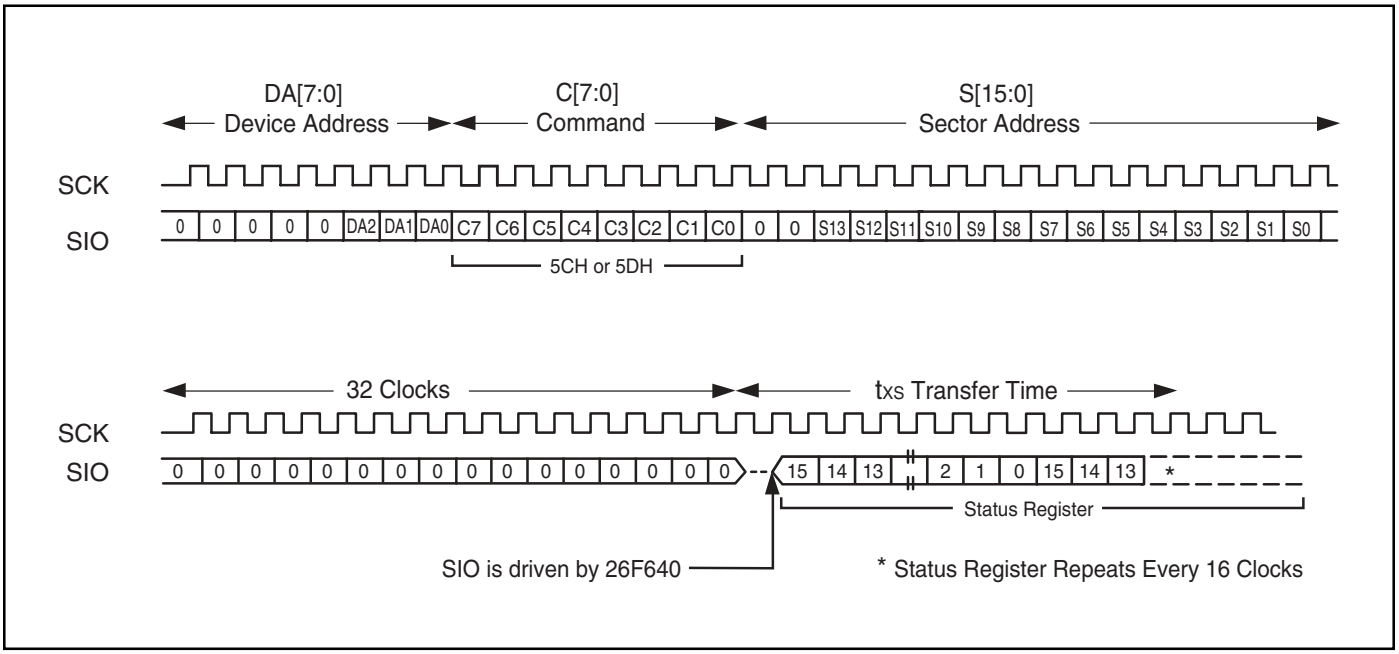


Figure 11. Transfer Sector to SRAM Command Sequence

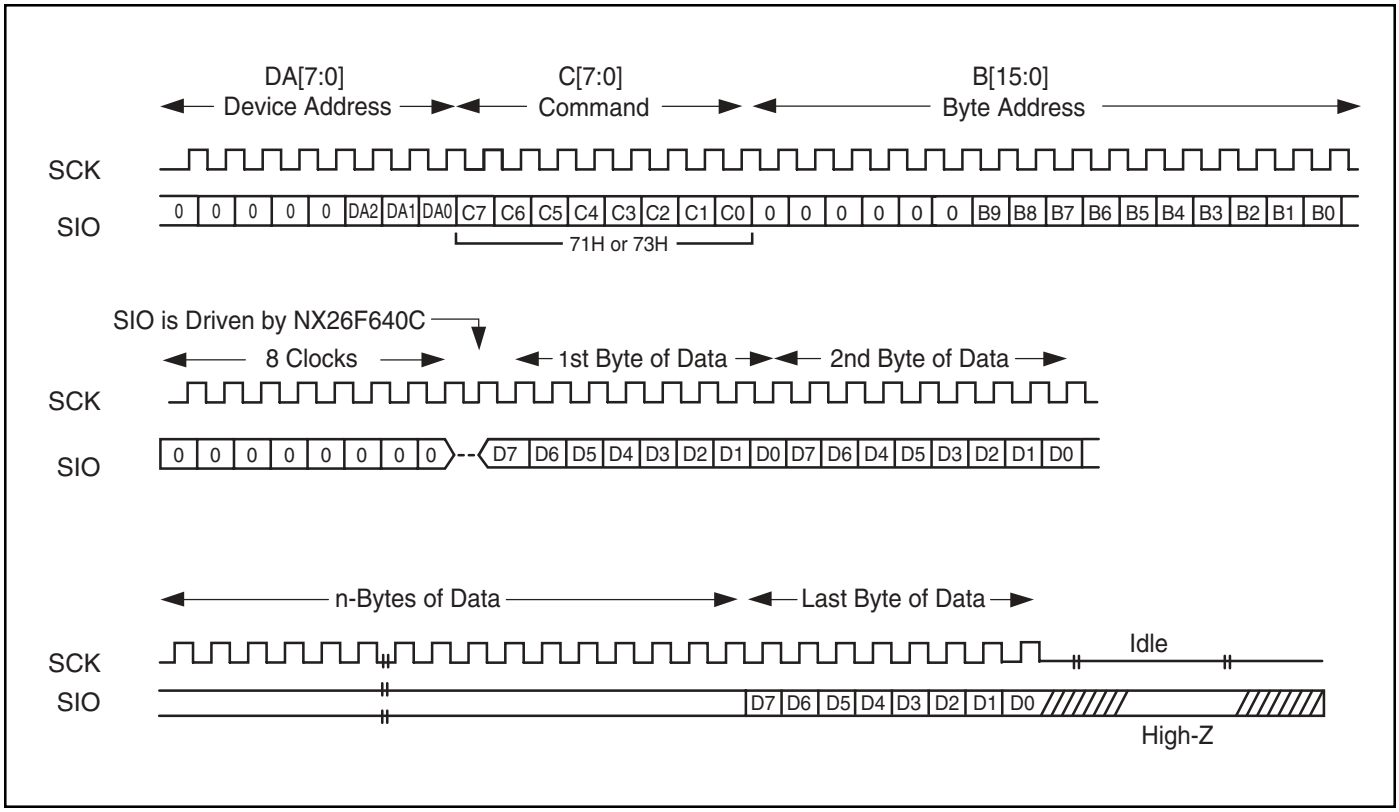


Figure 12. Read from SRAM Command Sequence

SERIAL FLASH SECTOR AND SRAM READ COMMANDS

Transfer Sector to SRAM (5CH and 5DH)

The *Transfer Sector to SRAM* command transfers the contents of a specified 522-byte sector directly to the SRAM. Writing to a sector is accomplished by first bringing $\overline{CS}$ low and shifting in the *Transfer Sector to SRAM* command (53H and 5DH) followed by a 16-bit "sector-address" field. Although the sector-address field is 16-bits, only bits S[13:0] are used. The uppermost sector address bits are not used but must be clocked in (use 0 data). Following the sector address, a 32-bit "0" field is clocked into the device. The transfer operation will start and the Busy and TR bit in the status register will be set. The Status Register bits ST[15:0] are then provided on the SO output every 16 clocks. This feature allows the Busy and TR bit in the status register to be checked without sending a separate Status Register command. When the transfer operation is complete the Busy and TR bits in the status register will be cleared and the Data Integrity bits DI0 and DI1 can be checked to confirm that data is valid.

Read SRAM (71H and 73H)

The *Read SRAM* command (71H and 73H) provides access to the 522-Byte SRAM independent of any Flash memory array operations. The TR bit in the status register should be checked first if *Transfer Sector to SRAM* or

Refresh Sector commands are used. Reading from the SRAM is accomplished by first bringing $\overline{CS}$ low then shifting in the *Read SRAM* command (71H or 73H) followed by its 16-bit "byte-address" field is clocked into the device to designate the starting location within the 522-byte sector. Only B[9:0] of the byte-address field are used; the uppermost bits are not used but must be clocked in (use 0 for data). Only byte-addresses of 0 to 209H (522 bytes) are valid. Following the byte-address field, 8 control clocks are required with data=0. The Serial Data Output (SO) will change from a high-impedance state and begin to drive the output. If SO uses the rising edge of clock (configuration register RCE=1), the output will be driven after the last control clock. If SO uses the falling edge of clock (RCE=0), the output will be driven on the next falling edge of clock. The data field is shifted out with the least significant byte first (i.e., byte-00H, byte-01H, ...). The bit order within each byte is the most significant bit first (i.e.,D7,...D0). The byte-address is internally incremented to the next higher byte address as the clock continues.

SERIAL FLASH SECTOR AND SRAM WRITE COMMANDS

Write Enable (06H)

Upon power-up, the Flash memory array is write- protected until the *Write Enable* command (06H) has been issued. The $\overline{WP}$ pin must be inactive while writing the command for the write enable to be accepted. The status of the device's write protect state can be read in the status register. The *Write Enable* command sequence is completed by asserting $\overline{CS}$ high after eight additional clocks.

Write Disable (04H)

The *Write Disable* command (04H) protects the Flash memory array from being programmed. Once issued, further *Write to Sector* or *Transfer SRAM to Sector* commands will be ignored. The status of the write protect state can be read in the status register. The *Write Disable* command sequence is completed by asserting $\overline{CS}$ high after eight additional clocks.

Write to Sector Using SRAM (F6H or 98H)

Before writing to a sector in the Flash memory array, all hardware and software write protection must be in an enabled state. This means that the $\overline{WP}$ pin must be in a high state, a *Write Enable* command must have previously been issued, and the sector location that is to be written to must be outside the write protect range set in the configuration register. Additionally, the Ready/Busy status should be checked to confirm that the memory array is available to be written to, refer to figures 8 and 12 for block diagram.

Writing to a sector is accomplished by first bringing $\overline{CS}$ low and shifting in the *Write to Sector* Using SRAM command (F6H or 98H) followed by a 16-bit "sector-address" field. Although the sector-address field is 16-bits, only bits S[13:0] are used. The uppermost sector address bits are not used but must be clocked in (use 0 data). Following the sector address, a 16-bit "byte-address" field is clocked into the device to designate the starting location within the 522-byte sector. Only bits B[9:0] of the byte-address field are used and only values of 0-209H (522 bytes) are valid.

After the byte-address has been loaded, data is shifted into the 522-byte SRAM, which serves as a temporary storage buffer. Existing data in the SRAM will be written over. The byte order of the data shifted into the SRAM is least significant byte first (i.e., byte-00H, byte-01H,...). The bit order within each byte is most significant bit first (i.e., D7,...D0). The byte-address is automatically incremented to the next higher byte address as the clock continues. When the last byte address to be written is reached, the command can be completed with an additional eight control clocks (with data=0) followed by asserting $\overline{CS}$ high.

After the $\overline{CS}$ pin is brought high, the data in the SRAM is transferred to the specified sector in memory array. See t_{WP} timing specifications. During this time the array and SRAM will be "busy" and will ignore further array-related commands until complete. All Ready/Busy status indicators will indicate a busy status.

Write to SRAM Command (72H and 74H)

The *Write to SRAM* command (72H and 74H) provides access to the 522-Byte SRAM independently of any Flash memory array operation. When $\overline{CS}$ is asserted high to complete the command, the contents of the SRAM will be maintained until overwritten through another command or the power is removed. Using the *Write to SRAM* command, data can be loaded in preparation of writing to a sector in memory and then transferred to a selected sector using the *Transfer SRAM to Sector* command. The TR bit in the status register should be checked first if *Transfer Sector to SRAM* or *Compare Sector to SRAM* commands are used.

TRANSFER AND REFRESH COMMANDS

Transfer SRAM to Sector (F6H and 98H)

The *Transfer SRAM to Sector* command (F6H and 98H) will write the existing contents of the SRAM to the specified sector in memory. The command sequence is identical to that of the *Write to Sector Using SRAM* command except that immediately after the sector address field S[15:0] and 16 control clocks, the $\overline{CS}$ pin is asserted high. This automatically transfers the 522-bytes of SRAM data to the specified sector in the memory array. During this time, the array and the SRAM will be busy.

Refresh Sector Using SRAM (58H and 59H)

The *Refresh Sector Using SRAM* command (58H and 59H) will automatically transfer the contents of the specified sector into the SRAM and then re-write the data to the same sector. The purpose of this command is to enhance data integrity and cycle endurance. Contact NexFlash Marketing for updated information regarding usage of the Refresh Command. During this command the array and the SRAM will be busy.

CONFIGURATION AND STATUS COMMANDS

Read Device Information Sector (15H)

The *Read Device Information* command provides access to a read-only sector that can be used to electronically identify the *NexFlash* Serial Flash device being interfaced to. Information available includes: part number, density, voltage, temperature range, package type, and any special options. Contact *NexFlash* for more detailed information on the Device Information Sector format.

Read Configuration Register (8CH)

The *Read Configuration Register* command provides access to the configuration register, which stores the current configuration of the reset timing and write protect range (see figure 5). A 16-bit Configuration Data field CF[15:0] provides the contents of the Configuration Register.

Write Configuration Register (8AH)

The *Write Configuration Register* command provides access to the configuration register which stores the current configuration of the reset timing and write protect range. The configuration register is non-volatile. Once set using the *Write Configuration Register* command, the contents will maintain even when power is removed. Because the register's state is stored in non-volatile memory, there is a finite endurance limit to the number of times it can be written to. To limit the number of writes, it is recommended that before writing to the configuration register it should first be read by using the *Read Configuration Register* command. If no change is required, the *Write Configuration Register* command can be skipped. This process will help extend the endurance of the configuration register bits and eliminate additional programming "busy" time.

The *Write Configuration Register* command sequence starts with the command byte (8AH) followed by a 16-bit field that specifies configuration register bit settings. Although the field is 16-bits long, only bits CF[7:0] are used. All other upper bits are reserved and must be clocked using 0 for data. After an additional 16 control clocks using 0 for data, the command can be completed by asserting CS high. The device will become busy for a short time (t_{WP}) while the non-volatile memory cells of the configuration register are programmed.

Read Status Register (84H)

The *Read Status Register* command provides access to the status register and its status flags for Ready/Busy (R/B), SRAM buffer transfer operations (TR0 and TR1), Write Enable/Disable (WE), Power Detect and Data Integrity bits (Figure 6). An 16-bit Status field ST[16:0] provides the contents of the Status Register.

Clear Power Detection Bit (09H)

The *Reset Power Detection Bit* command (09H) can be used to force the Power Detect Status bit in the status register to a 0 state. (see Set Power Detection Bit command (03H).

Set Power Detection Bit (03H)

The *Set Power Detection Bit* command (03H) can be used to detect if power has been removed from the device. The command works in conjunction with the Power Detect (PD) status bit. Upon power up the PD bit is cleared to 0. The PD bit can be set to a 1 using the *Set Power Detection Bit* command. Once set, if a power down condition occurs (Vcc voltage < 2V) the PD bit will reset to 0. This function is especially useful for applications using *NexFlash* Serial Flash Modules or other removable media.

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameters	Conditions	Range	Unit
Vcc	Supply Voltage		0 to +4.0	V
V_{IN}, V_{OUT}	Voltage Applied to Any Pin	Relative to Ground	–0.5 to Vcc + 0.5	V
T_{STG}	Storage Temperature		–65 to +150	˚C
T_{LEAD}	Lead Temperature	Soldering 10 Seconds	+300	˚C

Note:
1. This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure beyond absolute maximum ratings (listed above) may cause permanent damage.

OPERATING RANGES

Symbol	Parameter	Conditions	Min	Max	Unit
Vcc	Supply Voltage	3.0V	2.7	3.6	V
T_A	Ambient Temperature, Operating	Commercial	0	70	°C
		Industrial	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS (Preliminary)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage		–0.4	—	Vcc 0.2	V
V_{IH}	Input High Voltage		Vcc –0.7	—	Vcc +0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA, V_{CC} = 2.7V	—	—	0.45	V
V_{OH}	Output High Voltage	I_{OH} = –100 µA, V_{CC} = 2.7V	Vcc –0.85	—	—	V
V_{OLC}	Output Low Voltage CMOS	V_{CC} = 2.7V, I_{OL} = 10 µA	—	—	0.15	V
V_{OHC}	Output High Voltage CMOS	V_{CC} = 2.7V, I_{OH} = –10 µA	V_{CC} –0.3	—	—	V
I_{IL}	Input Leakage	0 < V_{IN} < Vcc	–10	—	+10	µA
I_{OL}	I/O Leakage	0 < V_{IN} < Vcc	–10	—	+10	µA
I_{CC} (active)	Active Power Supply Current	SCK @ 8 MHz, V_{CC} = 3V Erase/Write	—	2.5	5	mA
I_{CC} (active)	Active Power Supply Current	SCK @ 8 MHz, V_{CC} = 3V Read	—	5	10	mA
I_{CCSB} (standby)	Standby Vcc Supply Current	CS = V_{CC}, V_{IN} = Vcc or 0 Standby	—	<1	10	µA
C_{IN}	Input Capacitance (1)	T_A = 25°C, V_{CC} = 3V Frequency = 1 MHz	—	—	10	pF
C_{OUT}	Output Capacitance (1)	T_A = 25°C, V_{CC} = 3V Frequency = 1 MHz	—	—	10	pF

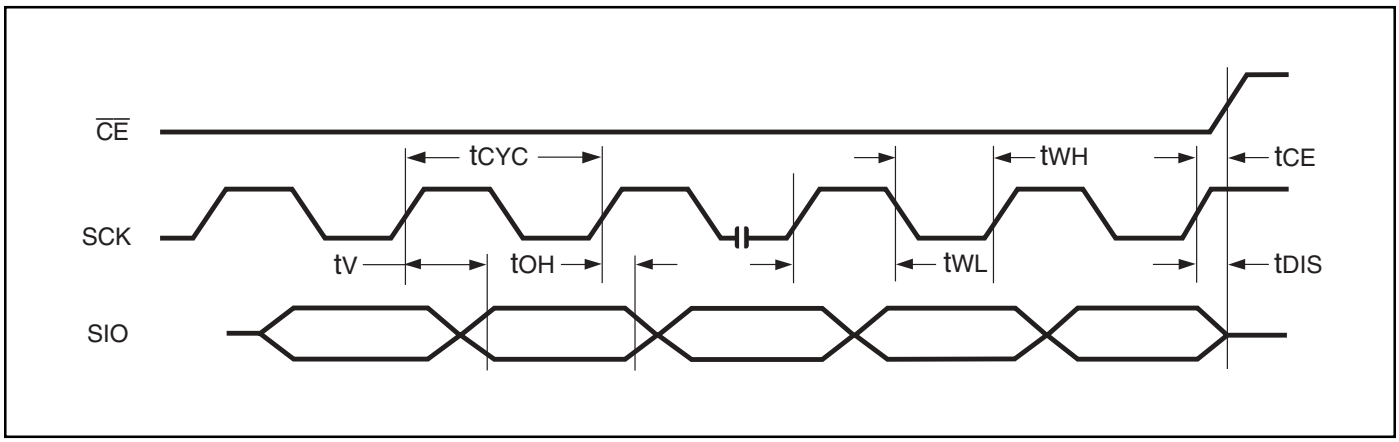
Note:
1. Tested on a sample basis or specified through design or characterization data.

AC ELECTRICAL CHARACTERISTICS (PRELIMINARY)

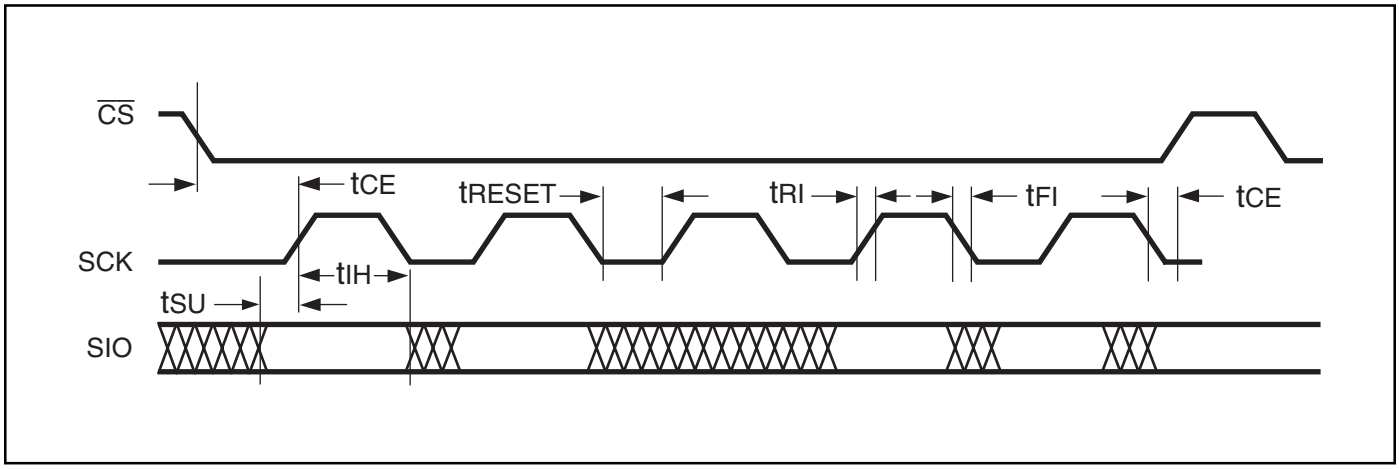
		16 MHz			
Symbol	**Description**	**Min**	**Typ**	**Max**	**Unit**
t_{CYC}	SCK Serial Clock Period	77	—	—	ns
t_{WH} t_{WL}	SCK Serial Clock High or Low Time	$t_{CYC}/2$	—	—	ns
t_{RI} t_{FI}	SCK Serial Clock Rise or Fall Time (1)	—	—	5	ns
t_{SU}	Data Input Setup Time to SCK	20	—	—	ns
t_{IH}	Data Input Hold Time from SCK	0	—	—	ns
t_{WP}	Erase/Write Program Time (3) *(see Write to Sector Command)*	—	10	15	ms
t_{XS}	Transfer Sector *(see Transfer Command)*	100	150	520	µs
t_{CE}	$\overline{CE}$ Select and Deselect Time	160	—	—	ns
t_{RB}	READY / BUSY Valid Time	160	—	—	ns
t_{DIS}	Data Output Disable Time	—	—	160	ns
t_{OH}	Data Output Hold Time After SCK	0	—	—	ns
t_{RESET}	SCK Low Duration for Valid Reset				
	Configuration Register CF8=0 (default)	1.5	—	5	µs
	Configuration Register CF8=1	5	—	10	µs

Notes:
1. Test points are 10% and 90% points for rise/fall times. All others timings are measured at 50% point.
2. With 30 pF (16 MHz) load SO to GND.
3. Maximum program time for 99% of sectors, <1% may require 4x this value.

SERIAL OUTPUT TIMING

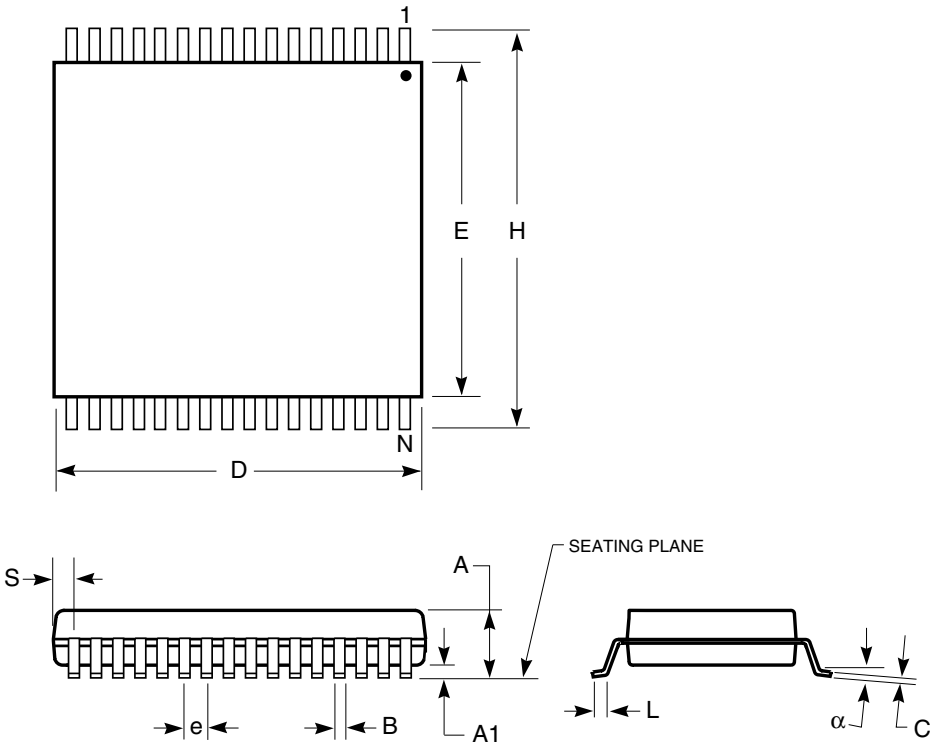


SERIAL INPUT TIMING



Plastic TSOP - 32-pins

Package Code: T (Type I)



Plastic TSOP (T—Type I)				
	Millimeters		Inches	
Symbol	Min	Max	Min	Max
Ref. Std.				
No. Leads		32		
A	–	1.20	–	0.047
A1	0.05	0.15	0.002	0.005
B	0.17	0.27	0.007	0.009
C	0.10	0.21	0.004	0.008
D	7.90	8.10	0.308	0.316
E	18.30	18.50	0.714	0.722
H	19.80	20.20	0.772	0.788
e	0.50 BSC		0.020 BSC	
L	0.50	0.70	0.016	0.024
a	0°	5°	0°	5°

Notes:
1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E do not include mold flash protrusions and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

PRELIMINARY DESIGNATION

The “Preliminary” designation on an *NexFlash* data sheet indicates that the product is not fully characterized. The specifications are subject to change and are not guaranteed. *NexFlash* or an authorized sales representative should be consulted for current information before using this product.

IMPORTANT NOTICE

NexFlash reserves the right to make changes to the products contained in this publication in order to improve design, performance or reliability. *NexFlash* assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Charts and schedules contained herein reflect representative operating parameters, and may vary depending upon a user’s specific application. While the information in this publication has been carefully checked, *NexFlash* shall not be liable for any damages arising as a result of any error or omission.

LIFE SUPPORT POLICY

NexFlash does not recommend the use of any of it's products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure in the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless *NexFlash* receives written assurances, to it’s satisfaction, that:

(a) the risk of injury or damage has been minimized;

(b) the user assumes all such risks; and

(c) potential liability of *NexFlash* is adequately protected under the circumstances.

Trademarks:

NexFlash is a trademark of *NexFlash Technologies, Inc.* All other marks are the property of their respective owner.

ORDERING INFORMATION

Size	Order Part No.	Package
64M-bit	NX26F640C-3T	NXS2, 32-pin, TSOP (Type I) 3V
64M-bit	NX26F640C-3T-R	NX26F640-3T with Restricted Sectors (max 64)

NexFlash® Technologies, Inc.

2711 North First Street • San Jose, CA 95134

Ph: 408-907-3600 • Fx: 408-907-3601 • sales@nexflash.com

www.nexflash.com