

N-channel 30 V, 2.7 mΩ typ., 150 A, STripFET™ H6 Power MOSFET in a TO-220 package

Datasheet – production data

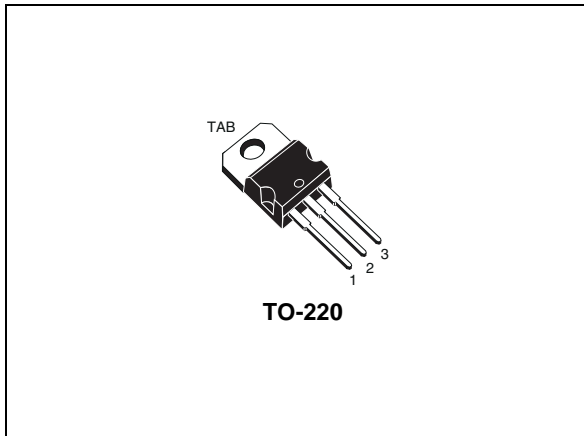
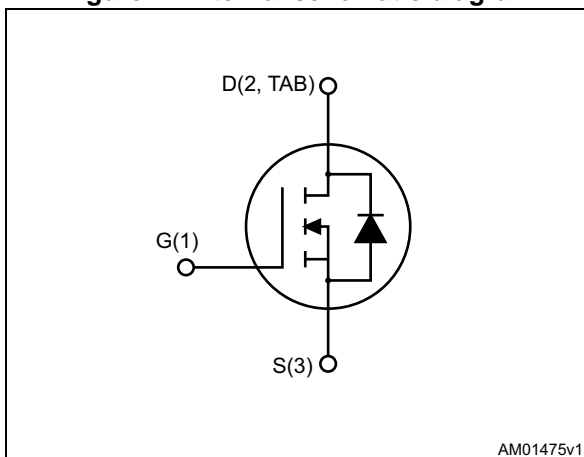


Figure 1. Internal schematic diagram



Features

| Order code | V _{DS} | R _{DS(on)} max. | I _D |
|------------|-----------------|--------------------------|----------------|
| STP105N3LL | 30 V | 3.5 mΩ | 150 A |

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the STripFET™ H6 technology, with a new trench gate structure. The resulting Power MOSFET exhibits very low R_{DS(on)} in all packages.

Table 1. Device summary

| Order code | Marking | Packages | Packaging |
|------------|----------|----------|-----------|
| STP105N3LL | P105N3LL | TO-220 | Tube |

Contents

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1 Electrical ratings

Table 2. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|----------------|--|------------|------|
| V_{DS} | Drain-source voltage | 30 | V |
| V_{GS} | Gate-source voltage | ± 20 | V |
| I_D | Continuous drain current at $T_C = 25\text{ °C}$ (silicon limited) | 150 | A |
| I_D | Continuous drain current at $T_C = 100\text{ °C}$ (silicon limited) | 105 | A |
| I_D | Continuous drain current at $T_C = 25\text{ °C}$ (package limited) | 80 | A |
| $I_{DM}^{(1)}$ | Pulsed drain current | 320 | A |
| P_{TOT} | Total dissipation at $T_C = 25\text{ °C}$ | 140 | W |
| | Derating factor | 0.9 | W/°C |
| $E_{AS}^{(2)}$ | Single pulse avalanche energy | 150 | mJ |
| T_{stg} | Storage temperature | -55 to 175 | °C |
| T_j | Max. operating junction temperature | 175 | °C |

1. Pulse width limited by safe operating area

2. Starting $T_j = 25\text{ °C}$, $I_{AV} = 40\text{ A}$

Table 3. Thermal data

| Symbol | Parameter | Value | Unit |
|----------------|---|-------|------|
| $R_{thj-case}$ | Thermal resistance junction-case max | 1.1 | °C/W |
| $R_{thj-amb}$ | Thermal resistance junction-ambient max | 62.5 | °C/W |

2 Electrical characteristics

($T_{CASE} = 25\text{ °C}$ unless otherwise specified).

Table 4. Static

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|--|--|------|------|-----------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown Voltage | $I_D = 250\ \mu\text{A}$, $V_{GS} = 0$ | 30 | | | V |
| I_{DSS} | Zero gate voltage drain current ($V_{GS} = 0$) | $V_{DS} = 30\text{ V}$ | | | 1 | μA |
| | | $V_{DS} = 30\text{ V}$, $T_C = 125\text{ °C}$ | | | 10 | μA |
| I_{GSS} | Gate body leakage current ($V_{DS} = 0$) | $V_{GS} = \pm 20\text{ V}$ | | | ± 100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{A}$ | 1 | | 2.5 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS} = 10\text{ V}$, $I_D = 40\text{ A}$ | | 2.7 | 3.5 | m Ω |
| | | $V_{GS} = 4.5\text{ V}$, $I_D = 40\text{ A}$ | | 3.5 | 4.5 | m Ω |

Table 5. Dynamic

| Symbol | Parameter | Test conditions | Min | Typ. | Max. | Unit |
|------------|------------------------------|---|-----|------|------|----------|
| C_{iss} | Input capacitance | $V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$ | - | 3500 | - | pF |
| C_{oss} | Output capacitance | | - | 400 | - | pF |
| C_{riss} | Reverse transfer capacitance | | - | 380 | - | pF |
| Q_g | Total gate charge | $V_{DD} = 15\text{ V}$, $I_D = 80\text{ A}$ | - | 42 | - | nC |
| Q_{gs} | Gate-source charge | $V_{GS} = 4.5\text{ V}$ | - | 9 | - | nC |
| Q_{gd} | Gate-drain charge | <i>Figure 14</i> | - | 18 | - | nC |
| R_g | Gate input resistance | $f = 1\text{ MHz}$, gate DC Bias = 0, test signal level = 20 mV, $I_D = 0$ | - | 1 | - | Ω |

Table 6. Switching on/off (inductive load)

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------|---------------------|---|------|------|------|------|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 15\text{ V}$, $I_D = 40\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 5\text{ V}$ <i>Figure 13</i> | - | 19 | - | ns |
| t_r | Rise time | | - | 91 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 24.5 | - | ns |
| t_f | Fall time | | - | 23.4 | - | ns |

Table 7. Source drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|---|------|------|------|------|
| I_{SD} | Source-drain current | | - | | 80 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | - | | 320 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $I_{SD} = 40\text{ A}$, $V_{GS} = 0$ | - | | 1.1 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 80\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 24\text{ V}$ Figure 15 | - | 28.6 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 22.8 | | nC |
| I_{RRM} | Reverse recovery current | | - | 1.6 | | A |

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

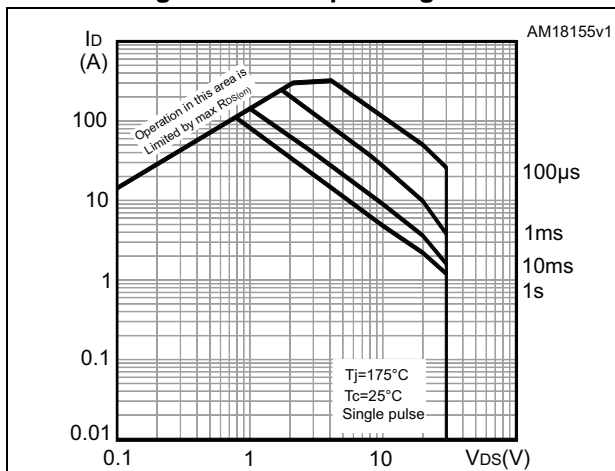


Figure 3. Thermal impedance

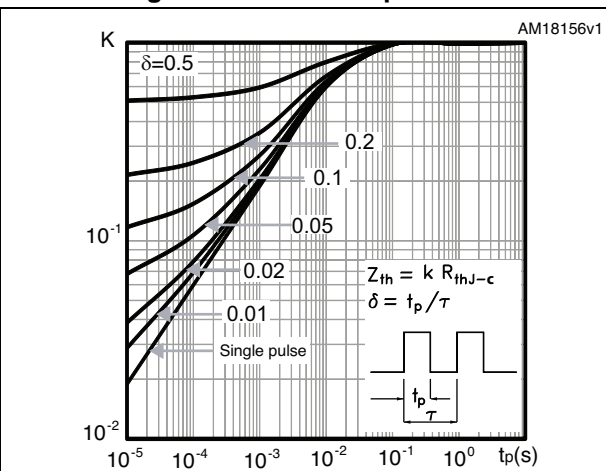


Figure 4. Output characteristics

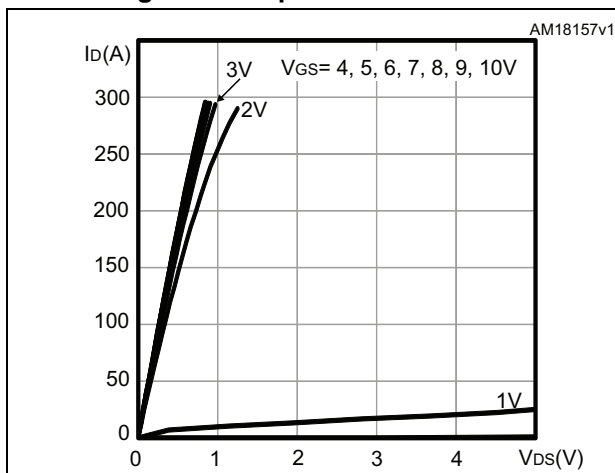


Figure 5. Transfer characteristics

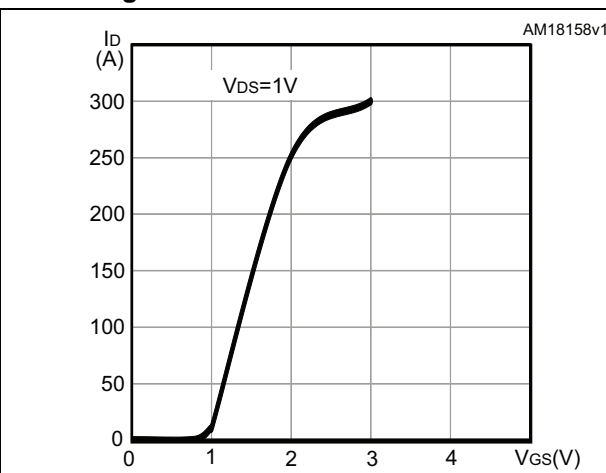


Figure 6. Gate charge vs gate-source voltage

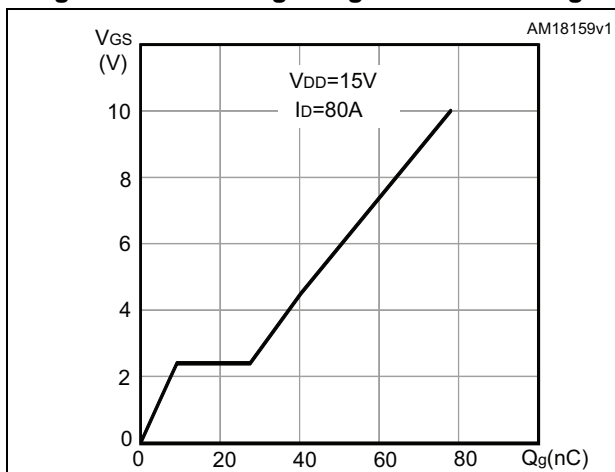


Figure 7. Static drain-source on-resistance

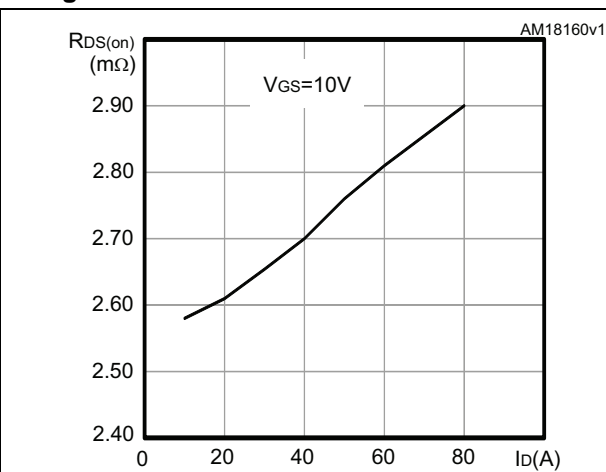


Figure 8. Capacitance variations

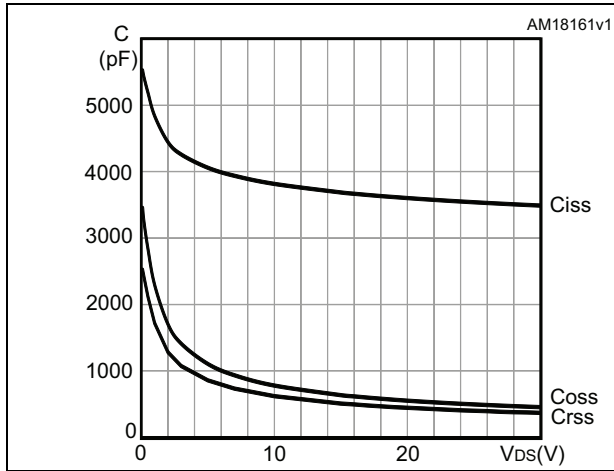


Figure 9. Normalized gate threshold voltage vs temperature

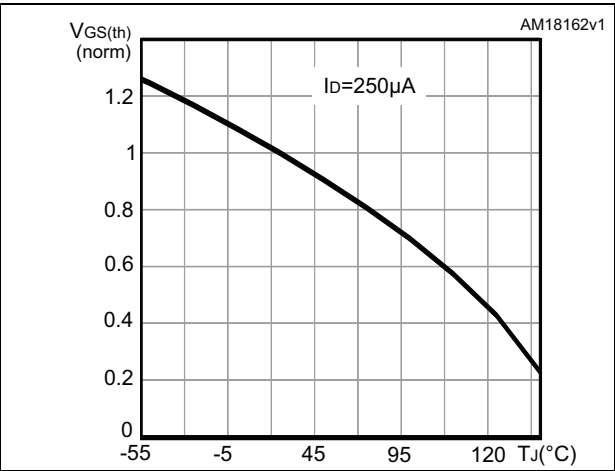


Figure 10. Normalized on-resistance vs temperature

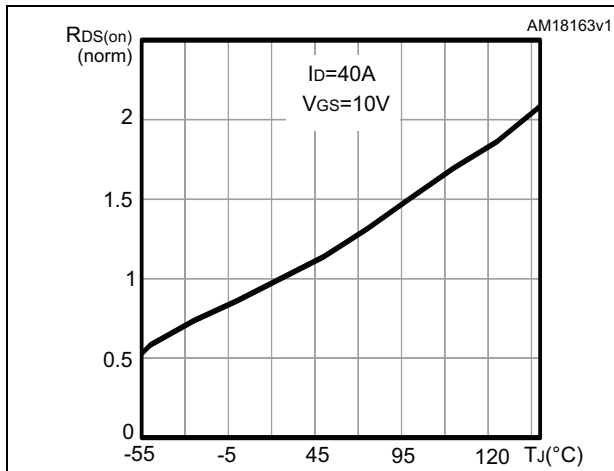


Figure 11. Normalized V(BR)DSS vs temperature

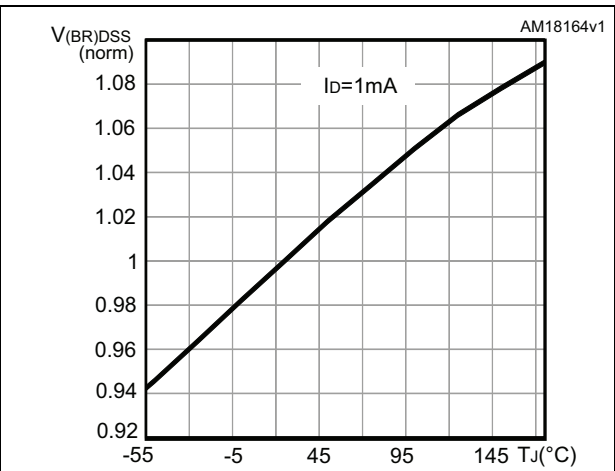
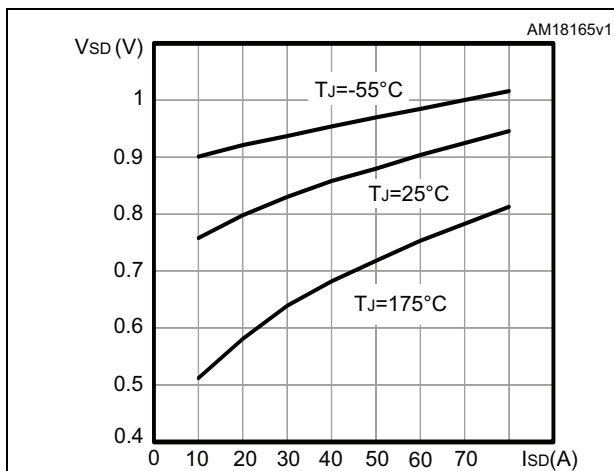


Figure 12. Source-drain diode forward characteristics



3 Test circuits

Figure 13. Switching times test circuit for resistive load



Figure 14. Gate charge test circuit

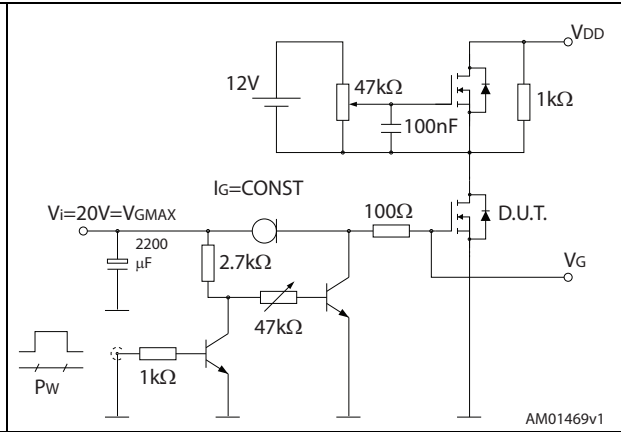


Figure 15. Test circuit for inductive load switching and diode recovery times



Figure 16. Unclamped inductive load test circuit



Figure 17. Unclamped inductive waveform



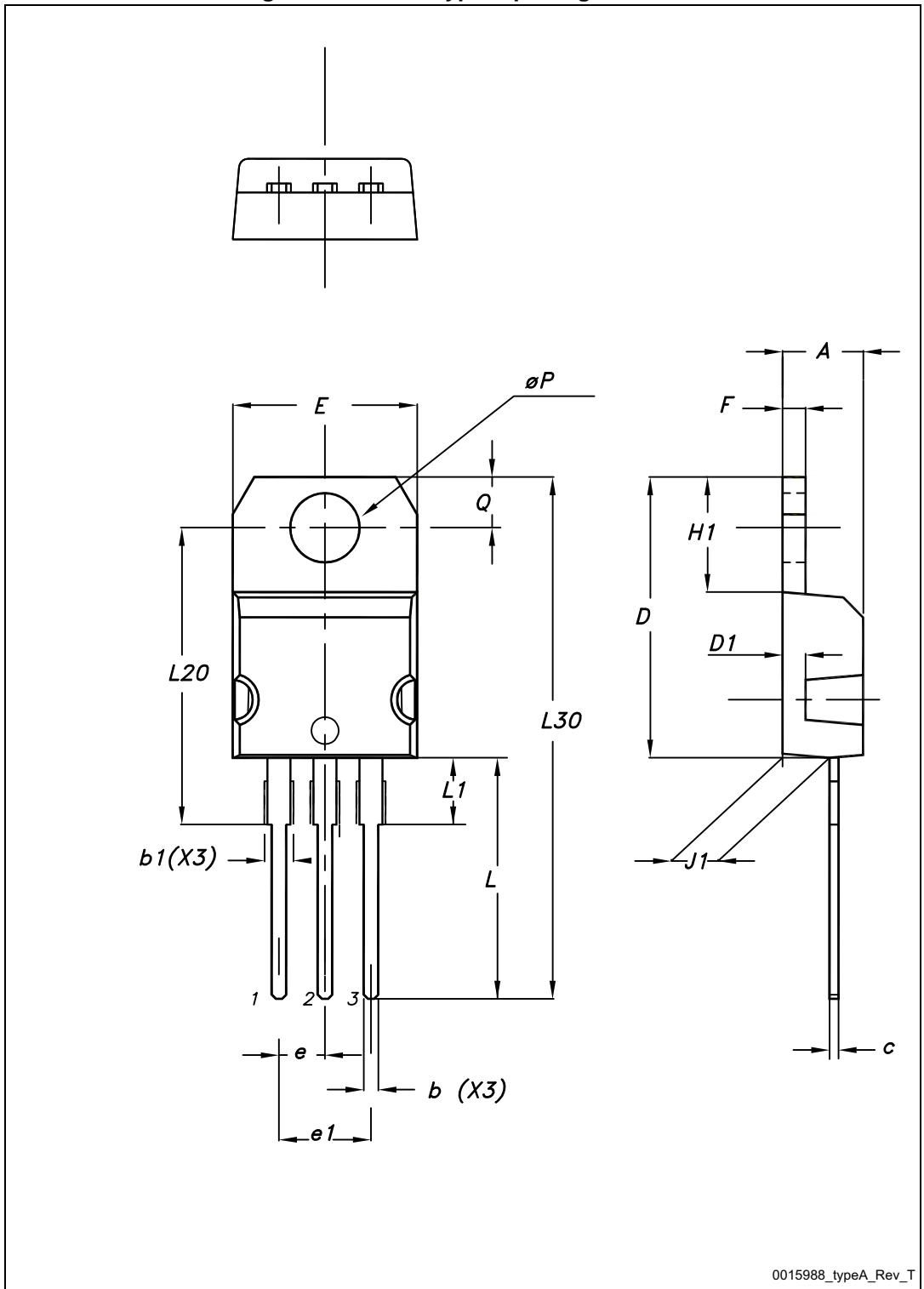
Figure 18. Switching time waveform



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Figure 19. TO-220 type A package outline



0015988_typeA_Rev_T

Table 8. TO-220 type A package mechanical data

| Dim. | mm | | |
|------|-------|-------|-------|
| | Min. | Typ. | Max. |
| A | 4.40 | | 4.60 |
| b | 0.61 | | 0.88 |
| b1 | 1.14 | | 1.70 |
| c | 0.48 | | 0.70 |
| D | 15.25 | | 15.75 |
| D1 | | 1.27 | |
| E | 10 | | 10.40 |
| e | 2.40 | | 2.70 |
| e1 | 4.95 | | 5.15 |
| F | 1.23 | | 1.32 |
| H1 | 6.20 | | 6.60 |
| J1 | 2.40 | | 2.72 |
| L | 13 | | 14 |
| L1 | 3.50 | | 3.93 |
| L20 | | 16.40 | |
| L30 | | 28.90 | |
| ØP | 3.75 | | 3.85 |
| Q | 2.65 | | 2.95 |

5 Revision history

Table 9. Document revision history

| Date | Revision | Changes |
|-------------|----------|--|
| 13-Dec-2012 | 1 | First release. |
| 03-Apr-2014 | 2 | – Added: Section 2.1: Electrical characteristics (curves) – Minor text changes |
| 06-Jul-2015 | 3 | – Updated Table 1: Device summary . – Updated title, features and description in cover page. – Minor text changes. |

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