

# $\mu$ PA2461T1Q

R07DS0186EJ0100

Rev.1.00

Dec 06, 2010

## MOS FIELD EFFECT TRANSISTOR

### Description

The  $\mu$ PA2461T1Q is a switching device, which can be driven directly by a 2.5 V power source.

The  $\mu$ PA2461T1Q features a low on-state resistance and excellent switching characteristics, and is suitable for applications such as power switch of portable machine and so on.

### Features

- 2.5 V drive available
- Low on-state resistance
  - $R_{DS(on)1} = 21.5 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 3.0 \text{ A)}$
  - $R_{DS(on)2} = 22.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.0 \text{ V, } I_D = 3.0 \text{ A)}$
  - $R_{DS(on)3} = 25.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 3.1 \text{ V, } I_D = 3.0 \text{ A)}$
  - $R_{DS(on)4} = 32.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 2.5 \text{ V, } I_D = 3.0 \text{ A)}$
- Built-in G-S protection diode against ESD

### Ordering Information

Part No.	LEAD PLATING	PACKING	Package
$\mu$ PA2461T1Q-E1-AX *1	Ni/Pd/Au	8 mm embossed taping 3000 p/reel	8-pin HUSON (2720)

Note: \*1. Pb-free (This product does not contain Pb in the external electrode and other parts.)

### Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ )

Item	Symbol	N-CHANNEL	Unit
Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ )	$V_{DSS}$	30	V
Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )	$V_{GSS}$	$\pm 12$	V
Drain Current (DC) *1	$I_{D(DC)}$	$\pm 6.5$	A
Drain Current (pulse) *2	$I_{D(pulse)}$	$\pm 50$	A
Total Power Dissipation (2 unit) *1	$P_{T1}$	1.0	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

Notes: \*1. Mounted on a glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mm

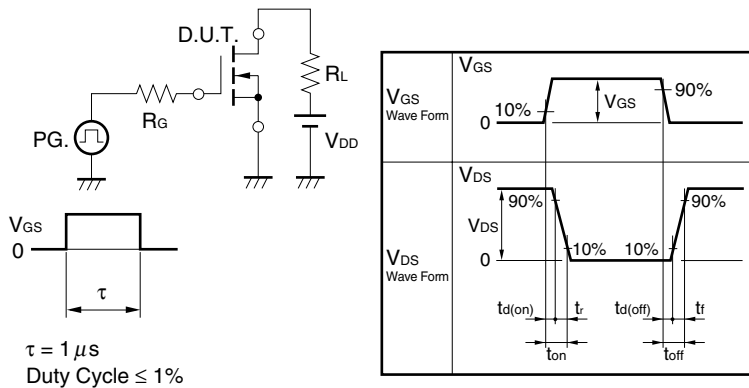
\*2.  $PW \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1\%$

**Electrical Characteristics (T<sub>A</sub> = 25°C)**

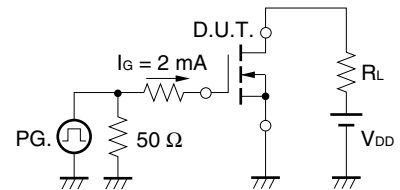
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I <sub>DSS</sub>			1	μA	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V
Gate Leakage Current	I <sub>GSS</sub>			±10	μA	V <sub>GS</sub> = ±12 V, V <sub>DS</sub> = 0 V
Gate to Source Cut-off Voltage	V <sub>GS(off)</sub>	0.5	1.0	1.5	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward Transfer Admittance *1	y <sub>fs</sub>	2.5			S	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 3.0 A
Drain to Source On-state Resistance *1	R <sub>DS(on)1</sub>	12	17.5	21.5	mΩ	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 3.0 A
	R <sub>DS(on)2</sub>	12.5	18	22	mΩ	V <sub>GS</sub> = 4.0 V, I <sub>D</sub> = 3.0 A
	R <sub>DS(on)3</sub>	14	19.5	25	mΩ	V <sub>GS</sub> = 3.1 V, I <sub>D</sub> = 3.0 A
	R <sub>DS(on)4</sub>	15.5	22.5	32	mΩ	V <sub>GS</sub> = 2.5 V, I <sub>D</sub> = 3.0 A
Input Capacitance	C <sub>iss</sub>		840		pF	V <sub>DS</sub> = 10 V,
Output Capacitance	C <sub>OSS</sub>		93		pF	V <sub>GS</sub> = 0 V,
Reverse Transfer Capacitance	C <sub>rss</sub>		65		pF	f = 1 MHz
Turn-on Delay Time	t <sub>d(on)</sub>		3		μs	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 3.0 A, V <sub>GS</sub> = 4 V, R <sub>G</sub> = 6 Ω
Rise Time	t <sub>r</sub>		6		μs	
Turn-off Delay Time	t <sub>d(off)</sub>		15		μs	
Fall Time	t <sub>f</sub>		10		μs	
Total Gate Charge	Q <sub>G</sub>		7.5		nC	V <sub>DD</sub> = 24 V, V <sub>GS</sub> = 4 V, I <sub>D</sub> = 6.5 A
Gate to Source Charge	Q <sub>GS</sub>		1.8		nC	
Gate to Drain Charge	Q <sub>GD</sub>		2.8		nC	
Body Diode Forward Voltage *1	V <sub>F(S-D)</sub>		0.83		V	I <sub>F</sub> = 6.5 A, V <sub>GS</sub> = 0 V

Note: \*1. Pulsed

**TEST CIRCUIT 1 SWITCHING TIME**

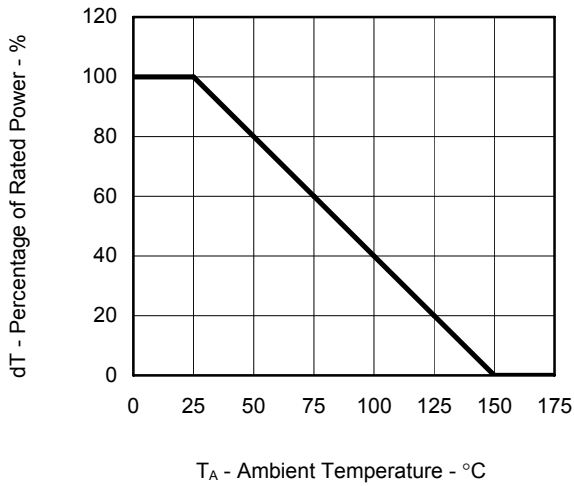


**TEST CIRCUIT 2 GATE CHARGE**

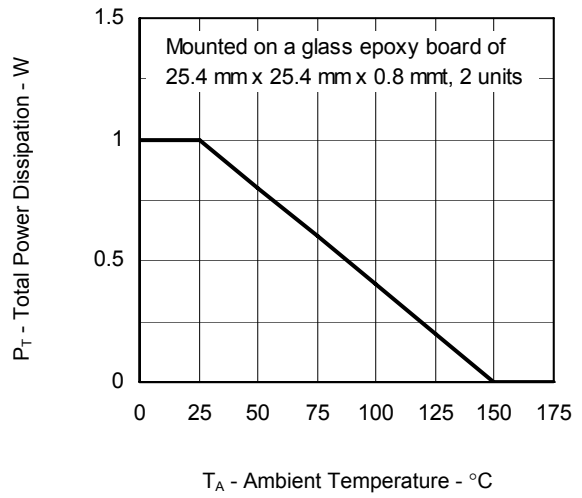


Typical Characteristics (T<sub>A</sub> = 25°C)

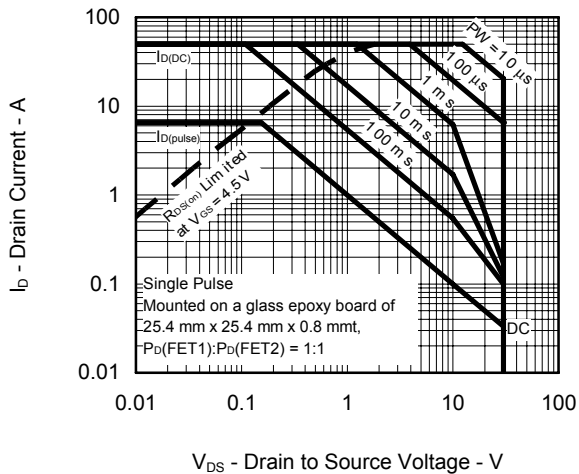
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



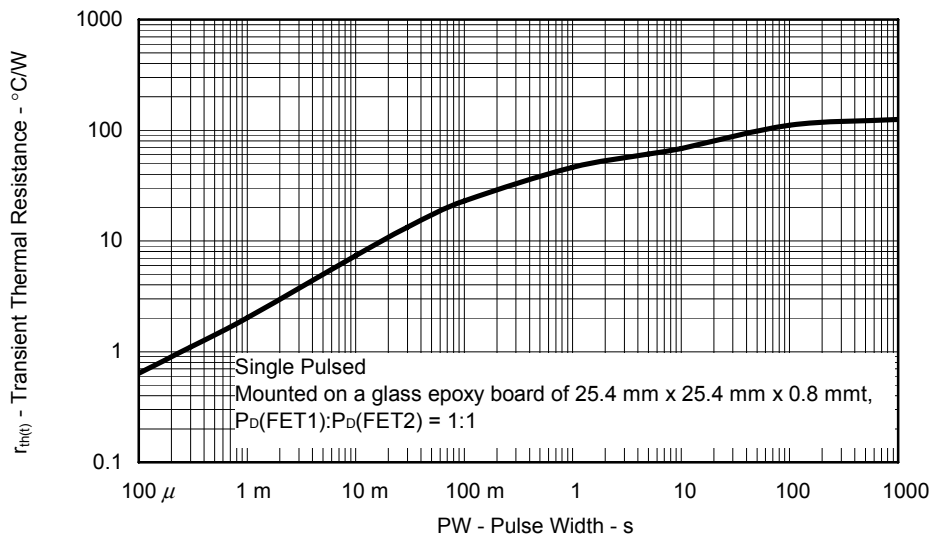
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



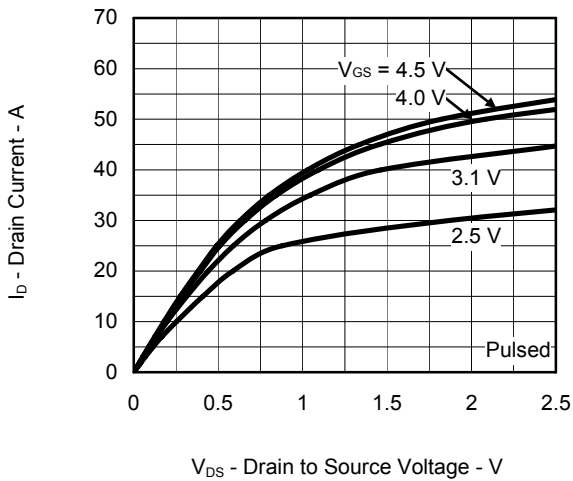
FORWARD BIAS SAFE OPERATING AREA



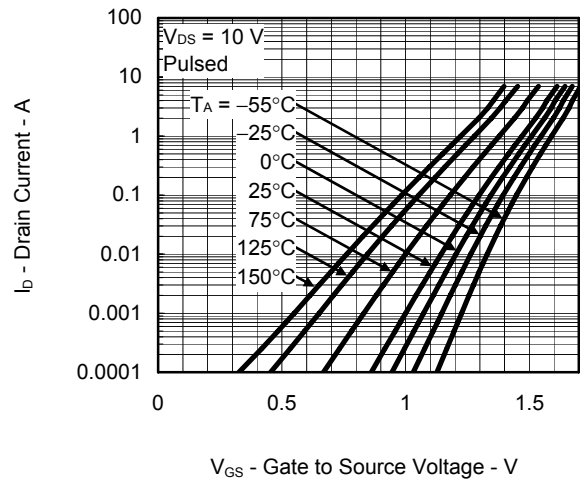
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



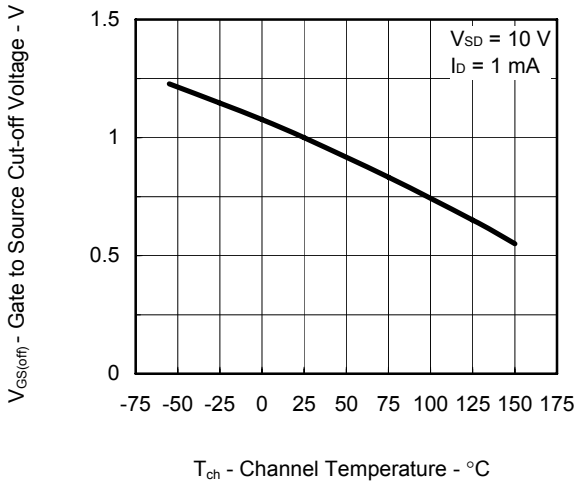
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



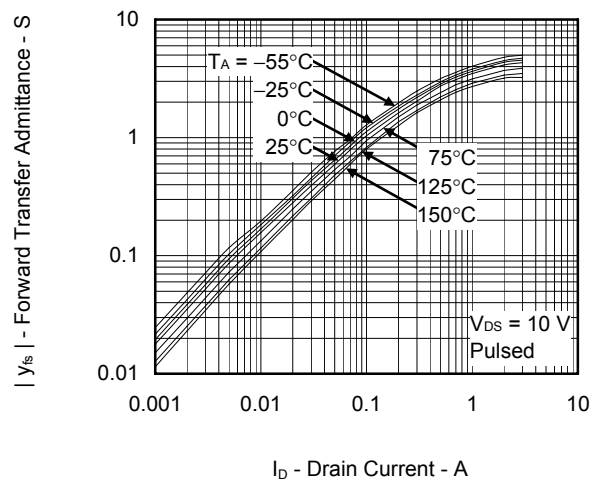
FORWARD TRANSFER CHARACTERISTICS



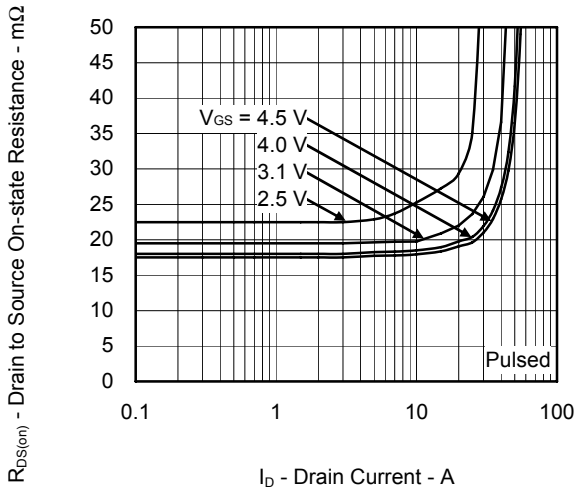
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



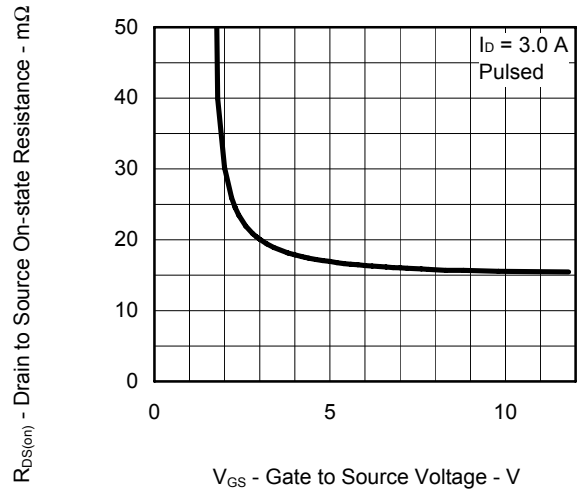
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



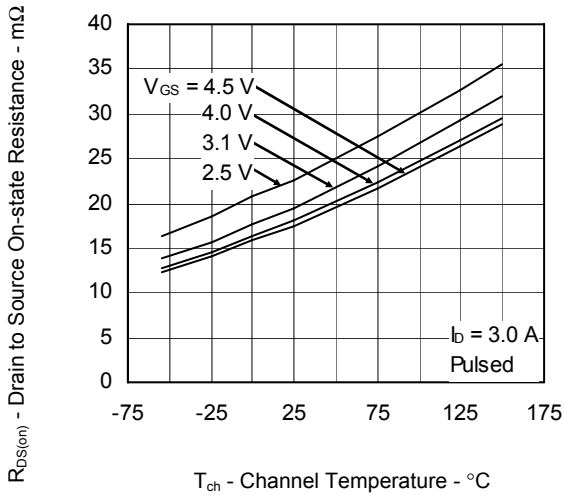
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



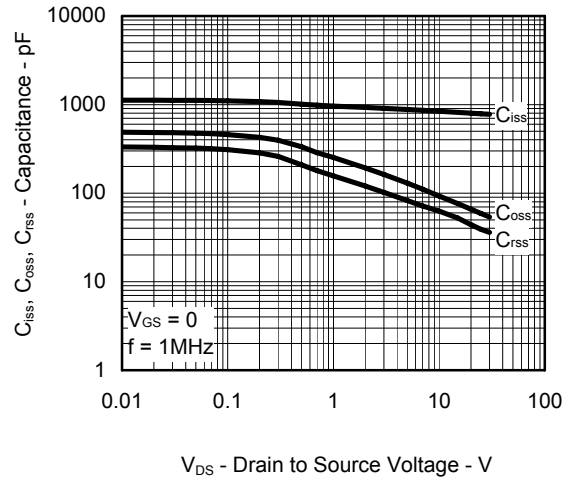
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



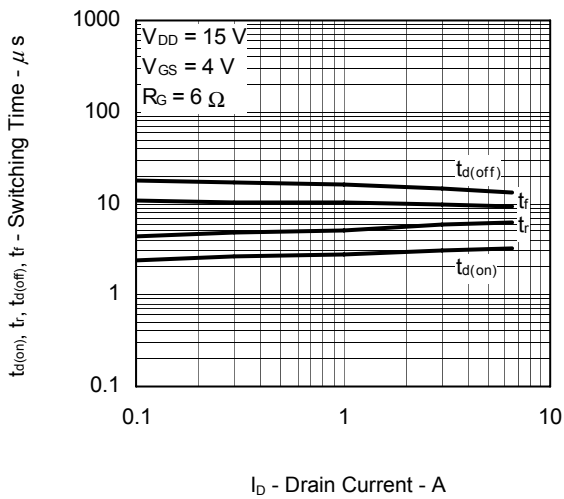
**DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE**



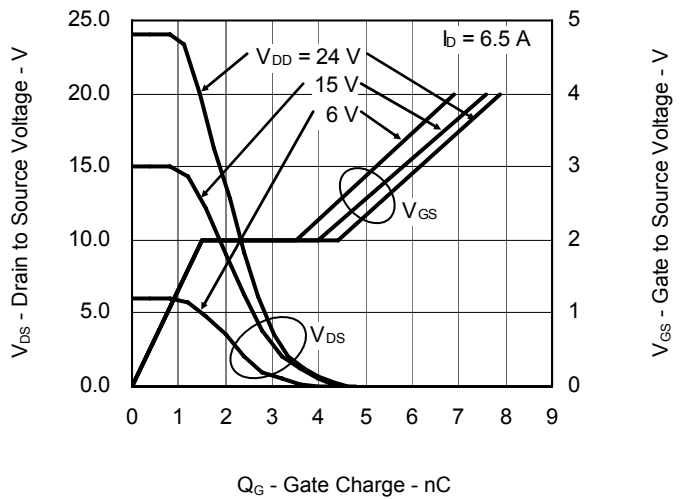
**CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE**



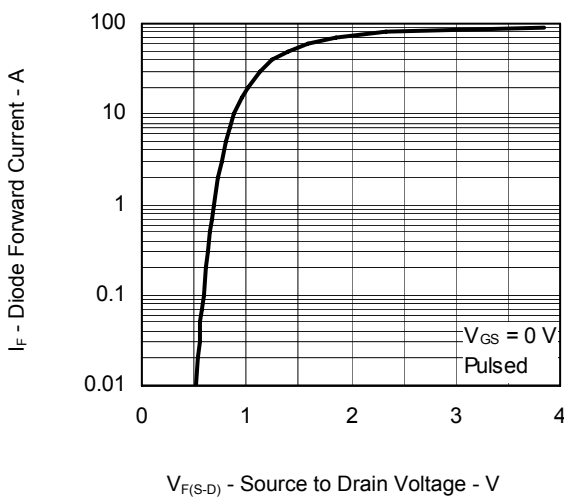
**SWITCHING CHARACTERISTICS**



**DYNAMIC INPUT/OUTPUT CHARACTERISTICS**

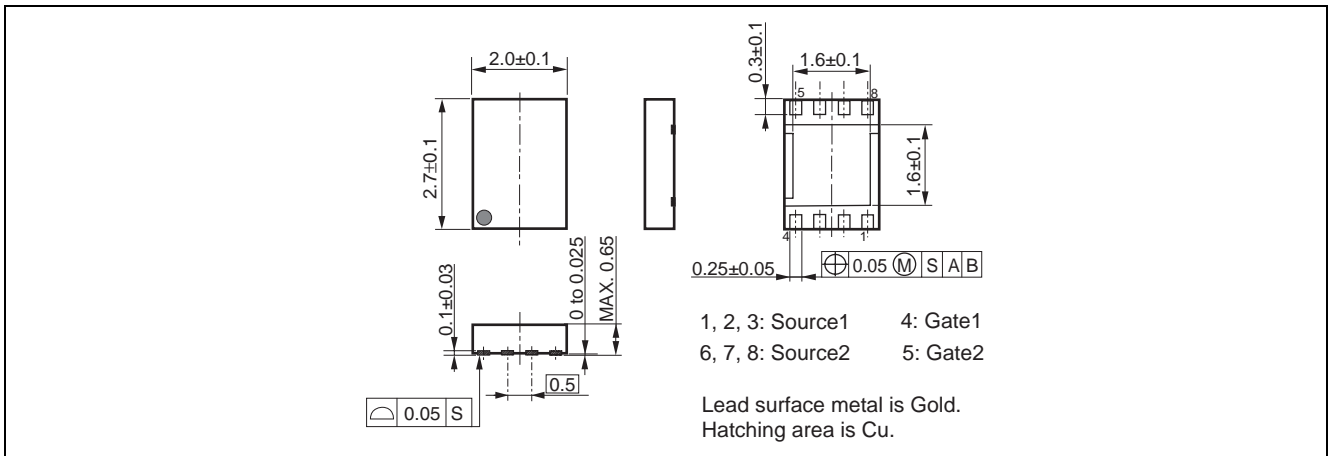


**SOURCE TO DRAIN DIODE FORWARD VOLTAGE**

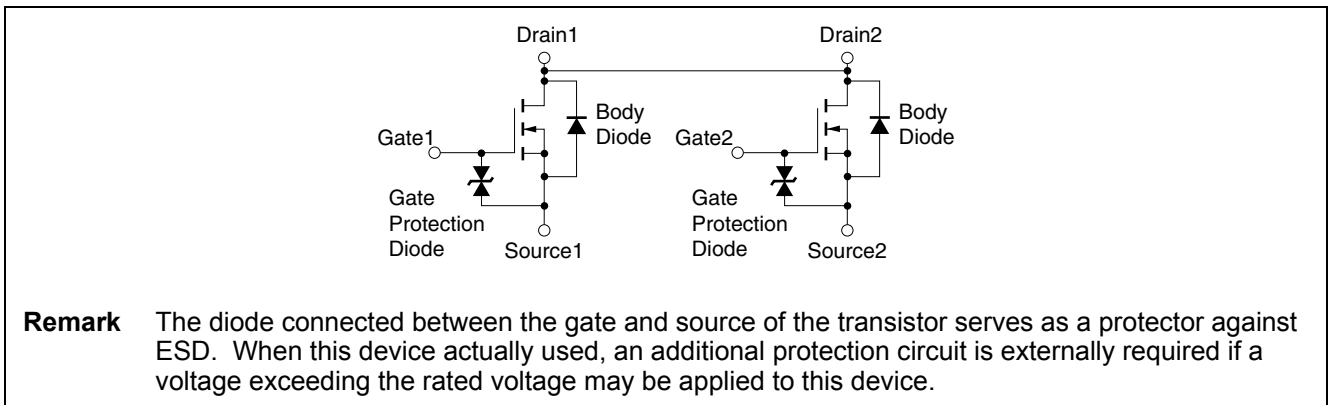


### Package Drawings (Unit: mm)

#### 8-pin HUSON (2720)



### Equivalent Circuit



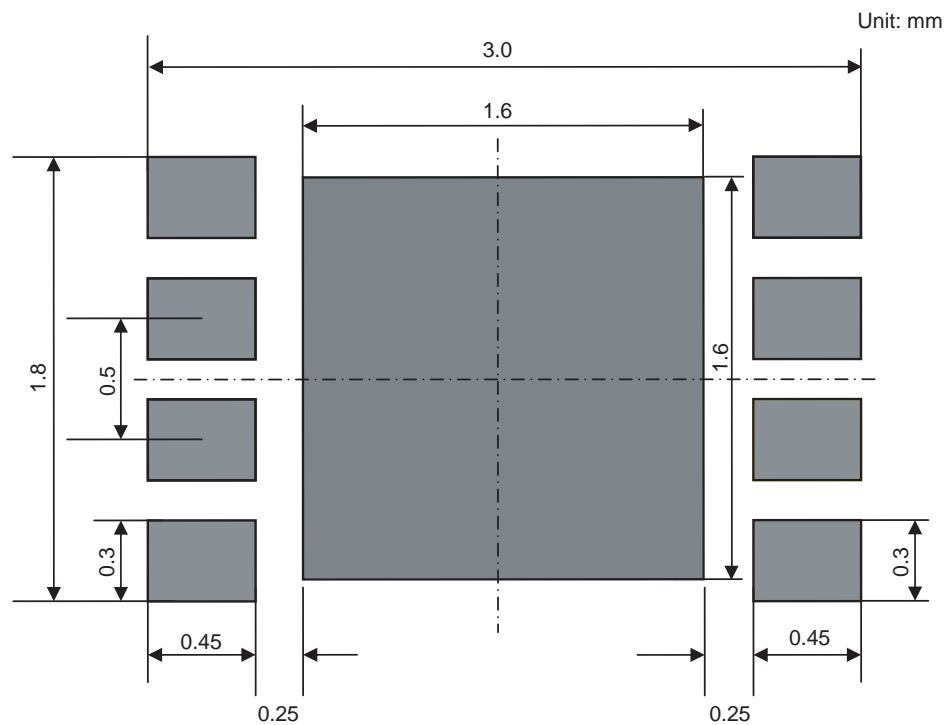
**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

### <Notes for using this device safely>

When you use this device, in order to prevent a customer's hazard and damage, use it with understanding the following contents. If used exceeding recommended conditions, there is a possibility of causing failure of the device and characteristic degradation.

1. When you mount the device on a substrate, carry out within our recommended soldering conditions of infrared reflow. If mounted exceeding the conditions, the characteristic of a device may be degraded and it may result in failure.
2. When you wash the device mounted the substrate, carry out within our recommended conditions. If washed exceeding the conditions, the characteristic of a device may be degraded and it may result in failure.
3. When you use ultrasonic wave to substrate after the device mounting, prevent from touching a resonance generator directly. If it touches, the characteristic of a device may be degraded and it may result in failure.
4. Please refer to **Figure 1** as an example of the land pattern. Optimize the land pattern in consideration of density, appearance of solder fillets, common difference, etc in an actual design.

**Figure 1. Example of the land pattern**



<b>Revision History</b>	<b><math>\mu</math>PA2461T1Q Data Sheet</b>
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<b>Rev.</b>	<b>Date</b>	<b>Description</b>	
		<b>Page</b>	<b>Summary</b>
1.00	Dec 06, 2010	–	First Edition Issued

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