

# μ PA2762UGR MOS FIELD EFFECT TRANSISTOR

## Description

The  $\mu$  PA2762UGR is N-Channel MOS Field Effect Transistor designed for power management applications of a notebook computer.

### Features

- Low on-state resistance
  - ----  $R_{DS(on)1} = 13.5 \text{ m}\Omega \text{ MAX}$ . ( $V_{GS} = 10 \text{ V}$ ,  $I_D = 12 \text{ A}$ )
  - R<sub>DS(on)2</sub> = 22 m $\Omega$  MAX. (V<sub>GS</sub> = 4.5 V, I<sub>D</sub> = 10 A)
- Low Ciss: Ciss = 710 pF TYP.  $(V_{DS} = 15 V, V_{GS} = 0 V)$
- Small and surface mount package (Power SOP8)
- RoHS Compliant

### **Ordering Information**

Part No.	LEAD PLATING	PACKING	Package
μ PA2762UGR-E1-AT <sup>*1</sup>	Pure Sn (Tin)	Tape 2500 p/reel	Power SOP8
μ PA2762UGR-E2-AT <sup>*1</sup>			0.08 g TYP.

Note: \*1. Pb-free (This product does not contain Pb in external electrode and other parts.)

### Absolute Maximum Ratings (T<sub>A</sub> = 25°C, All terminals are connected)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V <sub>GS</sub> = 0 V)	V <sub>DSS</sub>	30	V
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	V <sub>GSS</sub>	±20	V
Drain Current (DC)	I <sub>D(DC)</sub>	±12	A
Drain Current (pulse) *1	I <sub>D(pulse)</sub>	±50	A
Total Power Dissipation *2	P <sub>T1</sub>	1.1	W
Total Power Dissipation (PW = 10 sec) *2	P <sub>T2</sub>	2.5	W
Channel Temperature	T <sub>ch</sub>	150	°C
Storage Temperature	T <sub>stg</sub>	-55 to +150	°C
Single Avalanche Current *3	I <sub>AS</sub>	12	A
Single Avalanche Energy *3	E <sub>AS</sub>	14.4	mJ

Notes: \*1. PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1%

\*2. Mounted on glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mmt

\*3. Starting T<sub>ch</sub> = 25°C, V<sub>DD</sub> = 17.5 V, R<sub>G</sub> = 25  $\Omega$ , V<sub>GS</sub> = 20  $\rightarrow$  0 V, L = 100  $\mu$ H



ltem	Symbol	Min	Тур	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I <sub>DSS</sub>			1	μA	V <sub>DS</sub> = 30 V, V <sub>GS</sub> = 0 V
Gate Leakage Current	I <sub>GSS</sub>			±100	μA	$V_{GS}$ = ±20 V, $V_{DS}$ = 0 V
Gate Cut-off Voltage	V <sub>GS(off)</sub>	1.0		2.5	V	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 1 mA
Forward Transfer Admittance *1	y <sub>fs</sub>	3.5			S	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 6 A
Drain to Source On-state	R <sub>DS(on)1</sub>		11.0	13.5	mΩ	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 12 A
Resistance *1	R <sub>DS(on)2</sub>		15.8	22	mΩ	$V_{GS}$ = 4.5 V, I <sub>D</sub> = 10 A
Input Capacitance	C <sub>iss</sub>		710		pF	V <sub>DS</sub> = 15 V,
Output Capacitance	Coss		120		pF	V <sub>GS</sub> = 0 V,
Reverse Transfer Capacitance	C <sub>rss</sub>		71		pF	f = 1 MHz
Turn-on Delay Time	t <sub>d(on)</sub>		8.3		ns	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 6 A,
Rise Time	t <sub>r</sub>		3.9		ns	V <sub>GS</sub> = 10 V,
Turn-off Delay Time	t <sub>d(off)</sub>		28		ns	R <sub>G</sub> = 10 Ω
Fall Time	t <sub>f</sub>		5.5		ns	
Total Gate Charge	Q <sub>G</sub>		6.2		nC	V <sub>DD</sub> = 15 V,
Gate to Source Charge	Q <sub>GS</sub>		2.5		nC	V <sub>GS</sub> = 5 V,
Gate to Drain Charge	Q <sub>GD</sub>		3.0		nC	I <sub>D</sub> = 12 A
Body Diode Forward Voltage *1	V <sub>F(S-D)</sub>			1.2	V	I <sub>F</sub> = 12 A, V <sub>GS</sub> = 0 V
Reverse Recovery Time	t <sub>rr</sub>		22		ns	I <sub>F</sub> = 12 A, V <sub>GS</sub> = 0 V,
Reverse Recovery Charge	Q <sub>rr</sub>		15		nC	di/dt = 100 A/ <i>µ</i> s

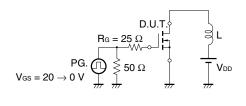
 $V_{\text{GS}}$ 

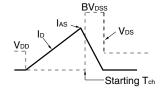
0

# Electrical Characteristics (T<sub>A</sub> = 25°C, All terminals are connected)

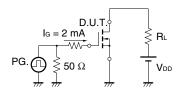
Note: \*1. Pulsed

### **TEST CIRCUIT 1 AVALANCHE CAPABILITY**

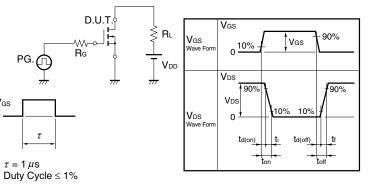




### **TEST CIRCUIT 3 GATE CHARGE**



#### **TEST CIRCUIT 2 SWITCHING TIME**

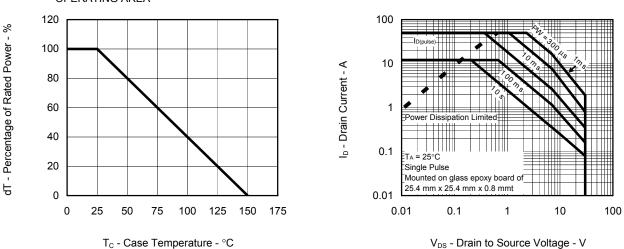




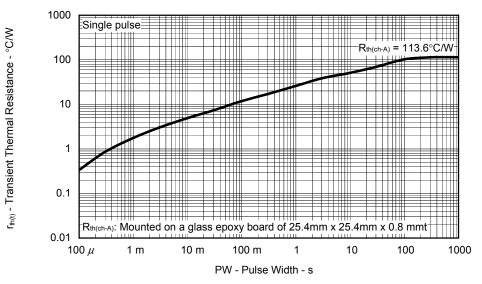
# Typical Characteristics (T<sub>A</sub> = 25°C)

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

FORWARD BIAS SAFE OPERATING AREA



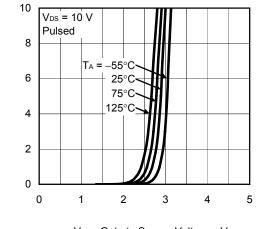
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH





50 40 l<sub>b</sub> - Drain Current - A V<sub>GS</sub> = 10 V 30 4.5 V 20 10 Pulsed 0 0 0.2 0.4 0.6 0.8 1 V<sub>DS</sub> - Drain to Source Voltage - V

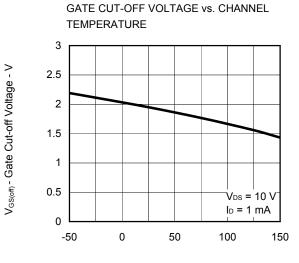
FORWARD TRANSFER CHARACTERISTICS



 $V_{\mbox{\scriptsize GS}}$  - Gate to Source Voltage - V



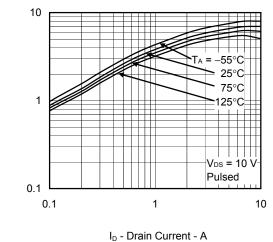
I<sub>D</sub> - Drain Current - A



T<sub>ch</sub> - Channel Temperature - °C

DRAIN TO SOURCE ON-STATE RESISTANCE vs.

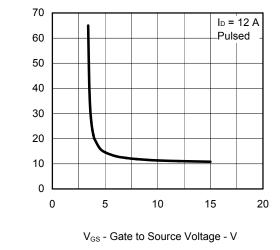
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



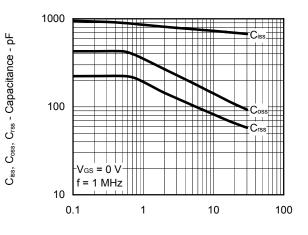
 $\mid y_{\rm fs} \mid$  - Forward Transfer Admittance - S

 $R_{DS(on)}$  - Drain to Source On-state Resistance -  $m\Omega$ 

DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



#### CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

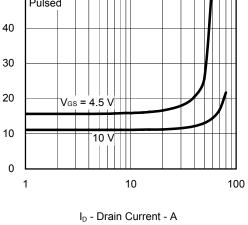


V<sub>DS</sub> - Drain to Source Voltage - V

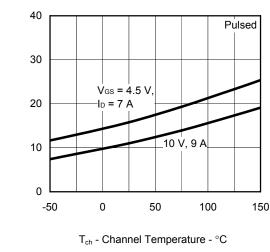
DRAIN CURRENT 50 Pulsed

 $R_{DS(on)}$  - Drain to Source On-state Resistance -  $m\Omega$ 

 $R_{\text{DS(on)}}$  - Drain to Source On-state Resistance -  $m\Omega$ 

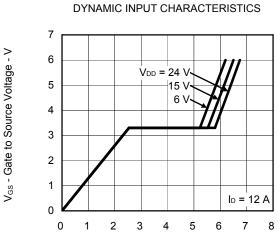


DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



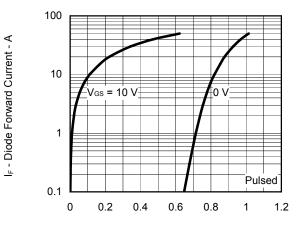
R07DS0011EJ0100 Rev.1.00 Jun 01, 2010





Q<sub>G</sub> - Gate Charge - nC

SOURCE TO DRAIN DIODE FORWARD VOLTAGE

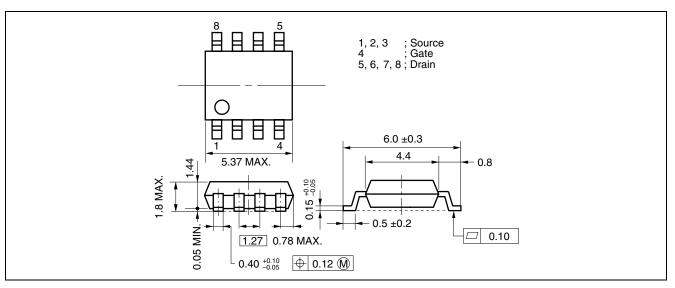


 $V_{\text{F(S-D)}}$  - Source to Drain Voltage - V

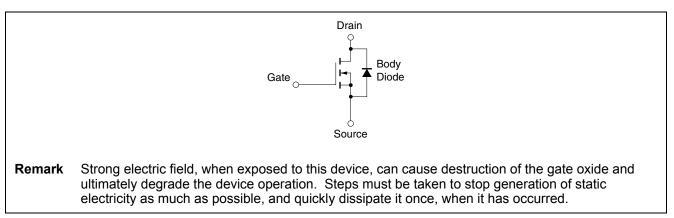


## Package Drawings (Unit: mm)

### Power SOP8



### **Equivalent Circuit**





<b>Revision History</b>	μΡΑ2762UGR

		Description		
Rev.	Date	Page	Summary	
1.00	June 01, 2010	-	First Eddition Issued	

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