μPA2762UGR

MOS FIELD EFFECT TRANSISTOR

R07DS0011EJ0100
Rev.1.00
Jun 01, 2010

Description

The μPA2762UGR is N-Channel MOS Field Effect Transistor designed for power management applications of a notebook computer.

Features

- Low on-state resistance
  - $R_{DS(on)1}$ = 13.5 mΩ MAX. (V_{GS} = 10 V, I_D = 12 A)
  - $R_{DS(on)2}$ = 22 mΩ MAX. (V_{GS} = 4.5 V, I_D = 10 A)
- Low Ciss: Ciss = 710 pF TYP. (V_{DS} = 15 V, V_{GS} = 0 V)
- Small and surface mount package (Power SOP8)
- RoHS Compliant

Ordering Information

Part No.	LEAD PLATING	PACKING	Package
μPA2762UGR-E1-AT *1	Pure Sn (Tin)	Tape 2500 p/reel	Power SOP8 0.08 g TYP.
μPA2762UGR-E2-AT *1			

Note: *1. Pb-free (This product does not contain Pb in external electrode and other parts.)

Absolute Maximum Ratings (T_A = 25°C, All terminals are connected)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	30	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$	±12	A
Drain Current (pulse) *1	$I_{D(pulse)}$	±50	A
Total Power Dissipation *2	P_{T1}	1.1	W
Total Power Dissipation (PW = 10 sec) *2	P_{T2}	2.5	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C
Single Avalanche Current *3	I_{AS}	12	A
Single Avalanche Energy *3	E_{AS}	14.4	mJ

Notes: *1. PW ≤ 10 μs, Duty Cycle ≤ 1%

*2. Mounted on glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mmt

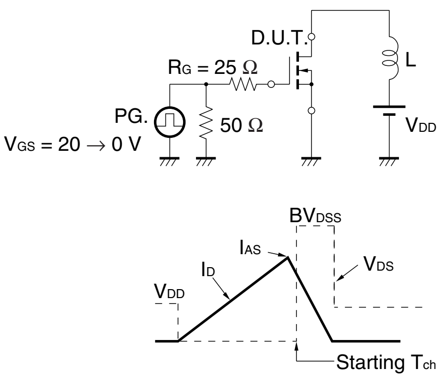
*3. Starting T_{ch} = 25°C, V_{DD} = 17.5 V, R_G = 25 Ω, V_{GS} = 20 → 0 V, L = 100 μH

Electrical Characteristics (T_A = 25°C, All terminals are connected)

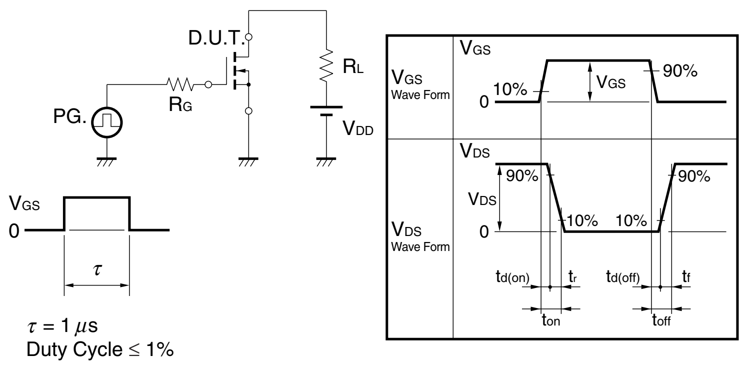
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}			1	μA	V_{DS} = 30 V, V_{GS} = 0 V
Gate Leakage Current	I_{GSS}			±100	μA	V_{GS} = ±20 V, V_{DS} = 0 V
Gate Cut-off Voltage	$V_{GS(off)}$	1.0		2.5	V	V_{DS} = 10 V, I_D = 1 mA
Forward Transfer Admittance *1	$\lvert y_{fs} \rvert$	3.5			S	V_{DS} = 10 V, I_D = 6 A
Drain to Source On-state Resistance *1	$R_{DS(on)1}$		11.0	13.5	mΩ	V_{GS} = 10 V, I_D = 12 A
	$R_{DS(on)2}$		15.8	22	mΩ	V_{GS} = 4.5 V, I_D = 10 A
Input Capacitance	C_{iss}		710		pF	V_{DS} = 15 V,
Output Capacitance	C_{oss}		120		pF	V_{GS} = 0 V,
Reverse Transfer Capacitance	C_{rss}		71		pF	f = 1 MHz
Turn-on Delay Time	$t_{d(on)}$		8.3		ns	V_{DD} = 15 V, I_D = 6 A,
Rise Time	t_r		3.9		ns	V_{GS} = 10 V,
Turn-off Delay Time	$t_{d(off)}$		28		ns	R_G = 10 Ω
Fall Time	t_f		5.5		ns	
Total Gate Charge	Q_G		6.2		nC	V_{DD} = 15 V,
Gate to Source Charge	Q_{GS}		2.5		nC	V_{GS} = 5 V,
Gate to Drain Charge	Q_{GD}		3.0		nC	I_D = 12 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$			1.2	V	I_F = 12 A, V_{GS} = 0 V
Reverse Recovery Time	t_{rr}		22		ns	I_F = 12 A, V_{GS} = 0 V,
Reverse Recovery Charge	Q_{rr}		15		nC	di/dt = 100 A/μs

Note: *1. Pulsed

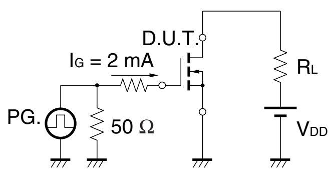
TEST CIRCUIT 1 AVALANCHE CAPABILITY



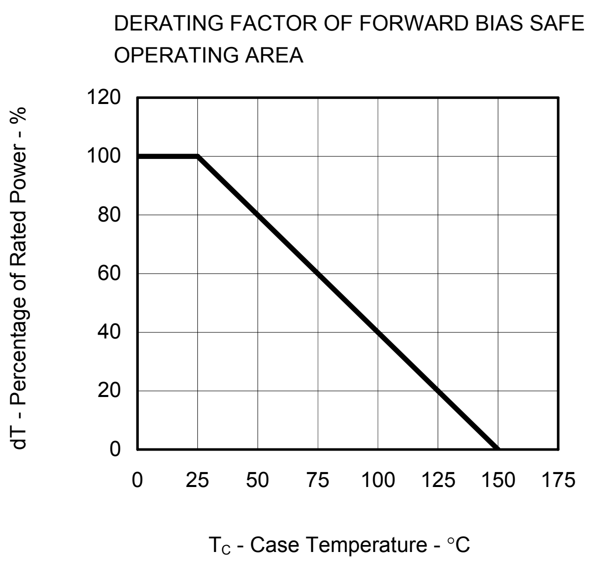
TEST CIRCUIT 2 SWITCHING TIME

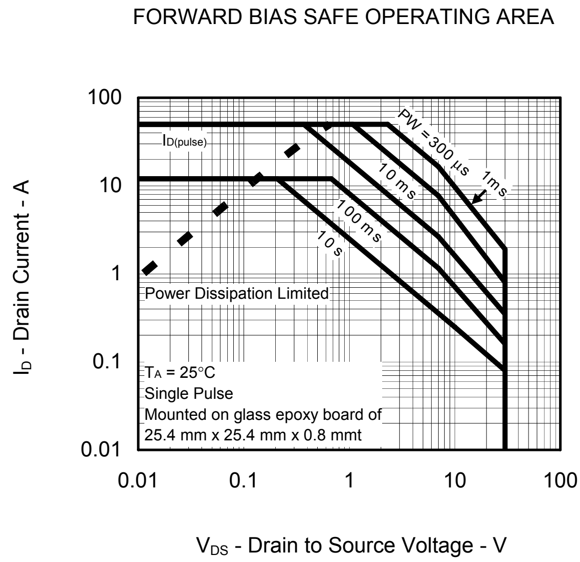


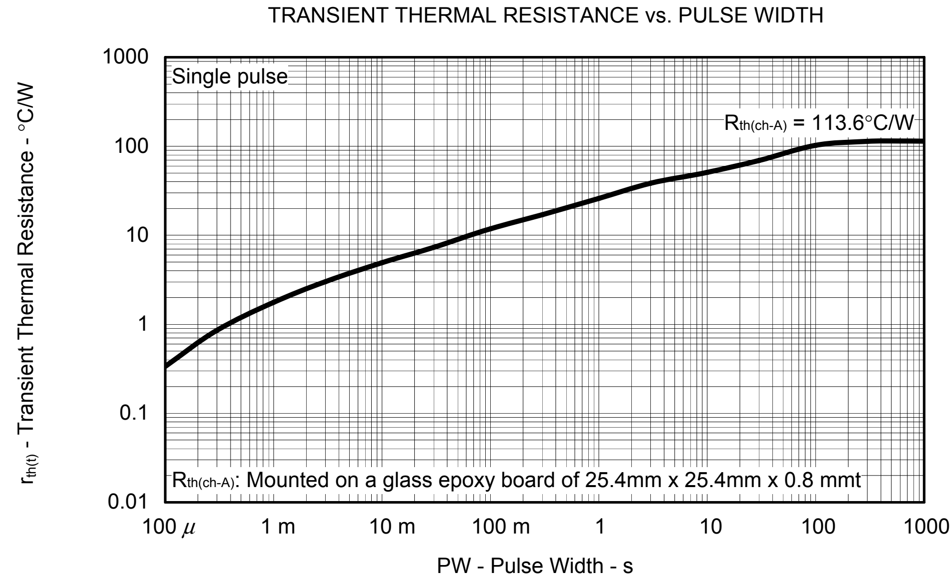
TEST CIRCUIT 3 GATE CHARGE

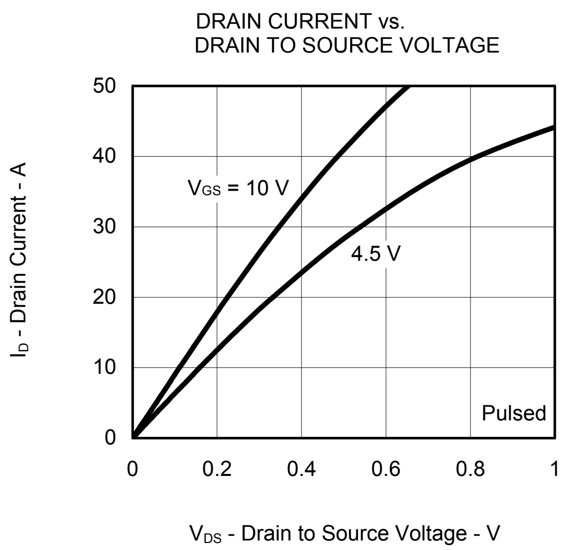


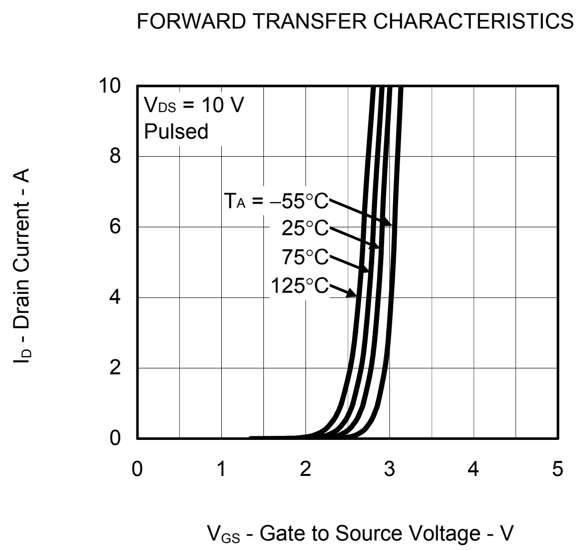
Typical Characteristics (T_A = 25°C)



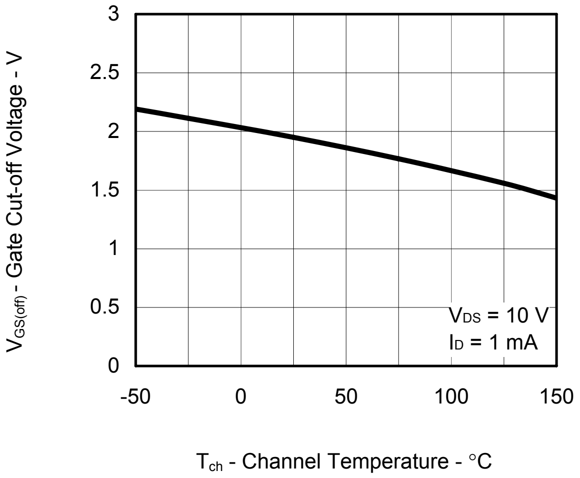




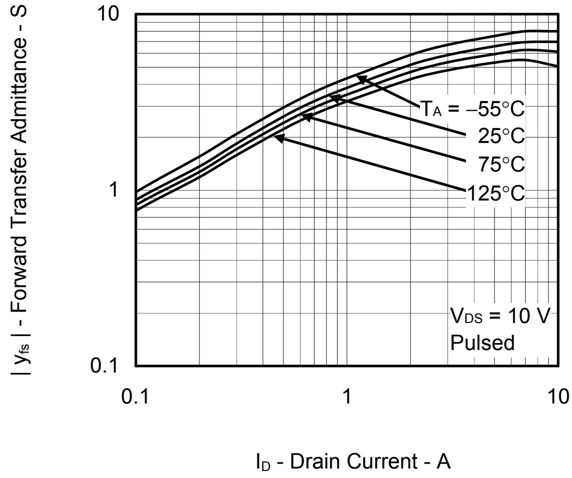




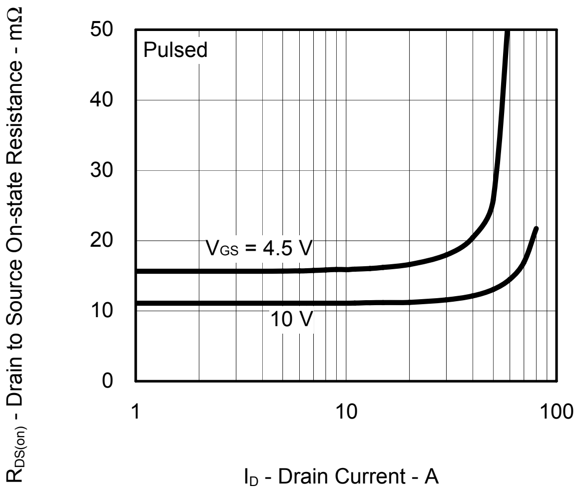
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



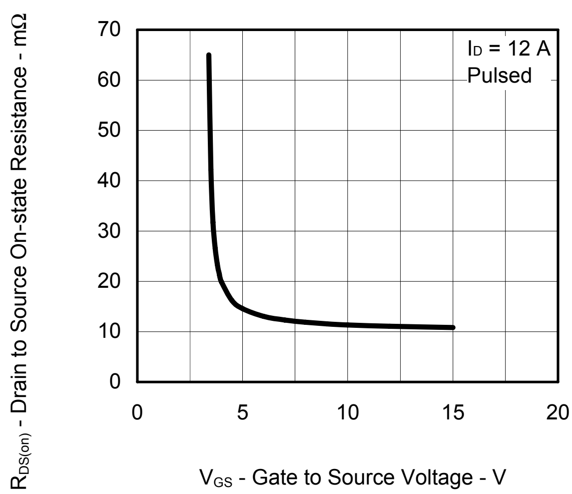
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



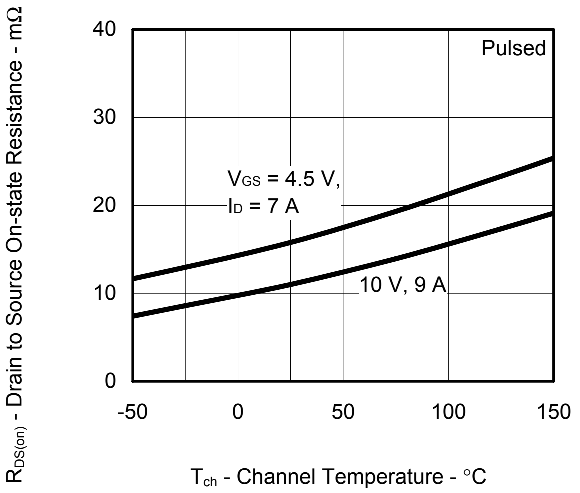
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



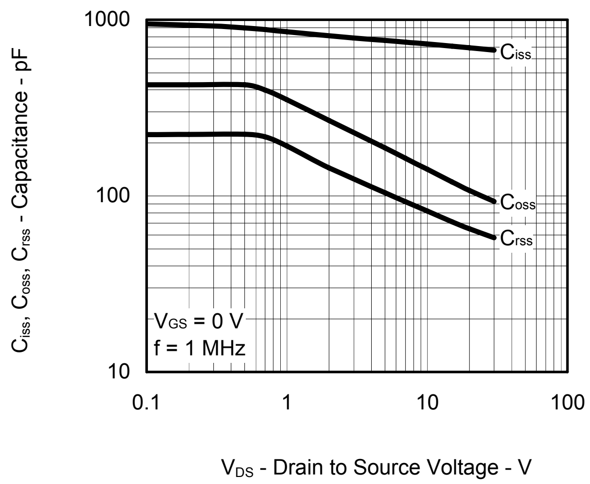
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



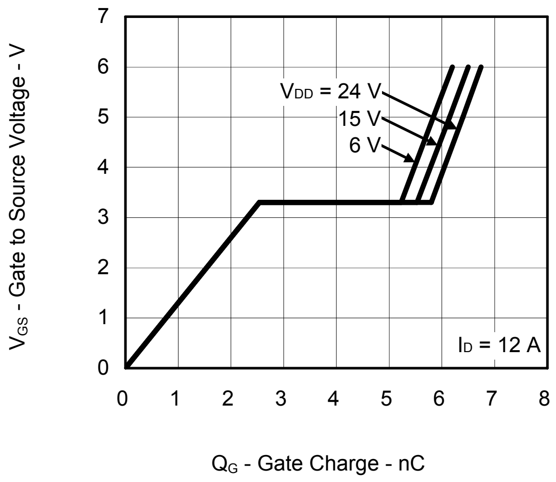
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



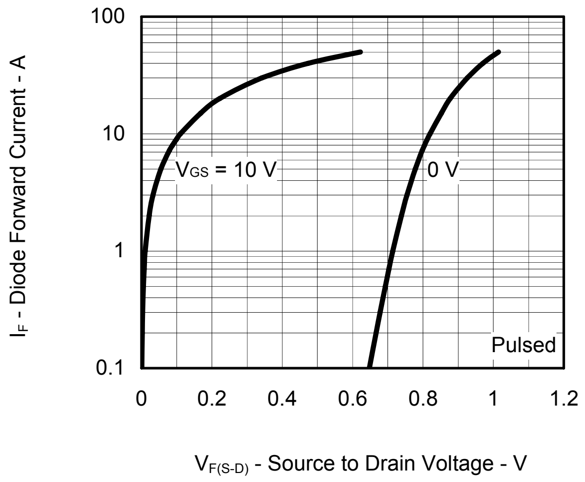
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



DYNAMIC INPUT CHARACTERISTICS

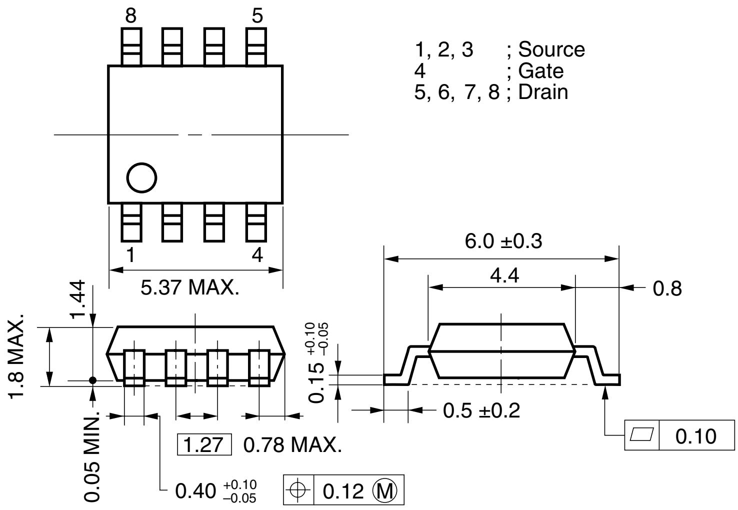


SOURCE TO DRAIN DIODE FORWARD VOLTAGE

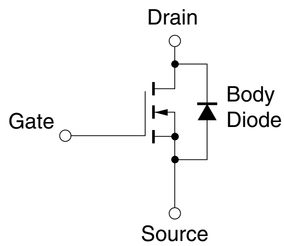


Package Drawings (Unit: mm)

Power SOP8



Equivalent Circuit



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Revision History	μPA2762UGR

Rev.	Date	Description	
		Page	Summary
1.00	June 01, 2010	–	First Eddition Issued

RENESAS

SALES OFFICES Renesas Electronics Corporation http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
7F, No. 363 Fu Shing North Road Taipei, Taiwan, R.O.C.
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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