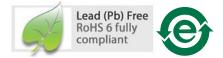


# PAW3212DB-TJDT ULTRA LOW POWER WIRELESS MOUSE SENSOR



## **General Description**

The PixArt PAW3212DB-TJDT is optimized for red LED based wireless mouse applications. It has low power architecture, high precision surface tracking ability, automatic power management modes, flexible programmable resolutions, configurable sleep and wake-up time which make it suitable for power-sensitive wireless mouse application. The PAW3212DB-TJDT is capable of high-speed motion detection up to the velocity of 30 inches/sec and acceleration of 10g.

**General Features** 

- Single power with wide voltage range Low Voltage Segment : 1.7V to 2.1V (VDD, VDDA short) High Voltage Segment : 2.1V to 3.6V (VDDA should connect a capacitor to GND)
- Selectable 3-wired (default) or 2-wired SPI serial interface
- Selectable 8-bit (default) or 12-bit motion data length for Delta\_X and Delta\_Y
- Selectable resolution up to 2400cpi with 38 cpi/ step (based on x1 lens magnification)
- Motion detection interrupt output
- Tracking speed up to 30ips (inches/sec) and 10g acceleration
- Built-in Low Power Timer (LPT) for Sleep1/ Sleep2/ Sleep3<sup>(1)</sup> mode
- Adaptive frame rate control for extra power saving during moving at different speeds

Key Specifications	
Supply Voltage	1.7V ~ 2.1V (VDD,VDDA short) 2.1V ~ 3.6V (VDDA should connect a capacitor to GND)
Interface	3-wired or 2-wired SPI Max clock speed : 2 MHz
Tracking Speed	Up to 30ips
Acceleration	Up to 10g
CPI Resolution	Up to 2400cpi with 38 cpi/step
Frame Rate	Adaptive frame rate Max : 4000 fps (frames per sec)
Operating Current	VDD=2.7V Run Avg : 0.25mA <sup>(2)</sup> Sleep1 : 16uA Sleep2 : 7uA Sleep3 : 4uA Power down : 3uA * Not including LED current
Package	iDIP 8

#### Note :

- 1. In default, Sleep3 is not enabled and it can be enabled by changing the setting in register 0x06 through SPI interface
- 2. An average current based on 85% weighting for sensor moving at speed  $\leq$  5ips and 15% weighting for speed >5ips



#### 1. Functional Block Diagram and Operation

PAW3212DB-TJDT is a high performance and ultra low power CMOS-processed optical image sensor with integrated digital image process circuits. It is based on an optical navigation technology which measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the speed, the direction and the magnitude of motion. The displacement delta\_X and delta\_Y information are available in registers which are accessible through SPI serial interface. A host controller reads and translates the data from the SPI serial interface into RF signals before sending them to the host PC. The word "sensor", instead of PAW3212DB-TJDT, is used in the document.

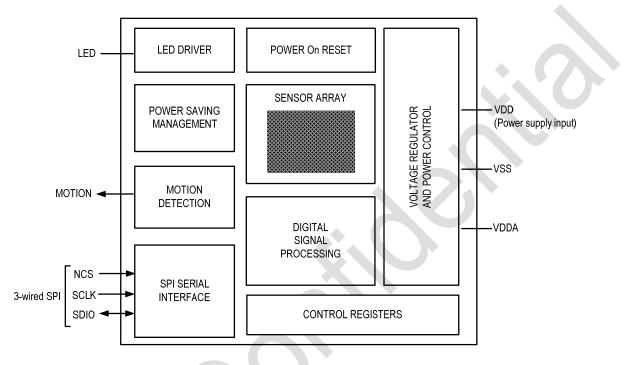


Figure 1. Function Block Diagram

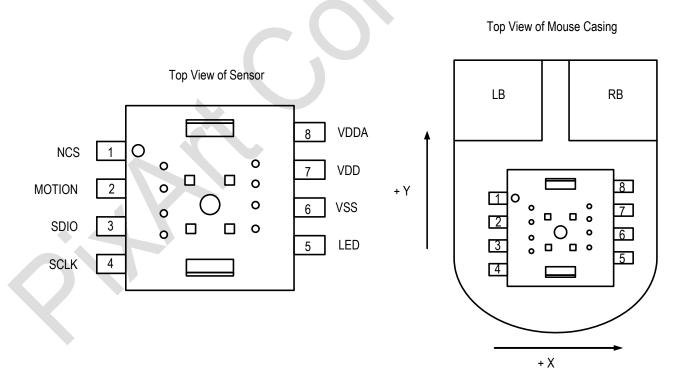


## 2. Pin Descriptions and Sensor Orientation

#### **Pin Descriptions**

Pin	Name	Туре	Definition
1	NCS	IN	Chip select for 3-wire SPI (active low). When using 2-wire SPI, this pin should tie to low
2	MOTION	OUT	Motion detection output (active low output)
3	SDIO	I/O	Bi-directional I/O for SPI
4	SCLK	IN	Clock input for SPI
5	LED	OUT	LED control
6	VSS	GND	Chip ground
7	VDD	PWR	VDD is the power supply input High Voltage Segment (VDD : 2.1V ~ 3.6V) : in this case, VDDA is the 1.8V regulator output and
8	VDDA	PWR	should connect a 4.7uF capacitor to GND. Low Voltage Segment (VDD : 1.7V ~ 2.1V) : VDDA should connect to VDD directly.

## **Sensor Orientation**



#### Figure 2. Orientation Relationship between Sensor and Mouse

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3. Z and 2D/3D Assembly

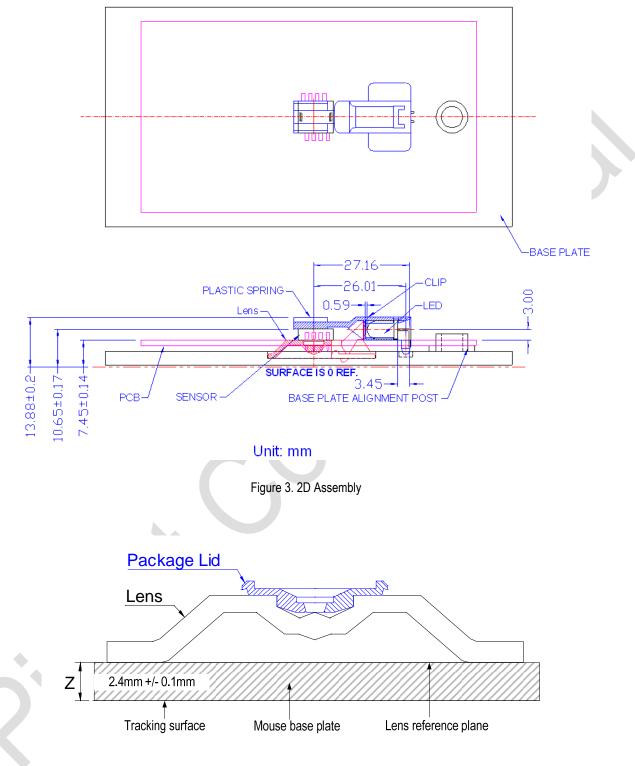


Figure 4. Distance from Lens Reference Plane to Tracking Surface





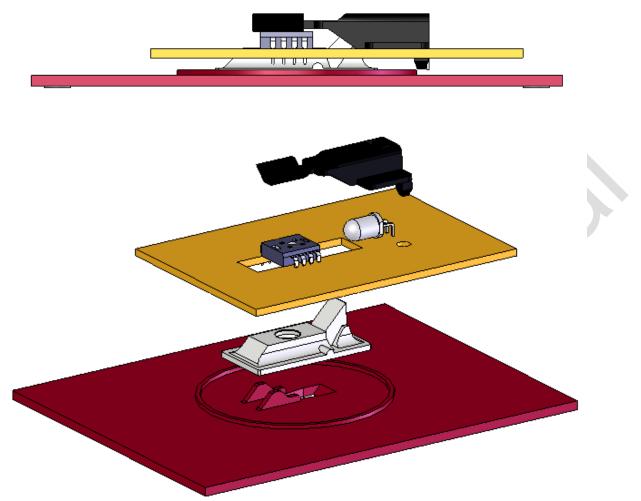
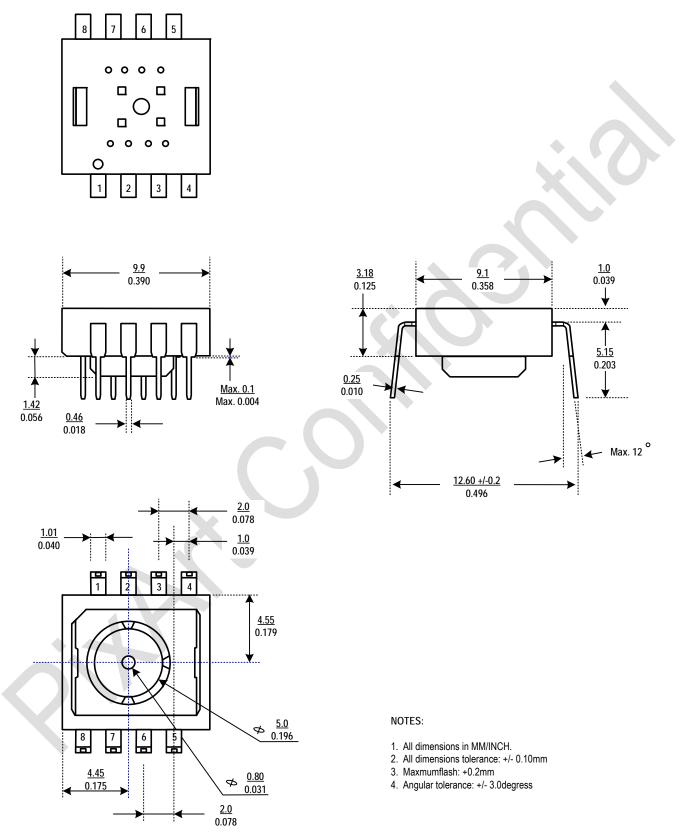


Figure 5. 3D Assembly for Mounting Instructions



PAW3212DB-TJDT

4. Package Information Package Outline Drawing





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PAW3212DB-TJDT



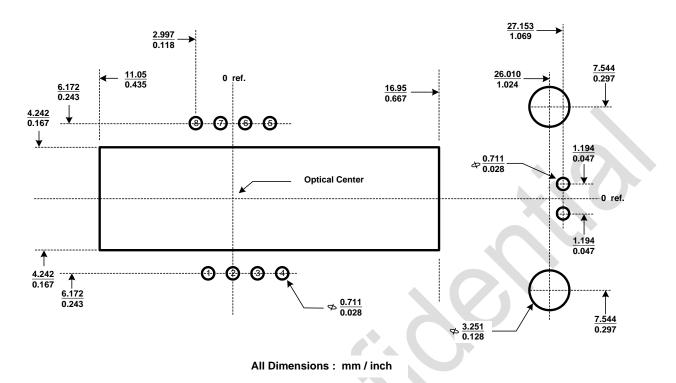
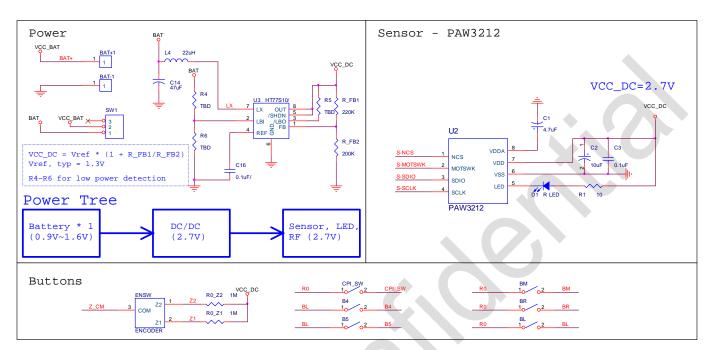


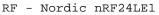
Figure 7. Recommended PCB Mechanical Cutouts and Spacing

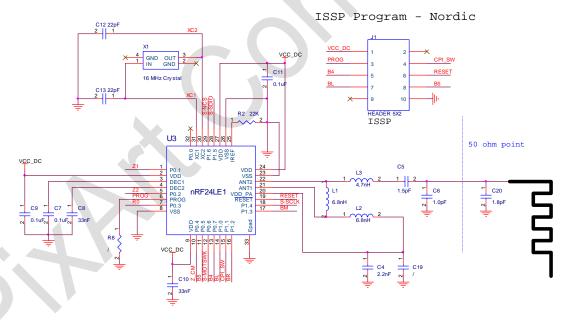


## 5. Reference Circuit Schematics

The reference circuit below is an example for a wireless red LED based mouse application with single AA or AAA battery, a DC/DC output at 2.7V and a Nordic RF IC as a host controller. This example is designed based on the High Voltage Segment configuration  $(2.1V \sim 3.6V)$ .











# 6. Specifications

#### Absolute Maximum Ratings

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are the stress ratings only and functional operation of the device at these or any other condition beyond those indicated for extended period of time may affect device reliability.

Symbol	Parameter	Min	Max	Unit	Notes
Tstg	Storage Temperature	-40	85	°C	
TA	Operating Temperature	-15	55	°C	
V <sub>DC</sub> DC Supply Voltage		-0.2	2.3	V	For Low Voltage Segment
	DC Supply Voltage	-0.3	3.9	V	For High Voltage Segment
VIN	DC Input Voltage	-0.3	VDC	V	All I/O pin
	Lead Solder Temp	-	260	°C	For 10 seconds, 1.6mm below seating plane.
ESD		-	2.0	kV	All pins, human body model MIL 883 Method 3015

## **Recommended Operating Conditions**

Recomm	ended Operating Conditions			Ċ		
Symbol	Parameter	Min	Тур	Мах	Unit	Notes
TA	Operating Temperature	0	-	40	°C	
	1.7	1.8	2.1	- V	Low Voltage Segment	
VDD	/DD Power Supply Voltage	2.1	2.7	3.6	- v	High Voltage Segment
VNPP	Supply Noise	-	-	100	mV	Peak to peak voltage within 10kHz - 80 MHz
SCLK	SPI Clock Frequency	-	-	2	MHz	
FR	Frame Rate		4000	-	frames/s	@ Run mode, +/- 5% tolerance
SP	Tracking speed	0	-	30	inches/s	
AC	Tracking acceleration	0	-	10	g	





# **AC Operating Conditions**

Electrical Characteristics over recommended operating conditions. Typical values at 25 °C, V<sub>DD</sub> = 2.7 V.

Symbol	Parameter	Min.	Тур.	Max.	Unit	Notes
FSCLK	SCLK frequency	-	-	2	MHz	SPI max. operation frequency
<b>t</b> <sub>NCSPU</sub>	NCS Low Time After Power-up	1	-	-	ms	NCS min. low time after power-up
tsclk-HI	SCLK High Time	250	-	-	ns	SCLK min. high time
tsclk-lo	SCLK Low Time	250	-	-	ns	SCLK min. low time
t <sub>NCS-LEAD</sub>	NCS Enable Lead Time	1	-	-	us	From NCS falling to first SCLK falling
t <sub>NCS-LAG</sub>	NCS Enable Lag Time	1	-	-	US	From Last SCLK rising to NCS rising
t <sub>NCS-HI</sub>	NCS min. High Time	2	-	-	us	From previous NCS rising to next NCS falling
tsetup-wr	SDIO Write Setup Time	250	-	-	ns	SDIO data valid before SCLK rising
thold-wr	SDIO Write Hold Time	250	-	-	ns	SDIO data valid after SCLK rising
t <sub>DLY-RD</sub>	SDIO delay after SCLK	-	-	50	ns	From SCLK falling to SDIO data valid, no load conditions
thold-rd	SDIO Read Hold Time	250	-	-	ns	SDIO data valid after SCLK rising
tsdio-r	SDIO Rise Time	-	30	-	ns	@C <sub>L</sub> = 30 pF
tsdio-f	SDIO Fall Time	-	30	-	ns	@CL = 30 pF
<b>t</b> RESYNC	SPI Re-Sync pulse width	1.0	-	-	US	Only for 2-wired SPI
t <sub>WDT</sub>	SPI Watch Dog Timer	1.7	-	-	ms	Only for 2-wired SPI
t <sub>QB</sub>	Quick Burst Pulse Width	2	-	100	us	Only for 2-wired SPI



# **DC Electrical Characteristics**

Electrical Characteristics over recommended operating conditions. Typical values at 25 °C, V<sub>DD</sub> = 2.7 V (Not including LED current)

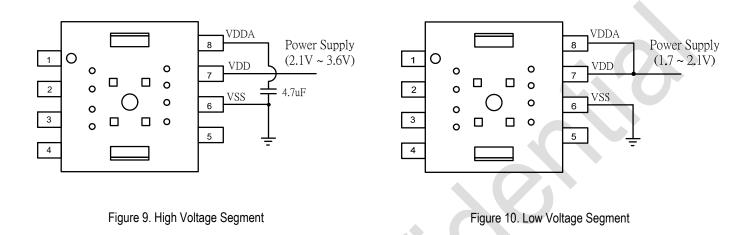
Symbol	Parameter	Min.	Тур.	Max.	Unit	· · · · · · · · · · · · · · · · · · ·
Operation cu	rrent of VDD pin					
Iddnm	Run mode Current	-	250	-	uA	85% weighting for speed $\leq$ 5ips and 15% weighting on speed >5ips
IDDS1	Sleep1 Current	-	16	-	uA	Based on the setting in register 0x0A Slp1_Freq[3:0] =7 (32ms)
IDDS2	Sleep2 Current	-	7	-	uA	Based on the setting in register 0x0B Slp2_Freq[3:0] = 1 (128ms)
I <sub>DDS3</sub>	Sleep3 Current	-	4	-	uA	Based on the setting in register 0x0C Slp3_Freq[3:0] = 7 (512ms)
IDDPD	Power Down Current	-	3	-	uA	
NCS, SCLK, S	SDIO, MOTION pins					
VIH	Input Voltage High	VDD*0.7	-	-	V	
VIL	Input Voltage Low	-	-	VDD*0.3	V	
Vон	Output Voltage High	VDD-0.4	-	-	V	@I <sub>ОН</sub> = 2mA
Vol	Output Voltage Low	-	-	0.4	V	@I <sub>OL</sub> = 2mA
LED pin						
Vol	Output Voltage Low	-	-	100	mV	@loL = 10mA
LEDS	LED Sink Current	-	-	50	mA	



## PAW3212DB-TJDT

#### 7. Power Supply Configuration

The sensor has 2 segments for power supply configuration, the High Voltage Segment and the Low Voltage Segment. With these two segments, the sensor provides the flexibility to applications with different power consideration. For High Voltage Segment, which means the power supply voltage ranges from 2.1V to 3.6V, the power pins VDD and VDDA of the sensor should be connected as shown in Figure 9. For Low Voltage Segment, which means the power supply voltage ranges from 1.7V to 2.1V, the power pins VDD and VDDA of the sensor should be connected as shown in Figure 10.



The sensor's power-up default settings are for the High Voltage Segment. If users want to use the Low Voltage Segment, one sensor register (address 0x4B) should be set (value 0x40) after the power-up sequence. If this register is not set properly, the sensor would consume extra power due to the current leakage of the internal regulator.

Write address 0x09 = 0x5A;	to disable Write Protect
Write address 0x4B = 0x04;	to turn off internal regulator for Low Voltage Segment
Write address 0x09 = 0x00;	to enable Write Protect



## 8. 3-wired SPI Serial Interface

The sensor supports 3-wired Serial Peripheral Interface (SPI). The host controller can use the SPI to write and read registers in the sensor, and to read out the motion information. The host controller always initiates communication; the sensor never initiates data transfers. NCS, SCLK and SDIO may be driven directly by the host controller. SDIO may also be driven by the sensor when data is read out from sensor registers.

- NCS : Chip select input (active low). NCS needs to be low to activate the SPI; otherwise, SDIO will be at high-Z state and SCLK will be ignored. NCS can also be used to reset the SPI in case a communicational error happens.
- SCLK : Clock input. It is always generated by the host controller.
- SDIO : Bi-directional input/output data

## NCS Low at Power-up Stage

In order to keep the 3-wired SPI function work correctly, the host controller MUST force NCS pin to low during the power-up stage and continues forcing for at least 1ms after the VDD power is stable. The host controller should always keep NCS pin high when SPI interface is idle.

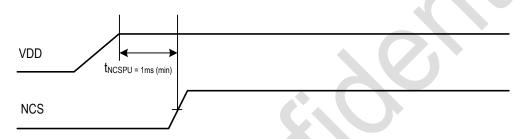


Figure 11. NCS Low at Power-up Sequence

#### **Transmission Protocol**

The transmission protocol is a 3-wired link, half duplex protocol between the host controller and the sensor. All data changes on SDIO are initiated by the falling edge on SCLK. The host controller always initiates communication; the sensor never initiates data transfers. The transmission protocol consists of the following two operation modes.

- Write Operation
- Read Operation

Both of the two operation modes consist of two bytes. The first byte contains the address (seven bits) and has a bit-7 as its MSB to indicate data direction. The second byte contains the data.

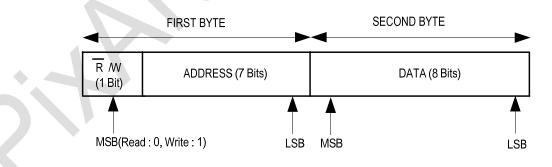
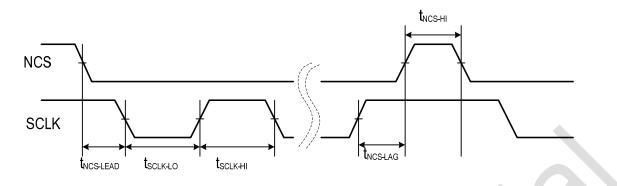


Figure 12. Transmission Protocol

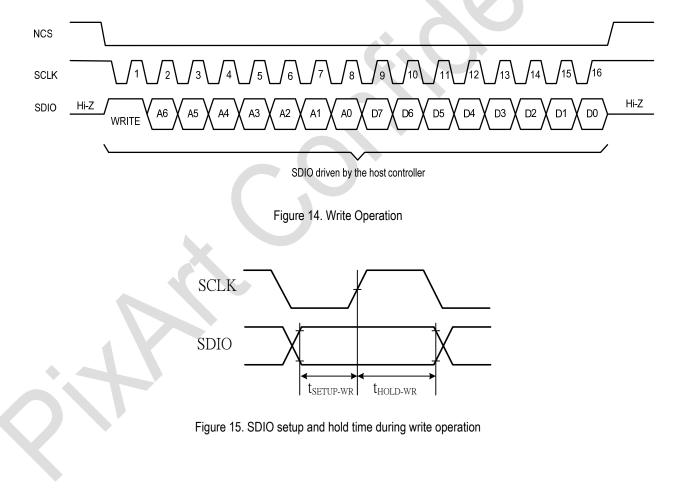






## Write Operation

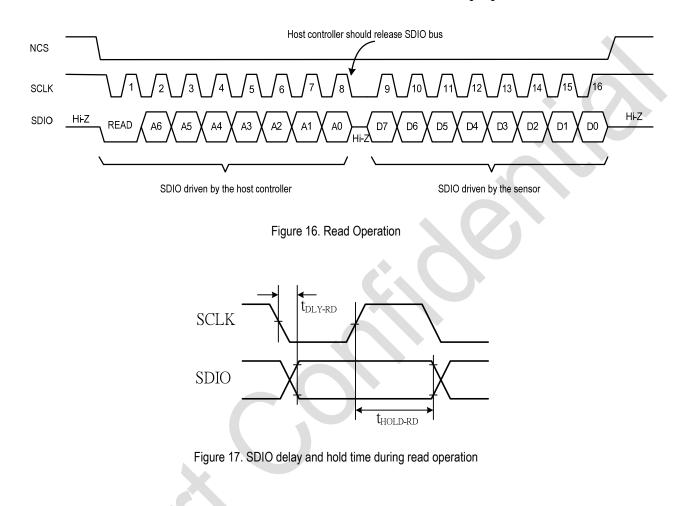
A write operation, defined as data is going from the host controller to the sensor, is always initiated by the host controller and consists of two bytes. The first byte contains the address (seven bits) and has a "1" as its MSB to indicate data direction. The second byte contains the data. The communication is synchronized by SCLK. The host controller changes SDIO on the falling edges of SCLK and the sensor reads SDIO on the rising edges of SCLK.





## **Read Operation**

A read operation is initiated by the host controller and consists of two bytes. The first byte contains the address specified by the host controller and has a "0" as its MSB to indicate data direction. The second byte contains the data which is outputted by the sensor. The communication is synchronized by SCLK. SDIO is changed on the falling edges of SCLK and is read on every rising edge of SCLK. The host controller must release SDIO bus and handover the control of SDIO bus to the sensor on the falling edge of last address bit.





#### 9. 2-wired SPI Serial Interface

To be compatible to PixArt previous generation mouse sensors, the sensor reserves 2-wired SPI interface mode (SCLK, SDIO). All the transmission protocols are exactly the same as 3-wired SPI except the NCS pin is ignored in 2-wired SPI mode.

#### Switching to 2-wired SPI Mode

Since the 3-wired SPI is the power-on default setting of the sensor, the host controller has to write sensor registers to switch the sensor from 3-wired SPI mode to 2-wired SPI mode after the sensor power-up sequence. By forcing the NCS pin to low, the host is able to write the registers below to switch to 2-wired SPI mode. Without writing the registers below, the re-synchronization mechanism will be invalid.

Write address 0x09 = 0x5A;	to disable Write Protect
Write address 0x26 = 0x34;	to switch to 2-wired SPI and disable NCS pin function
Write address 0x09 = 0x00;	to enable Write Protect

## Re-synchronization of the SPI

Two possible conditions listed below might cause the 2-wired SPI being out of synchronization and the host controller will not be able to correctly access the registers of the sensor.

- Wrong system power-up sequence The host controller begins to toggle the SPI while the sensor has not finished the power-up sequence.
- Unexpected ESD event When ESD event happens, the SCLK signal might be destroyed by electric surge and causes the SPI being out of synchronization.

Since there is no NCS function to reset the SPI bus when SPI communication is being out of synchronization, a special mechanism is needed to reset the SPI. To recover the correct communication of SPI, the host controller can de-assert the SCLK for at least treesync (1us min), and then keep SCLK asserted for a certain time interval twDT (1.7ms, min) as shown in Figure 17. to force the SPI control circuits of the sensor to reset. This method of re-synchronization is called "watchdog timer timeout". The re-synchronization will only reset the SPI circuits of the sensor, and the existing sensor register values will keep unchanged. Be noticed that this re-synchronization is NOT valid when the sensor is at power down mode. If users perform re-synchronization during power down mode, the SPI will be out of synchronization. To make sure if the 2-wired SPI interface is back to synchronization, the host controller could read register address 0x00 to check if the value is 0x30. If the value is not correct, please perform re-synchronization again until the correct value (0x30) has been read.

SCLK	twdt (1.7ms, min)		9 10 11 12 13 14 15 16
	Being un-synchronous state	Being synchronous state	*
SDIO		Hi-Z (ADDRESS (RW)	DATA

Figure 18. Re-synchronization the SPI Using Watchdog Timer



#### 10. Pin1 Functions in 2-wired SPI Mode

After the sensor has been successfully switched to 2-wired SPI mode, the NCS pin will lose its original function in 3-wired SPI mode. Thus the NCS pin (Pin1) can be further switched to the following three different functions according to Pin1\_Sel bits (bit 5 and 4) in register SPI\_Sel (address 0x26).

#### Hardware Reset Function

The host controller can assert Pin1 to reset the sensor. A full chip reset will thus be executed, just like the effect of using Software Reset Function. After the reset, all the recommended register settings must be reloaded to ensure the sensor works properly.

#### Quick Burst (QB) Function

This function is to reduce the host controller SPI access time thus to save the power of the host controller. In QB mode, the host controller doesn't need to specify the sensor address through SPI interface to get sensor motion data.

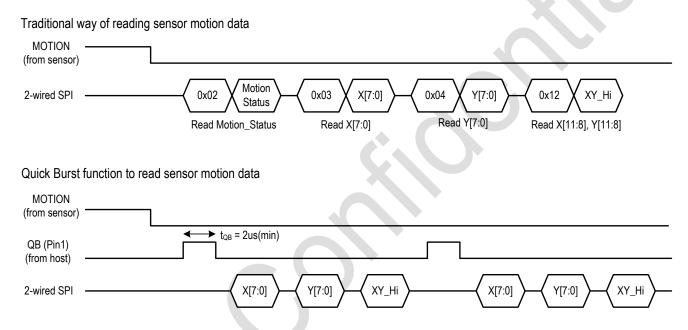


Figure 19. Reading motion data via Quick Burst function and traditional function

## Hardware Power-Down Function

The host controller can assert Pin1 to force the sensor operated at extremely low power state, just like the effect of using Software Power-Down function.



## 11. MOTION Pin Function

The MOTION pin will go from high to low or keep low whenever the sensor detects the occurrence of motion. The MOTION pin can be used to monitor whether if the sensor motion data has been cleared. If the motion data is not cleared, MOTION pin will remain low. After all the motion data is read out by the host controller (i.e. Motion bit, Delta\_X and Delta\_Y are all zero), the MOTION pin will go high. When a mouse system is working at an idle state where the sensor is at Sleep1/Sleep2/Sleep3 mode and the host controller is at idle mode, and when the sensor detects the occurrence of motion, the MOTION pin will go low. The falling edge on MOTION pin can be used as an interrupt event to wake up the host controller.



State 1 : No motion detected. Register Motion, Delta\_X and Delta\_Y are all zero.

State 2 : Motion detected. Register Motion =1 and Delta\_X and Delta\_Y are available to read (non-zero values).

State 3 : Motion continues. Register Motion =1 and Delta\_X and Delta\_Y are available to read (non-zero values).

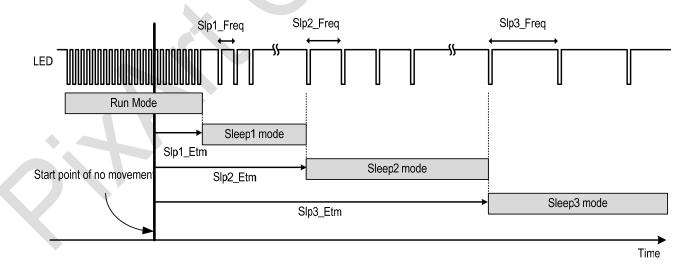
State 4 : Motion stops and the last reports of motion have been read out. Register Motion, Delta\_X and Delta\_Y are all zero.

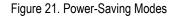
State 5 : No motion detected. Register Motion, Delta\_X and Delta\_Y are all zero.

#### Figure 20. Motion Function

#### 12. Power Management Modes

The sensor has three power-saving modes (Sleep1, Sleep2 and Sleep3). Each mode has a different motion detection period to detect the motion periodically. When left idle, the sensor automatically changes from Run mode to Sleep1 mode, to Sleep2 mode and finally to Sleep3 mode which consumes the least current. Be noticed that the current consumption is the lowest at Sleep3 mode and highest at Sleep1 mode, however the time required for the sensor to "wake up" to Run mode from Sleep1 mode is the shortest and longest from Sleep3 mode. The entering time (Slp1\_Etm, Slp2\_Etm, Slp3\_Etm) is the elapsed time from the time when the sensor is idle to Sleep modes. The sampling frequency time (Slp1\_Freq, Slp2\_Freq, Slp3\_Freq) is the time period to detect the motion under Sleep modes. The relationship between the entering time and the sampling frequency time is shown in figure below.







#### 13. Software Power-Down Function

The sensor can be placed in an extremely low power state (power-down mode) by setting PD\_enh bit (bit 3) in the register Configuration (address 0x06) through SPI interface. In power-down mode, all the sensor register settings are retained and can be accessed through SPI interface as well. To get the sensor out of the power-down mode, please just reset the PD\_enh bit. To get more accurate motion reports, it is recommended that the host controller should wait at least 3ms before reading the motion reports after resetting the PD\_enh bit.

## 14. Software Reset Function

During power-up, the sensor does not need an external power-on reset as there is an internal circuitry that performs power-on reset function in the sensor. However the sensor can also be reset by setting the Reset bit (bit 7) of register Configuration (address 0x06). A full chip reset will thus be executed and all the registers will be reset to power-on default values. After the reset, all the recommended register settings must be reloaded to ensure the sensor works properly.



15. Optical Criterion

## Recommended Red LED Angle Criterion

Recommend using Chang-Yu LED goniophotometer V110 to measure the LED viewing angle.

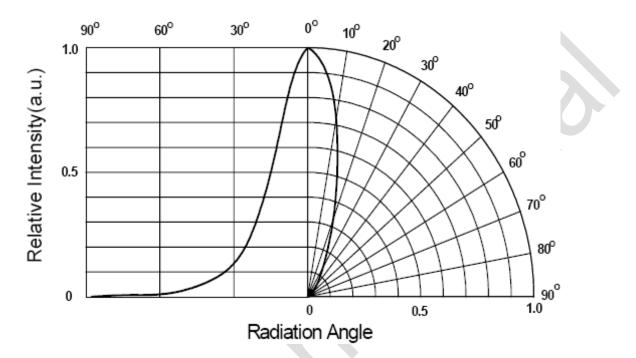


Figure 22. Radiation Characteristics

LED Viewing Angle	Min.	Тур.	Max.
201/2	24	30	36

Recommended Red LED Optical Power

In order to optimize the tracking performance and minimize the LED power consumption, PixArt recommends the LED optical power conform with the table listed below. LED optical power is measured through the base plate opening of the mouse casing with the LED set to continuous mode. Recommend using ADCMT power meter 8230E to measure the LED optical power. The sequence to set LED to continuous mode is as followed.

*Write address 0x09 = 0x5A; Write address 0x5B = 0x63;* 

to disable Write Protect to set LED to continuous mode

Parameter	Min.	Тур.	Max.	Unit
Red LED Optical Power	1600	-	-	uW



## 16. Register Summary and Descriptions

The sensor internal registers are accessible through SPI serial interface. The registers not listed in the table below and the registers which are marked as RSVD are NOT allowed to perform write operation in any case.

	-	
Register	Summary	
Register	Juining	

Address	Name	R/W	PWR On Default	Brief description
0x00	Product_ID1	R	0x30	Product Identifier [11:4]
0x01	Product_ID2	R	0x02	Upper 4 bits for Product Identifier, PID [3:0] Lower 4 bits for Product Version, VID [3:0]
0x02	Motion_Status	R	-	Motion Status information
0x03	Delta_X	R	-	Eight bits 2's complement number for X-axis motion data
0x04	Delta_Y	R	-	Eight bits 2's complement number for Y-axis motion data
0x05	Operation_Mode	R/W	0xB8	Operation mode selection
0x06	Configuration	R/W	0x11	Software power down and reset
0x09	Write_Protect	R/W	0x00	Write Protect to avoid mis-writing registers
0x0A	Sleep1	R/W	0x77	Sleep1 configuration
0x0B	Sleep2	R/W	0x10	Sleep2 configuration
0x0C	Sleep3	R/W	0x70	Sleep3 configuration
0x0D	CPI_X	R/W	0x1B	CPI setting for X axis
0x0E	CPI_Y	R/W	0x1B	CPI setting for Y axis
0x12	Delta_XY_Hi	R	-	Upper 4 bits of Delta_X and Delta_Y for 12-bit data format
0x13	IQC	R	-	Image Quality Complement
0x14	Shutter	R	-	Index of LED shutter time
0x17	Frame_Avg	R	-	Average brightness of a frame
0x19	Mouse_Option	R/W	0x00	Mouse orientation selection
0x26	SPI_Mode	R/W	0xB4	3-wired or 2-wired SPI interface



## **Detailed Register Descriptions**

Product_ID Access: Rea					ess: 0x00 It Value: 0x30			
Bit		6	5	4	3	2	1	0
Field	PID <sub>11</sub>	PID <sub>10</sub>	PID <sub>9</sub>	PID <sub>8</sub>	PID7	PID <sub>6</sub>	PID₅	PID <sub>4</sub>
			1103	1100		1100	1103	1104
Data Type:	Eight-bit num	ber.						
Usage:		d to check if the roduct Identifier[	communication c 11:4].	f the SPI link is	valid.		i (	2
Product_ID2	2			Addre	ess: 0x01			
Access: Rea					It Value: 0x02			
Bit	7	6	5	4	3	2	1	0
Field	PID <sub>3</sub>	PID <sub>2</sub>	PID <sub>1</sub>	PID <sub>0</sub>	VID <sub>3</sub>	VID <sub>2</sub>	VID <sub>1</sub>	VID <sub>0</sub>
Data Type: Usage:	Four-bit numb		communication of	f the SPI link is	valid.			
	Field Name	De	scription					
	PID [3:0]	Pro	duct Identifier[3:	0]				
	VID [3:0]	Pro	duct Version[3:0					
Motion_Stat	us		C	Addre	ess: 0x02			
Access: Rea	d Only			Defau	lt Value: NA			
Bit	7	6	5	4	3	2	1	0
Field	Motion	Reserved	Reserved	DYOVF	DXOVF	Reserved	Reserved	Reserved
Dete Tures	Ditfield							
	If the Motion bit	is set, the motion ading out Delta_	routine, the host n data in Delta_X X and Delta_Y re out.	and Delta_Y re	gisters are valid	and ready to be	read. Be sure t	o read Motion
	Typically in the r If the Motion bit bit first before re	is set, the motion ading out Delta_	n data in Delta_X X and Delta_Y re out.	and Delta_Y re	gisters are valid	and ready to be	read. Be sure t	o read Motior
	Typically in the r If the Motion bit bit first before re have overflowed	is set, the motion ading out Delta_ I since last read Descr	n data in Delta_X X and Delta_Y re out.	and Delta_Y re egisters. DXOVI	gisters are valid	and ready to be	read. Be sure t	o read Motion
	Typically in the r If the Motion bit bit first before re have overflowed	is set, the motion ading out Delta_ I since last read Descr Motion	n data in Delta_X X and Delta_Y re out.	and Delta_Y re egisters. DXOVI	gisters are valid	and ready to be	read. Be sure t	o read Motion
	Typically in the r If the Motion bit bit first before re have overflowed Field Name	is set, the motion ading out Delta_ I since last read Descr Motion 0 = No	n data in Delta_X X and Delta_Y re out. iption	and Delta_Y re egisters. DXOVI ast report	gisters are valid <sup>=</sup> bit and DYOVI	and ready to be bit show wheth	e read. Be sure t er if the motion	o read Motion report buffers
	Typically in the r If the Motion bit bit first before re have overflowed Field Name Motion	is set, the motion ading out Delta_ I since last read Descr Motion 0 = No 1 = Mo Delta_	a data in Delta_X X and Delta_Y re out. iption detected since la motion (Default) stion detected, da Y overflowed sin	and Delta_Y re egisters. DXOVI ast report ta in Delta_X and ce last read out	gisters are valid bit and DYOVI	and ready to be bit show wheth	e read. Be sure t er if the motion	o read Motior report buffers
	Typically in the r If the Motion bit bit first before re have overflowed Field Name	is set, the motion ading out Delta_ I since last read Descr Motion 0 = No 1 = Mo Delta_ 0 = No	a data in Delta_X X and Delta_Y re out. iption detected since la motion (Default) tion detected, da Y overflowed sin- overflow (Defau	and Delta_Y re egisters. DXOVI ast report ta in Delta_X and ce last read out	gisters are valid bit and DYOVI	and ready to be bit show wheth	e read. Be sure t er if the motion	o read Motior report buffers
Data Type: Usage:	Typically in the r If the Motion bit bit first before re have overflowed Field Name Motion	is set, the motion ading out Delta_ I since last read Descr Motion 0 = No 1 = Mo Delta_ 0 = No 1 = Ov	a data in Delta_X X and Delta_Y re out. iption detected since k motion (Default) tion detected, da Y overflowed sin- overflow (Defau erflow occurred	and Delta_Y re egisters. DXOVI ast report ta in Delta_X and ce last read out lt)	gisters are valid bit and DYOVI nd Delta_Y regis	and ready to be bit show wheth	e read. Be sure t er if the motion	o read Motior report buffers
	Typically in the r If the Motion bit bit first before re have overflowed Field Name Motion DYOVF	is set, the motion ading out Delta_ I since last read Descr Motion 0 = No 1 = Mo Delta_ 0 = No 1 = Ov Delta_	a data in Delta_X X and Delta_Y re out. iption detected since la motion (Default) tion detected, da Y overflowed sin- overflow (Defau erflow occurred X overflowed sin-	and Delta_Y re egisters. DXOVI ast report ta in Delta_X and ce last read out lt) ce last read out	gisters are valid bit and DYOVI nd Delta_Y regis	and ready to be bit show wheth	e read. Be sure t er if the motion	o read Motior report buffers
	Typically in the r If the Motion bit bit first before re have overflowed Field Name Motion	is set, the motion ading out Delta_ l since last read Descr Motion 0 = No 1 = Mo Delta_ 0 = No 1 = Ov Delta_ 0 = No 0 = No	a data in Delta_X X and Delta_Y re out. iption detected since k motion (Default) tion detected, da Y overflowed sin- overflow (Defau erflow occurred	and Delta_Y re egisters. DXOVI ast report ta in Delta_X and ce last read out lt) ce last read out	gisters are valid bit and DYOVI nd Delta_Y regis	and ready to be bit show wheth	e read. Be sure t er if the motion	o read Motior report buffers

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Delta_X	Delta_X Address: 0x03									
Access: Read	Read Only Default Value: NA									
Bit	7	6 5 4 3 2 1 0								
Field	Field         X7         X6         X5         X4         X3         X2         X1         X0									

Data Type: Eight-bit 2's complement number.

Usage: Delta\_X register is the X-axis motion in counts after reading Motion\_Status register. Absolute value is determined by the resolution setting CPI\_X. Reading this register clears the content of this register. Report range -128 ~ +127. The MSB bit represents the sign bit.

Delta_Y	Delta_Y Address: 0x04							
Access: Read	Only		Default Value: NA					
Bit	7	6	5	4	2	1	0	
Field	Field         Y7         Y6         Y5         Y4         Y3						<b>Y</b> 1	<b>Y</b> <sub>0</sub>

Data Type: Eight-bit 2's complement number.

Usage: Delta\_Y register is the Y-axis motion in counts after reading Motion\_Status register. Absolute value is determined by resolution setting CPI\_Y. Reading this register clears the content of this register. Report range –128 ~ +127. The MSB bit represents the sign bit.



Dperation_					ess: 0x05						
Access: Rea					It Value: 0xB8						
Bit	7	6	5	4	3	2	1	0			
Field	Reserved	Reserved	Reserved	Slp_Enh	Slp2_Enh	Slp1mu_Enh	Slp1mu_Enh	Wakeup			
Data Type:	Bit field.										
Usage:	Operation_Mode below.	register allows	users to change	the sensor ope	eration modes.	The various com	binations of bit4~	bit0 are liste			
	"0xxxx" = Sleep1 and Sleep2 mode are all disabled "10xxx" = Sleep1 mode is enabled but Sleep2 mode is disable "11xxx" = Sleep1 and Sleep2 modes are all enabled "11100" = Force sensor to enter Sleep2 mode "1x010" = Force sensor to enter Sleep1 mode										
	For Slp2mu_Enh reset automatical simultaneously.	•	•	•							
	Field Name	Descri									
	Enable/Disable Sleep mode (including Sleep1 and Sleep2)         Slp_Enh       0 = Disable         1 = Enable (Default)										
	Enable/Disable Sleep2 mode       Slp2_Enh       0 = Disable       1 = Enable (Default)										
	Slp2mu_Enh         Force to enter Sleep2 mode.           Structure         Set "1" to enter Sleep2, and then it will be reset to "0" automatically										
	Slp1mu_Enh		o enter Sleep1 r to enter Sleep1,		be reset to "0" a	automatically					
	Wakeup Sensor from Sleep mode. Set "1" to wake up and then it will be reset to "0" automatically										
	+										



Configurati	on			Addre	ess: 0x06							
Access: Rea	ess: Read/Write Default Value: 0x11           Bit         7         6         5         4         3         2         1         0           Sidd         Descrived         Descrived											
Bit	7	6	5	4	3	2	1	0				
Field	Reset	Reserved	Slp3_Enh	Reserved	PD_Enh	Reserved	Reserved	Reserved				
Data Type:	Bit field.						•					
Usage:	Configuration re	gister allows use	rs to change the	configuration of	the sensor.							
	Field Name Description											
	Full chip reset. This bit will be de-asserted automatically.											
	Reset 0 = Normal operation mode (Default)											
		1 = Ful	I chip reset (to re	eset all the sens	or's internal regi	sters and states	;)					
		Enable	/Disable Sleep3	mode								
	Slp3_Enh	0 = Dis	able (Default)									
		1 = Ena	able									
		Power	down mode for I	owest power co	nsumption							
	PD_Enh	0 = No	rmal operation (I	Default)								
		1 = Pov	wer down mode	(but retain the s	ensor register se	ettings)						
						5						

Write_Protect				Addr	Address: 0x09					
Access: Read/Write Default Value: 0x00										
Bit	7	6	5 4 3 2 1							
Field	WP7	WP <sub>6</sub>	WP <sub>5</sub>	WP <sub>4</sub>	WP <sub>3</sub>	WP <sub>2</sub>	WP <sub>1</sub>	WP <sub>0</sub>		

Data Type: Eight-bit number.

Write Protect register is used to avoid host controller mis-writing the registers after address 0x09. Usage: 0x00 = Enable (Default), registers after address 0x09 are read only 0x5A = Disable, registers after address 0x09 can be read/write

Sleep1			Address: 0x0A					
Access: Read	Access: Read/Write Default Value: 0x77							
Bit	7	6	5	4	3	2	1	0
Field	Slp1_Freq₃	Slp1_Freq <sub>2</sub>	Slp1_Freq₁	Slp1_Freq₀	Slp1_Etm₃	Slp1_Etm <sub>2</sub>	Slp1_Etm <sub>1</sub>	Slp1_Etm₀

Data Type: Four-bit number.

Sleep1 register allows users to set the sampling frequency time during Sleep1 mode and the entering time from Run mode to Usage: Sleep1 mode.

Field Name	Description
Slp1_Freq[3:0]	Each step is equivalent to 4ms. Relative to its value 0 ~ 15, the sampling frequency time is 4ms ~ 64ms. Default Slp1_Freq[3:0] =7 (32ms)
Slp1_Etm[3:0]	Each step is equivalent to 32ms. Relative to its value $0 \sim 15$ , the entering time is 32ms $\sim 512$ ms. Default Slp1_Etm[3:0] = 7 (256ms)

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Sleep2				Addro	ss: 0x0B			
Access: Rea	ad/Write				t Value: 0x10			
Bit	7	6	5	4	3	2	1	0
Field	Slp2_Freq <sub>3</sub>	Slp2_Freq2	Slp2_Freq1	Slp2_Freq₀	Slp2_Etm₃	Slp2_Etm <sub>2</sub>	Slp2_Etm1	Slp2_Etm₀
Data Type:	Four-bit numbe	er.						
Usage:	Sleep2 register a Sleep2 mode.	llows users to s	et the sampling	frequency time	during Sleep2 n	node and the er	ntering time from	n Run mode to
	Field Name	Descri	otion					
	Slp2_Freq[3:0]			quivalent to 64r It Slp2_Freq[3:0	ns. Relative to it ] = 1 (128ms)	ts value 0 ~ 15,	the sampling fr	equency time i
	Slp2_Etm[3:0]			nt to 20.48sec. 2_Etm[3:0] = 0 (;	Relative to its v 20.48sec)	alue 0 ~ 15, th	e entering time	is 20.48sec ~
Sleep3				Addre	ss: 0x0C			
Access: Rea	ad/Write			Defaul	t Value: 0x70			
Bit	7	6	5	4	3	2	1	0
Field	Slp3_Freq₃	Slp3_Freq <sub>2</sub>	Slp3_Freq₁	Slp3_Freq₀	Slp3_Etm₃	Slp3_Etm <sub>2</sub>	Slp3_Etm₁	Slp3_Etm₀
Data Type:	Four-bit numbe	er.						
Usage:	Sleep3 register a Sleep3 mode.		et the sampling	frequency time	during Sleep3 n	node and the er	ntering time from	n Run mode to
Usage:			C	frequency time	during Sleep3 n	node and the er	ntering time from	Run mode to
Usage:	Sleep3 mode.	llows users to s Descri Each s	otion tep is equivalen	t to 64ms. Rela	tive to its value			
Usage:	Sleep3 mode. Field Name	llows users to s Descri Each s 1024ms Each s	otion tep is equivalen s. Default Slp3_ ep change is ec	t to 64ms. Rela Freq[3:0] = 7 (51 juivalent to 20.4	tive to its value 2ms) 8sec. Relative to	0 ~ 15, the san	npling frequency	time is 64ms -
Usage:	Sleep3 mode. Field Name Slp3_Freq[3:0]	llows users to s Descri Each s 1024ms Each s	otion tep is equivalen s. Default Slp3_ ep change is ec	t to 64ms. Rela Freq[3:0] = 7 (51	tive to its value 2ms) 8sec. Relative to	0 ~ 15, the san	npling frequency	<sup>7</sup> time is 64ms <sup>2</sup>
	Sleep3 mode. Field Name Slp3_Freq[3:0]	llows users to s Descri Each s 1024ms Each s	otion tep is equivalen s. Default Slp3_ ep change is ec	t to 64ms. Rela Freq[3:0] = 7 (51 juivalent to 20.4 lp3_Etm[3:0] = 0	tive to its value 2ms) 8sec. Relative to	0 ~ 15, the san	npling frequency	<sup>7</sup> time is 64ms <sup>7</sup>
CPI_X	Sleep3 mode. Field Name Slp3_Freq[3:0] Slp3_Etm[3:0]	llows users to s Descri Each s 1024ms Each s	otion tep is equivalen s. Default Slp3_ ep change is ec	t to 64ms. Rela Freq[3:0] = 7 (51 juivalent to 20.4 lp3_Etm[3:0] = 0 Addre	tive to its value 2ms) 8sec. Relative to (20.48sec)	0 ~ 15, the san	npling frequency	time is 64ms
Usage: CPI_X Access: Rea Bit Field	Sleep3 mode. Field Name Slp3_Freq[3:0] Slp3_Etm[3:0]	llows users to s Descri Each s 1024ms Each s	otion tep is equivalen s. Default Slp3_ ep change is ec	t to 64ms. Rela Freq[3:0] = 7 (51 juivalent to 20.4 lp3_Etm[3:0] = 0 Addre	tive to its value 2ms) 8sec. Relative to (20.48sec) ss: 0x0D	0 ~ 15, the san	npling frequency	time is 64ms -

Data Type: Six-bit number.

Usage: This register is the CPI resolution of sensor for X axis. Each step is equivalent to 38 counts based on x1 lens magnification. Default value is 27 (CPI = 1026). Target CPI = 38 \* CPI\_X. Recommended range : 16 ~ 63 (CPI = 608 ~ 2394)



CPI_Y				Addre	ess: 0x0E			
Access: Read/Write Default Value: 0x1B								
Bit	7	6	5	4	3	2	1	0
Field Reserved Reserved CPI_Y5 CP					CPI_Y <sub>3</sub>	CPI_Y <sub>2</sub>	CPI_Y <sub>1</sub>	CPI_Y <sub>0</sub>

Data Type: Six-bit number.

Usage: This register is the CPI resolution of sensor for Y axis. Each step is equivalent to 38 counts based on x1 lens magnification. Default value is 27 (CPI = 1026). Target CPI = 38 \* CPI\_Y. Recommended range : 16 ~ 63 (CPI = 608 ~ 2394).

Delta_XY_Hi				Addre	ess: 0x12		XIV		
Access: Read	Only	Default Value: NA							
Bit	Bit 7 6 5 4 3					2	1	0	
Field         X11         X10         X9         X8         Y11						<b>Y</b> <sub>10</sub>	Y9	Y <sub>8</sub>	

Data Type: Four-bit number.

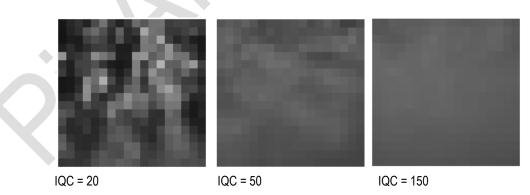
The upper 4 bits of Delta\_X[11:0] and Delta\_Y[11:0] for 12-bit data format. Usage:

Field Name	Description
X[11:8]	the upper 4 bits of Delta_X[11:0] for 12-bit data format
Y[11:8]	the upper 4 bits of Delta_Y[11:0] for 12-bit data format

IQC		Address: 0x13						
Access: Read Only Default Value: NA								
Bit	7	6	5	4	3	2	1	0
Field	IQC7	IQC <sub>6</sub>	IQC <sub>5</sub>	IQC <sub>4</sub>	IQC <sub>3</sub>	IQC <sub>2</sub>	IQC <sub>1</sub>	IQC <sub>0</sub>

Data Type: Eight-bit number.

Usage: IQC means Image Quality Compliment. This register represents the fuzziness of a surface viewed by the sensor. The smaller the index is, the easier for the sensor to have a good tracking on the surface. IQC ranges from 0 ~ 255.



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Shutter	Address: 0x14								
Access: Rea	Access: Read Only Default Value: NA								
Bit	7	6	5	4	3	2	1	0	
Field	Reserved	Reserved	Reserved	Shutter <sub>4</sub>	Shutter <sub>3</sub>	Shutter <sub>2</sub>	Shutter <sub>1</sub>	Shutter <sub>0</sub>	
Data Type: Usage:									
Frame_Avg				Addre	ess: 0x17		X	0	

Access: Read Only					Defaul	t value: NA			
Γ	Bit	7	6	5	4	3	2	1	0
	Field	FA <sub>7</sub>	FA <sub>6</sub>	FA <sub>5</sub>	FA <sub>4</sub>	FA <sub>3</sub>	FA <sub>2</sub>	FA <sub>1</sub>	FA <sub>0</sub>

Data Type: Eight-bit number.

Usage: Frame\_Avg register represent s the average brightness of all pixels within a frame (324 pixels). This value ranges from 0 to 255.

Mouse_Option Address: 0x19								
Access: Read/Write Default Value: 0x00								
Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Movxy_SW	Movy_Inv	Movx_Inv	XY12bit_Enh	Reserved	Reserved

Data Type: Bit field.

# Usage: To select the mouse X/Y direction and Delta\_X, Delta\_Y motion data length (8-bit or 12-bit).

LB	RB	LB	RB	LB	RB	LB	RB
					वितवन		
0x19[5:	:3] = 0	0x19[5	5:3] = 6	0x19	[5:3] = 5	0x19	9[5:3] = 3

Field Name	Description	
Movxy_Sw	To swap the XY direction. Default is 0.	
Movy_Inv	To invert the Y direction. Default is 0.	
Movx_Inv	To invert the X direction. Default is 0.	
XY12bit_Enh	To select 8-bit or 12-bit motion data length. Default is 0 (8-bit mode)	

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SPI_Mode Address: 0x26								
Access: Read/Write Default					t Value: 0xB4			
Bit	7	6	5	4	3	2	1	0
Field	SPI_Sel	Reserved	Pin1_Sel₁	Pin1_Sel₀	Reserved	Reserved	Reserved	Reserved

Data Type: One-bit and Two-bit numbers.

Usage: To select 3-wired or 2-wired SPI interface, and to select the Pin1 function when the 2-wired SPI mode has been chosen.

Field Name	Description	
	To select 3-wired or 2-wired SPI interface.	
SPI_Sel	0 = 2-wired SPI mode.	
	1 = 3-wired SPI mode (default).	
	To select Pin1 function when SPI is in 2-wired SPI mo	de
	0 = Hardware Reset function.	
Pin1_Sel[1:0]	1 = Quick Burst (QB) function.	
	2 = Hardware Power-Down function.	
	3 = No function (default).	



## 17. Sensor Registers Initialization Sequence

- High Voltage Segment with 3-wired SPI
   No sensor settings are required
- High Voltage Segment and 2-wired SPI
   Write address 0x09 = 0x5A; to disable Write Protect
   Write address 0x26 = 0x34; to switch to 2-wired SPI
   Write address 0x09 = 0x00; to enable Write Protect
- Low Voltage Segment with 3-wired SPI Write address 0x09 = 0x5A; to disable Write Protect Write address 0x4B = 0x04; to turn off internal regulator for Low Voltage Segment Write address 0x09 = 0x00; to enable Write Protect
- Low Voltage Segment with 2-wired SPI Write address 0x09 = 0x5A; to disable Write Protect
   Write address 0x26 = 0x34; to switch to 2-wired SPI
   Write address 0x4B = 0x04; to turn off internal regulator for Low Voltage Segment
   Write address 0x09 = 0x00; to enable Write Protect



# 18. Revision History

Revision No.	Date	Notes
R1.0	22.07.2014	New creation
R1.1	15.08.2014	<ol> <li>Added chapter 10 to introduce the Pin1 Function in 2-wired SPI Mode, including Quick Burst read function</li> <li>Added register SPI_Mode (address 0x26) in register table</li> <li>Added t<sub>QB</sub> specification in AC Operation Conditions table</li> </ol>
R1.2	19.11.2014	Added "NCS Low at Power-up Stage" section in chapter 8.