

PC3H2/PC3Q62

High Resistance to Noise, Half Pitch Photocoupler

■ Features

- Half pitch surface mount type for high density mounting
(Lead pitch : 1.27 mm)
- High resistance to noise due to high common mode rejection voltage (CMR : MIN.10kV/ μ s)
- Soldering reflow type (230°C, for 30seconds)
- High temperature tested model
- Taping package
 - PC3H2** (1ch)
 - PC3Q62** (4ch)
- Recognized by UL, file No. E64380

■ Applications

- Programmable controllers

■ Package Specifications

Model No.	Package specification
PC3H2	Taping reel diameter 330mm (3 000pcs)
PC3Q62	Taping reel diameter 330mm (1 000pcs)

■ Absolute Maximum Ratings (Ta=25°C)

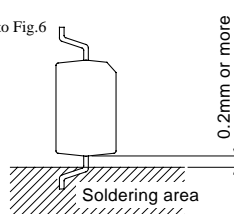
	Parameter	Symbol	Rating	Unit
Input	*1 Forward current	I_F	50	mA
	*2 Peak forward current	I_{FM}	1	A
	Reverse voltage	V_R	6	V
Output	*1 Power dissipation	P	70	mW
	*1 Collector-emitter voltage	V_{CEO}	70	V
	Emitter-collector voltage	V_{ECO}	6	V
	Collector current	I_C	50	mA
	*1 Collector dissipation	P_C	150	mW
	*1 Total power dissipation	P_{tot}	170	mW
	Operating temperature	T_{opr}	-30 to +100	°C
	Tstg Storage temperature	T_{stg}	-40 to +125	°C
*3 Viso Isolation voltage	V_{iso}	2.5	kV _{rms}	
*4 Soldering temperature	T_{SOL}	260	°C	

*1 The derating factors of absolute maximum ratings due to ambient temperature are shown in Fig.2 to 5

*2 Pulse width \leq 100 μ s, Duty ratio:0.01, Refer to Fig.6

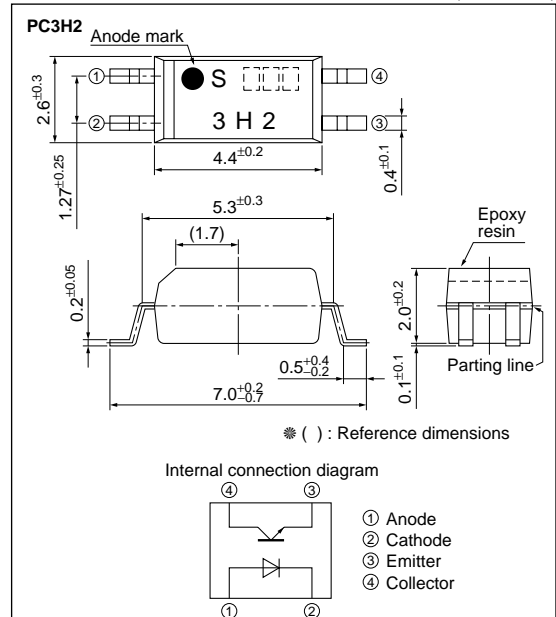
*3 AC for 1min., 40 to 60% RH, f=60Hz

*4 For 10s

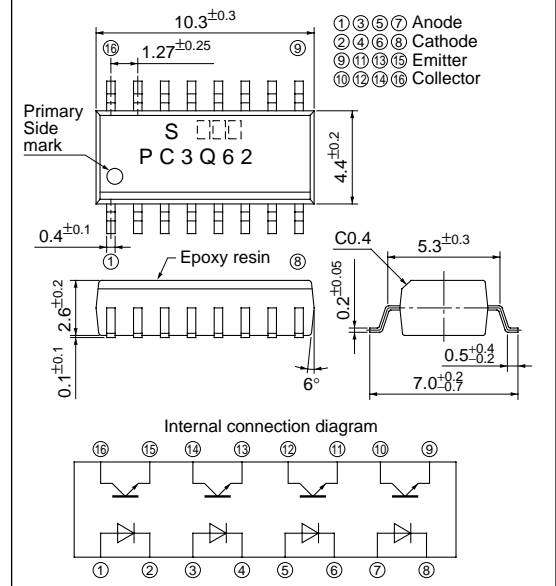


■ Outline Dimensions

(Unit : mm)



PC3Q62



■ Electro-optical Characteristics

(Ta=25°C)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit								
Input	Forward voltage	V_F	$I_F=20\text{mA}$	-	1.2	1.4	V								
	Reverse current	I_R	$V_R=4\text{V}$	-	-	10	μA								
	Terminal capacitance	C_t	$V=0, f=1\text{kHz}$	-	30	250	pF								
Output	Collector dark current	<table border="1"> <tr> <td>PC3H2</td> <td rowspan="2">I_{CEO}</td> <td>$V_{CE}=50\text{V}, I_F=0$</td> <td rowspan="2">-</td> <td rowspan="2">-</td> <td rowspan="2">100</td> <td rowspan="2">nA</td> </tr> <tr> <td>PC3Q62</td> <td>$V_{CE}=20\text{V}, I_F=0$</td> </tr> </table>	PC3H2	I_{CEO}	$V_{CE}=50\text{V}, I_F=0$	-	-	100	nA	PC3Q62	$V_{CE}=20\text{V}, I_F=0$				
			PC3H2		I_{CEO}					$V_{CE}=50\text{V}, I_F=0$	-	-	100	nA	
	PC3Q62	$V_{CE}=20\text{V}, I_F=0$													
Collector-emitter breakdown voltage	BV_{CEO}	$I_C=0.1\text{mA}$ $I_F=0$	70	-	-	V									
	Emitter-collector breakdown voltage	BV_{ECO}	$I_E=10\mu\text{A}, I_F=0$	6	-	-	V								
Transfer characteristics	Collector current	I_C	$I_F=1\text{mA}$ $V_{CE}=5\text{V}$	0.2	-	4.0	mA								
	Collector-emitter saturation voltage	$V_{CE(sat)}$	$I_F=20\text{mA}$ $I_C=1\text{mA}$	-	0.1	0.2	V								
	Isolation resistance	R_{ISO}	DC500V 40 to 60%RH	5×10^{10}	1×10^{11}	-	Ω								
	Floating capacitance	C_f	$V=0, f=1\text{MHz}$	-	0.6	1.0	pF								
	Response time	Rise time	t_r	$V_{CE}=2\text{V}$ $I_C=2\text{mA}$ $R_L=100\Omega$	-	4	18	μs							
		Fall time	t_f		-	3	18	μs							
*5 Common mode rejection voltage		CMR	Ta=25°C, $R_L=470\Omega$ $V_{CM}=1.5\text{kV(peak)}$ $I_F=0\text{mA}, V_{CC}=9\text{V}$, $V_{np}=100\text{mV}$	10	-	-	kV/ μs								

*5 Refer to Fig.1

Fig.1 Test Circuit for Common Mode Rejection Voltage

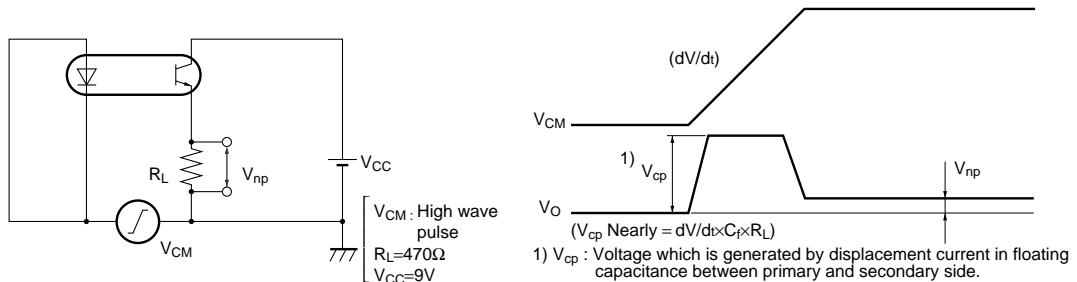


Fig.2 Forward Current vs. Ambient Temperature

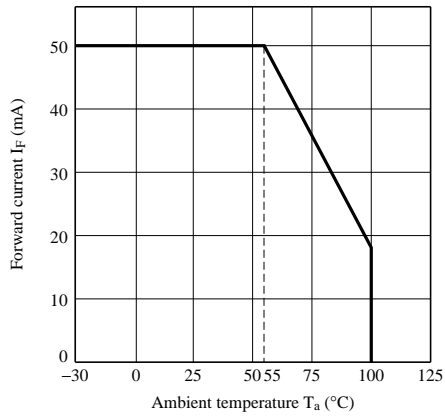


Fig.3 Diode Power Dissipation vs. Ambient Temperature

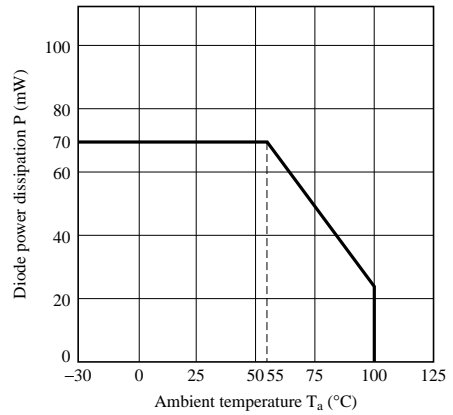


Fig.4 Collector Power Dissipation vs. Ambient Temperature

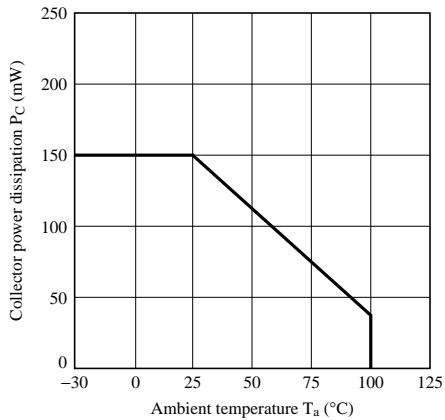


Fig.5 Total Power Dissipation vs. Ambient Temperature

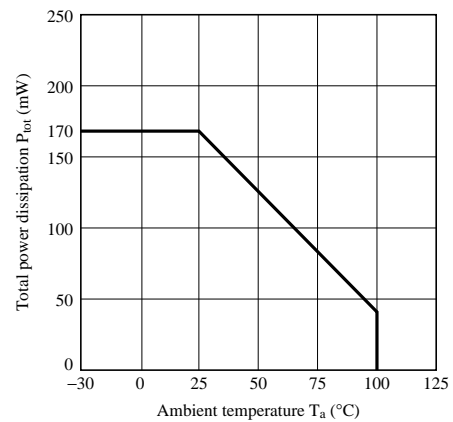


Fig.6 Peak Forward Current vs. Duty Ratio

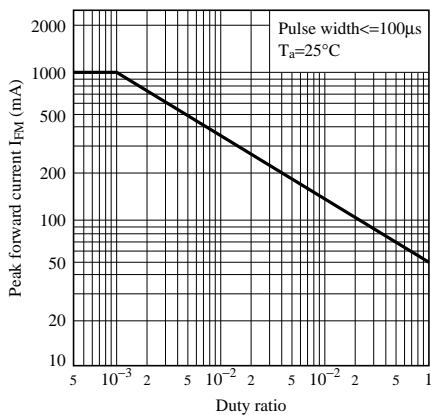


Fig.7 Forward Current vs. Forward Voltage

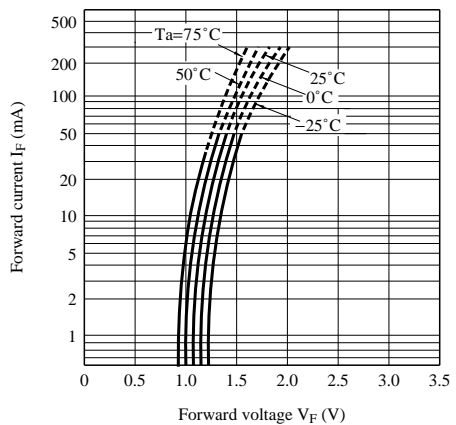


Fig.8 Current Transfer Ratio vs. Forward Current

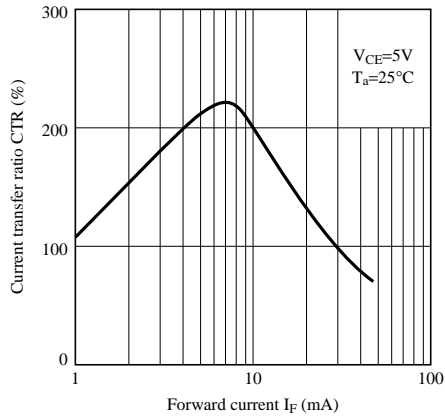


Fig.9 Collector Current vs. Collector-emitter Voltage

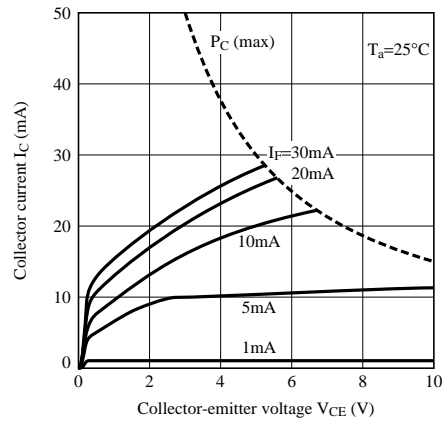


Fig.10 Relative Current Transfer Ratio vs. Ambient Temperature

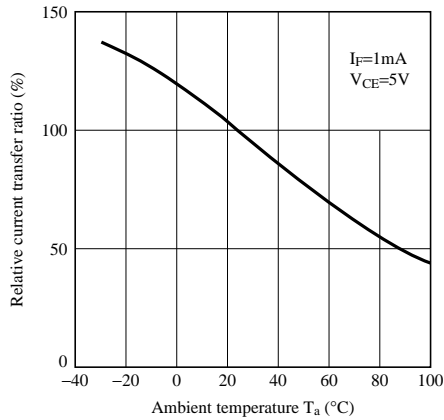


Fig.11 Collector-emitter Saturation Voltage vs. Ambient Temperature

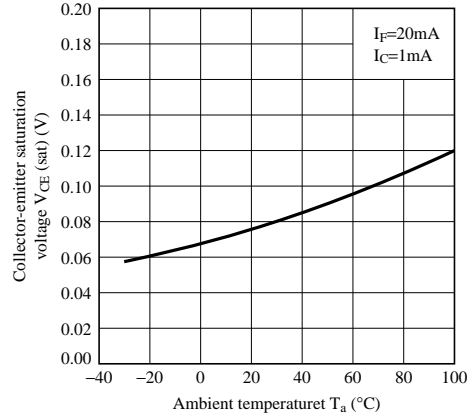


Fig.12 Collector Dark Current vs. Ambient Temperature

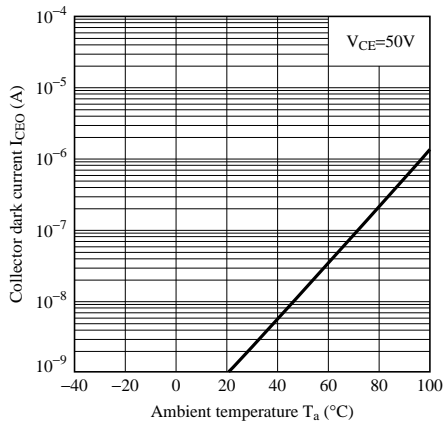


Fig.13 Response Time vs. Load Resistance

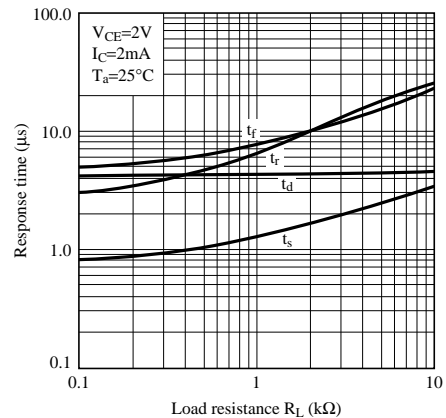


Fig.14 Test Circuit for Response Time

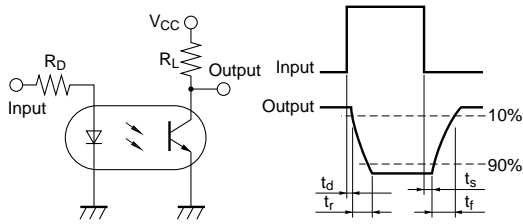


Fig.15 Voltage Gain vs Frequency

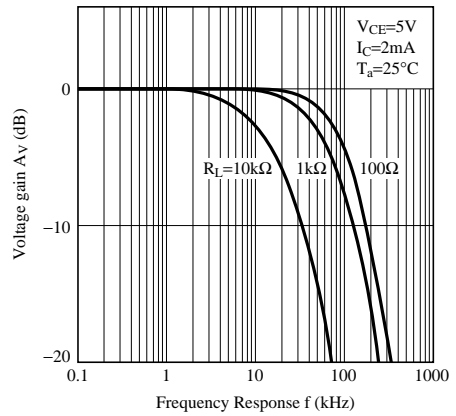


Fig.16 Collector-emitter Saturation Voltage vs. Forward Current

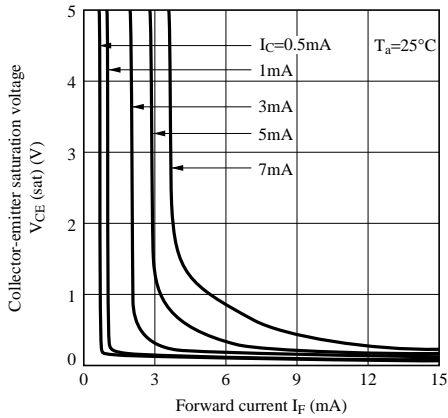
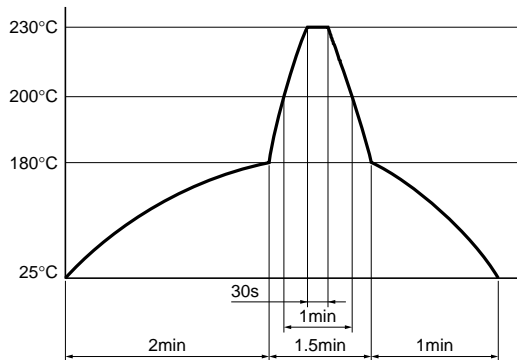


Fig.17 Reflow Soldering

Only one time soldering is recommended within the temperature profile shown below.



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