



# PCA9555A

Low-voltage 16-bit I<sup>2</sup>C-bus I/O port with interrupt and weak pull-up

Rev. 1 — 11 September 2012

Product data sheet

## 1. General description

---

The PCA9555A is a low-voltage 16-bit General Purpose Input/Output (GPIO) expander with interrupt and weak pull-up resistors for I<sup>2</sup>C-bus/SMBus applications. NXP I/O expanders provide a simple solution when additional I/Os are needed while keeping interconnections to a minimum, for example, in ACPI power switches, sensors, push buttons, LEDs, fan control, etc.

In addition to providing a flexible set of GPIOs, the wide V<sub>DD</sub> range of 1.65 V to 5.5 V allows the PCA9555A to interface with next-generation microprocessors and microcontrollers where supply levels are dropping down to conserve power.

The PCA9555A contains the PCA9555 register set of four pairs of 8-bit Configuration, Input, Output, and Polarity Inversion registers.

The PCA9555A is a pin-to-pin replacement to the PCA9555 and other industry-standard devices. A more fully featured device, the PCAL9555A, is available with Agile I/O features. See the respective data sheet for more details.

The PCA9555A open-drain interrupt ( $\overline{\text{INT}}$ ) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed.

$\overline{\text{INT}}$  can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I<sup>2</sup>C-bus. Thus, the PCA9555A can remain a simple slave device.

The device outputs have 25 mA sink capabilities for directly driving LEDs while consuming low device current.

The power-on reset sets the registers to their default values and initializes the device state machine.

All input/output pins have weak pull-up resistors connected to them to eliminate external components.

Three hardware pins (A0, A1, A2) select the fixed I<sup>2</sup>C-bus address and allow up to eight devices to share the same I<sup>2</sup>C-bus/SMBus.



## 2. Features and benefits

- I<sup>2</sup>C-bus to parallel port expander
- Operating power supply voltage range of 1.65 V to 5.5 V
- Low standby current consumption:
  - ◆ 1.5  $\mu$ A (typical at 5 V  $V_{DD}$ )
  - ◆ 1.0  $\mu$ A (typical at 3.3 V  $V_{DD}$ )
- Schmitt-trigger action allows slow input transition and better switching noise immunity at the SCL and SDA inputs
  - ◆  $V_{hys} = 0.10 \times V_{DD}$  (typical)
- 5 V tolerant I/Os
- Open-drain active LOW interrupt output ( $\overline{INT}$ )
- 400 kHz Fast-mode I<sup>2</sup>C-bus
- Internal power-on reset
- Power-up with all channels configured as inputs with weak pull-up resistors
- No glitch on power-up
- Latched outputs with 25 mA drive maximum capability for directly driving LEDs
- Latch-up performance exceeds 100 mA per JESD78, Class II
- ESD protection exceeds JESD22
  - ◆ 2000 V Human Body Model (A114-A)
  - ◆ 1000 V Charged-Device Model (C101)
- Packages offered: TSSOP24, HWQFN24

## 3. Ordering information

Table 1. Ordering information

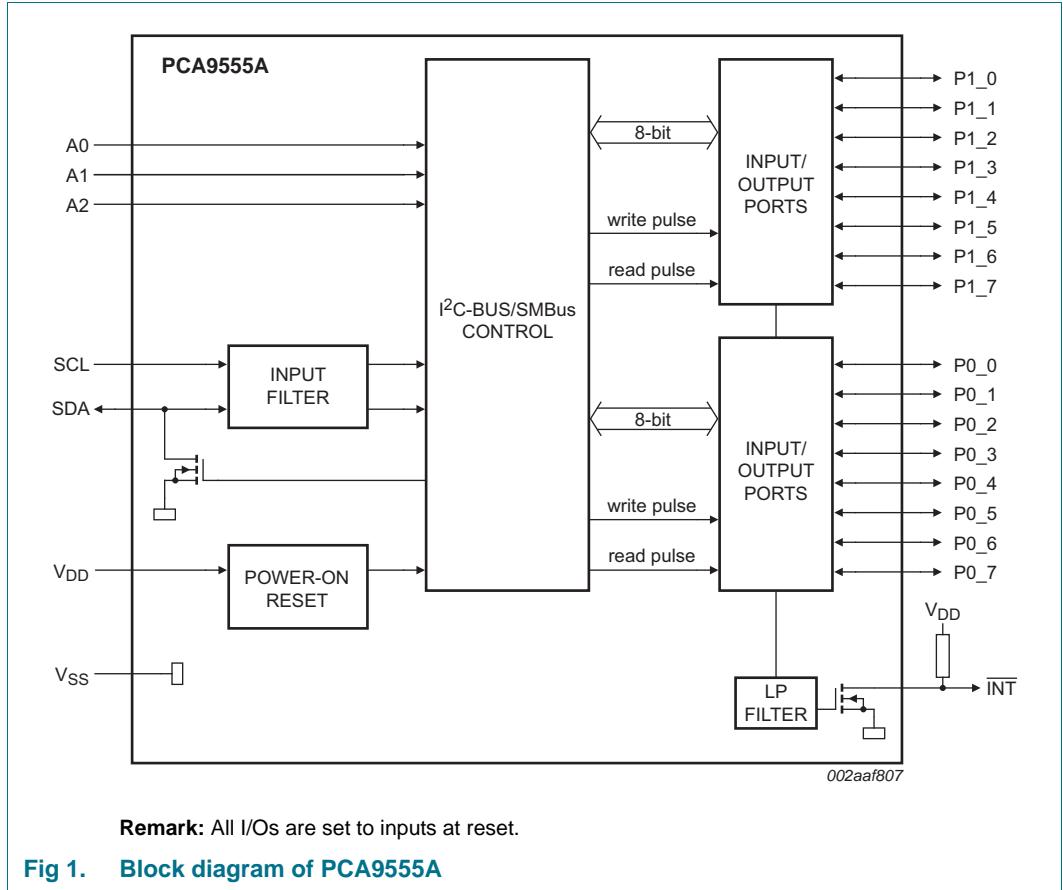
| Type number | Package |   |          |
|-------------|---------|---|----------|
|             | Name    | Description   | Version  |
| PCA9555APW  | TSSOP24 | plastic thin shrink small outline package; 24 leads; body width 4.4 mm                                  | SOT355-1 |
| PCA9555AHF  | HWQFN24 | plastic thermal enhanced very very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.75 mm | SOT994-1 |

### 3.1 Ordering options

Table 2. Ordering options

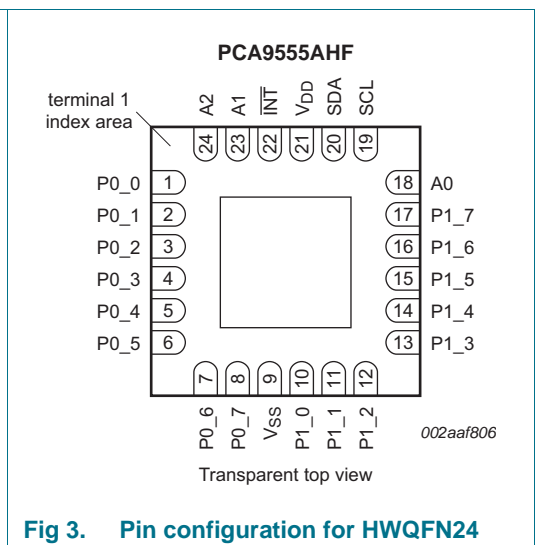
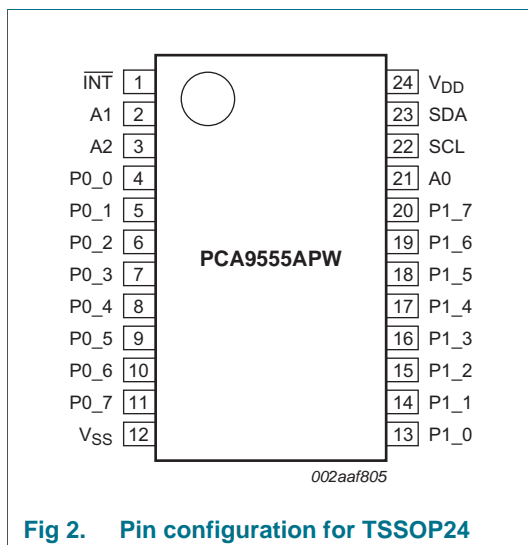
| Type number | Topside mark | Temperature range |
|-------------|--------------|-------------------|
| PCA9555APW  | PCA9555A     | -40 °C to +85 °C  |
| PCA9555AHF  | 555A         | -40 °C to +85 °C  |

### 4. Block diagram



### 5. Pinning information

#### 5.1 Pinning



## 5.2 Pin description

Table 3. Pin description

| Symbol                  | Pin     |                  | Type  | Description   |
|-------------------------|---------|------------------|-------|---|
|                         | TSSOP24 | HWQFN24          |       |   |
| $\overline{\text{INT}}$ | 1       | 22               | O     | Interrupt output. Connect to $V_{\text{DD}}$ through a pull-up resistor.  |
| A1                      | 2       | 23               | I     | Address input 1. Connect directly to $V_{\text{DD}}$ or $V_{\text{SS}}$ . |
| A2                      | 3       | 24               | I     | Address input 2. Connect directly to $V_{\text{DD}}$ or $V_{\text{SS}}$ . |
| P0_0 <sup>[2]</sup>     | 4       | 1                | I/O   | Port 0 input/output 0.  |
| P0_1 <sup>[2]</sup>     | 5       | 2                | I/O   | Port 0 input/output 1.  |
| P0_2 <sup>[2]</sup>     | 6       | 3                | I/O   | Port 0 input/output 2.  |
| P0_3 <sup>[2]</sup>     | 7       | 4                | I/O   | Port 0 input/output 3.  |
| P0_4 <sup>[2]</sup>     | 8       | 5                | I/O   | Port 0 input/output 4.  |
| P0_5 <sup>[2]</sup>     | 9       | 6                | I/O   | Port 0 input/output 5.  |
| P0_6 <sup>[2]</sup>     | 10      | 7                | I/O   | Port 0 input/output 6.  |
| P0_7 <sup>[2]</sup>     | 11      | 8                | I/O   | Port 0 input/output 7.  |
| $V_{\text{SS}}$         | 12      | 9 <sup>[1]</sup> | power | Ground.   |
| P1_0 <sup>[3]</sup>     | 13      | 10               | I/O   | Port 1 input/output 0.  |
| P1_1 <sup>[3]</sup>     | 14      | 11               | I/O   | Port 1 input/output 1.  |
| P1_2 <sup>[3]</sup>     | 15      | 12               | I/O   | Port 1 input/output 2.  |
| P1_3 <sup>[3]</sup>     | 16      | 13               | I/O   | Port 1 input/output 3.  |
| P1_4 <sup>[3]</sup>     | 17      | 14               | I/O   | Port 1 input/output 4.  |
| P1_5 <sup>[3]</sup>     | 18      | 15               | I/O   | Port 1 input/output 5.  |
| P1_6 <sup>[3]</sup>     | 19      | 16               | I/O   | Port 1 input/output 6.  |
| P1_7 <sup>[3]</sup>     | 20      | 17               | I/O   | Port 1 input/output 7.  |
| A0                      | 21      | 18               | I     | Address input 0. Connect directly to $V_{\text{DD}}$ or $V_{\text{SS}}$ . |
| SCL                     | 22      | 19               | I     | Serial clock bus. Connect to $V_{\text{DD}}$ through a pull-up resistor.  |
| SDA                     | 23      | 20               | I/O   | Serial data bus. Connect to $V_{\text{DD}}$ through a pull-up resistor.   |
| $V_{\text{DD}}$         | 24      | 21               | power | Supply voltage.   |

[1] HWQFN24 package die supply ground is connected to both  $V_{\text{SS}}$  pin and exposed center pad.  $V_{\text{SS}}$  pin must be connected to supply ground for proper device operation. For enhanced thermal, electrical, and board level performance, the exposed pad needs to be soldered to the board using a corresponding thermal pad on the board and for proper heat conduction through the board, thermal vias need to be incorporated in the PCB in the thermal pad region.

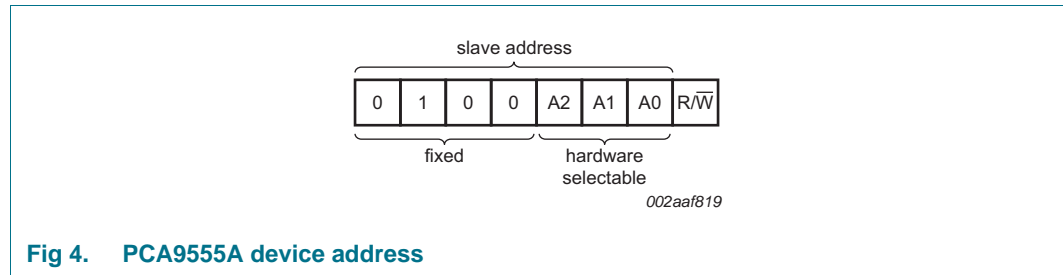
[2] Pins P0\_0 to P0\_7 correspond to bits P0.0 to P0.7. At power-up, all I/O are configured as high-impedance inputs.

[3] Pins P1\_0 to P1\_7 correspond to bits P1.0 to P1.7. At power-up, all I/O are configured as high-impedance inputs.

## 6. Functional description

Refer to [Figure 1 “Block diagram of PCA9555A”](#).

### 6.1 Device address



A2, A1 and A0 are the hardware address package pins and are held to either HIGH (logic 1) or LOW (logic 0) to assign one of the eight possible slave addresses. The last bit of the slave address (R/W) defines the operation (read or write) to be performed. A HIGH (logic 1) selects a read operation, while a LOW (logic 0) selects a write operation.

### 6.2 Registers

#### 6.2.1 Pointer register and command byte

Following the successful acknowledgement of the address byte, the bus master sends a command byte, which is stored in the Pointer register in the PCA9555A. The lower three bits of this data byte state the operation (read or write) and the internal registers (Input, Output, Polarity Inversion, or Configuration) that will be affected. This register is write only.

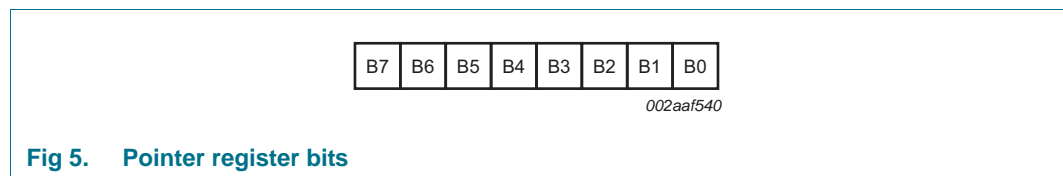


Table 4. Command byte

| Pointer register bits |    |    |    |    |    |    |    | Command byte<br>(hexadecimal) | Register                  | Protocol        | Power-up<br>default      |
|-----------------------|----|----|----|----|----|----|----|-------------------------------|---------------------------|-----------------|--------------------------|
| B7                    | B6 | B5 | B4 | B3 | B2 | B1 | B0 |                               |                           |                 |                          |
| 0                     | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 00h                           | Input port 0              | read byte       | xxxx xxxx <sup>[1]</sup> |
| 0                     | 0  | 0  | 0  | 0  | 0  | 0  | 1  | 01h                           | Input port 1              | read byte       | xxxx xxxx                |
| 0                     | 0  | 0  | 0  | 0  | 0  | 1  | 0  | 02h                           | Output port 0             | read/write byte | 1111 1111                |
| 0                     | 0  | 0  | 0  | 0  | 0  | 1  | 1  | 03h                           | Output port 1             | read/write byte | 1111 1111                |
| 0                     | 0  | 0  | 0  | 0  | 1  | 0  | 0  | 04h                           | Polarity Inversion port 0 | read/write byte | 0000 0000                |
| 0                     | 0  | 0  | 0  | 0  | 1  | 0  | 1  | 05h                           | Polarity Inversion port 1 | read/write byte | 0000 0000                |
| 0                     | 0  | 0  | 0  | 0  | 1  | 1  | 0  | 06h                           | Configuration port 0      | read/write byte | 1111 1111                |
| 0                     | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 07h                           | Configuration port 1      | read/write byte | 1111 1111                |

[1] Undefined.

### 6.2.2 Input port register pair (00h, 01h)

The Input port registers (registers 0 and 1) reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. The Input port registers are read only; writes to these registers have no effect. The default value 'X' is determined by the externally applied logic level. An Input port register read operation is performed as described in [Section 7.2 "Reading the port registers"](#).

**Table 5. Input port 0 register (address 00h)**

| Bit     | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|---------|------|------|------|------|------|------|------|------|
| Symbol  | I0.7 | I0.6 | I0.5 | I0.4 | I0.3 | I0.2 | I0.1 | I0.0 |
| Default | X    | X    | X    | X    | X    | X    | X    | X    |

**Table 6. Input port 1 register (address 01h)**

| Bit     | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|---------|------|------|------|------|------|------|------|------|
| Symbol  | I1.7 | I1.6 | I1.5 | I1.4 | I1.3 | I1.2 | I1.1 | I1.0 |
| Default | X    | X    | X    | X    | X    | X    | X    | X    |

### 6.2.3 Output port register pair (02h, 03h)

The Output port registers (registers 2 and 3) show the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in these registers have no effect on pins defined as inputs. In turn, reads from these registers reflect the value that was written to these registers, **not** the actual pin value. A register pair write is described in [Section 7.1](#) and a register pair read is described in [Section 7.2](#).

**Table 7. Output port 0 register (address 02h)**

| Bit     | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|---------|------|------|------|------|------|------|------|------|
| Symbol  | O0.7 | O0.6 | O0.5 | O0.4 | O0.3 | O0.2 | O0.1 | O0.0 |
| Default | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    |

**Table 8. Output port 1 register (address 03h)**

| Bit     | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|---------|------|------|------|------|------|------|------|------|
| Symbol  | O1.7 | O1.6 | O1.5 | O1.4 | O1.3 | O1.2 | O1.1 | O1.0 |
| Default | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    |

### 6.2.4 Polarity inversion register pair (04h, 05h)

The Polarity inversion registers (registers 4 and 5) allow polarity inversion of pins defined as inputs by the Configuration register. If a bit in these registers is set (written with '1'), the corresponding port pin's polarity is inverted in the Input register. If a bit in this register is cleared (written with a '0'), the corresponding port pin's polarity is retained. A register pair write is described in [Section 7.1](#) and a register pair read is described in [Section 7.2](#).

**Table 9. Polarity inversion port 0 register (address 04h)**

| Bit     | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|---------|------|------|------|------|------|------|------|------|
| Symbol  | N0.7 | N0.6 | N0.5 | N0.4 | N0.3 | N0.2 | N0.1 | N0.0 |
| Default | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |

**Table 10. Polarity inversion port 1 register (address 05h)**

| Bit     | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|---------|------|------|------|------|------|------|------|------|
| Symbol  | N1.7 | N1.6 | N1.5 | N1.4 | N1.3 | N1.2 | N1.1 | N1.0 |
| Default | 0    | 0    | 0    | 0    | 0    | 0    | 0    | 0    |

### 6.2.5 Configuration register pair (06h, 07h)

The Configuration registers (registers 6 and 7) configure the direction of the I/O pins. If a bit in these registers is set to 1, the corresponding port pin is enabled as a high-impedance input. If a bit in these registers is cleared to 0, the corresponding port pin is enabled as an output. A register pair write is described in [Section 7.1](#) and a register pair read is described in [Section 7.2](#).

**Table 11. Configuration port 0 register (address 06h)**

| Bit     | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|---------|------|------|------|------|------|------|------|------|
| Symbol  | C0.7 | C0.6 | C0.5 | C0.4 | C0.3 | C0.2 | C0.1 | C0.0 |
| Default | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    |

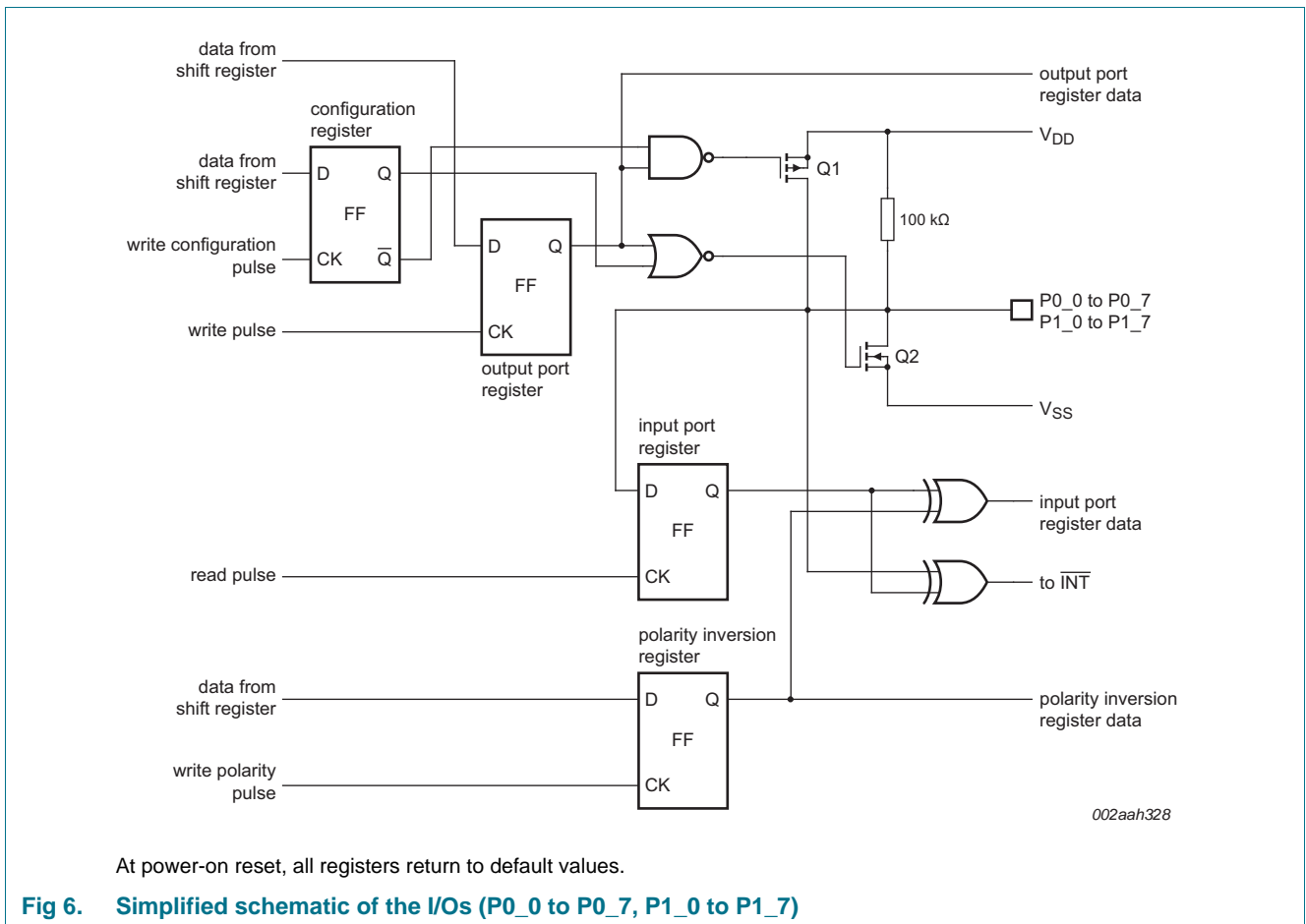
**Table 12. Configuration port 1 register (address 07h)**

| Bit     | 7    | 6    | 5    | 4    | 3    | 2    | 1    | 0    |
|---------|------|------|------|------|------|------|------|------|
| Symbol  | C1.7 | C1.6 | C1.5 | C1.4 | C1.3 | C1.2 | C1.1 | C1.0 |
| Default | 1    | 1    | 1    | 1    | 1    | 1    | 1    | 1    |

### 6.3 I/O port

When an I/O is configured as an input, FETs Q1 and Q2 are off, which creates a high-impedance input. The input voltage may be raised above  $V_{DD}$  to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output port register. In this case, there are low-impedance paths between the I/O pin and either  $V_{DD}$  or  $V_{SS}$ . The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.





## 6.4 Power-on reset

When power (from 0 V) is applied to  $V_{DD}$ , an internal power-on reset holds the PCA9555A in a reset condition until  $V_{DD}$  has reached  $V_{POR}$ . At that time, the reset condition is released and the PCA9555A registers and I<sup>2</sup>C-bus/SMBus state machine initializes to their default states. After that,  $V_{DD}$  must be lowered to below  $V_{PORF}$  and back up to the operating voltage for a power-reset cycle. See [Section 8.2 “Power-on reset requirements”](#).

## 6.5 Interrupt output

An interrupt is generated by any rising or falling edge of the port inputs in the Input mode. After time  $t_{V(INT)}$ , the signal  $INT$  is valid. The interrupt is reset when data on the port changes back to the original value or when data is read from the port that generated the interrupt (see [Figure 10](#) and [Figure 11](#)). Resetting occurs in the Read mode at the acknowledge (ACK) or not acknowledge (NACK) bit after the rising edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Any change of the I/Os after resetting is detected and is transmitted as  $\overline{INT}$ .

A pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur, if the state of the pin does not match the contents of the Input Port register.

# 7. Bus transactions

The PCA9555A is an I<sup>2</sup>C-bus slave device. Data is exchanged between the master and PCA9555A through write and read commands using I<sup>2</sup>C-bus. The two communication lines are a serial data line (SDA) and a serial clock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

## 7.1 Writing to the port registers

Data is transmitted to the PCA9555A by sending the device address and setting the least significant bit to a logic 0 (see [Figure 4 “PCA9555A device address”](#)). The command byte is sent after the address and determines which register will receive the data following the command byte.

Eight registers within the PCA9555A are configured to operate as four register pairs. The four pairs are input port, output port, polarity inversion, configuration registers. After sending data to one register, the next data byte is sent to the other register in the pair (see [Figure 7](#) and [Figure 8](#)). For example, if the first byte is sent to Output Port 1 (register 3), the next byte is stored in Output Port 0 (register 2).

There is no limitation on the number of data bytes sent in one write transmission. In this way, the host can continuously update a register pair independently of the other registers, or the host can simply update a single register.

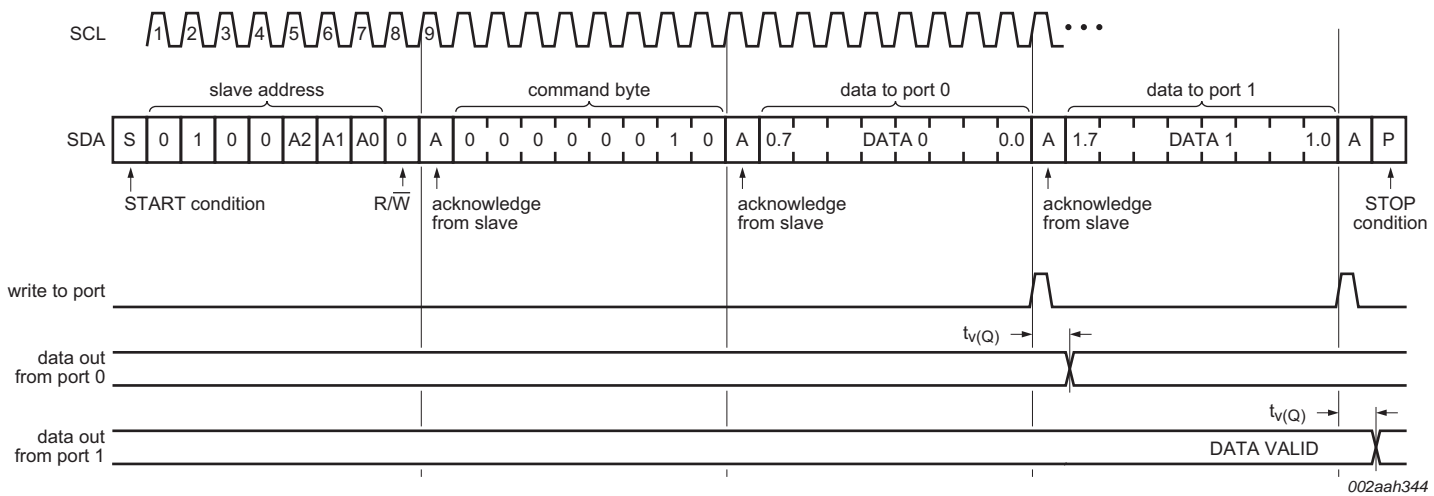


Fig 7. Write to output port registers

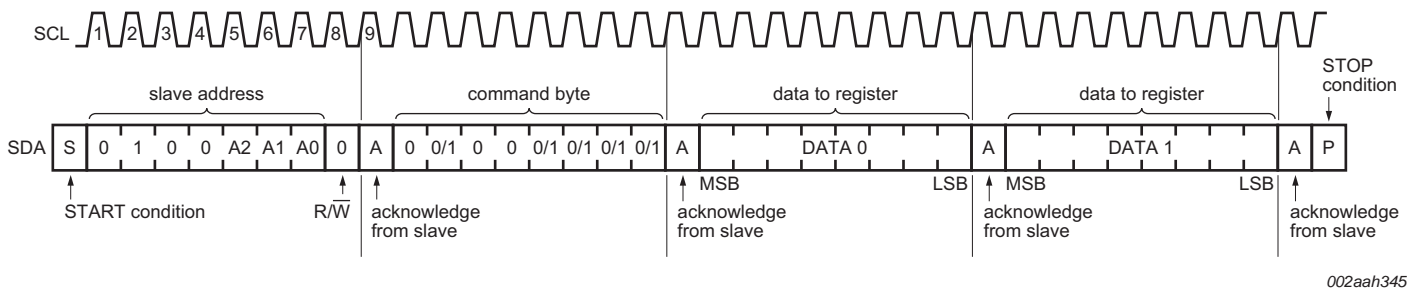
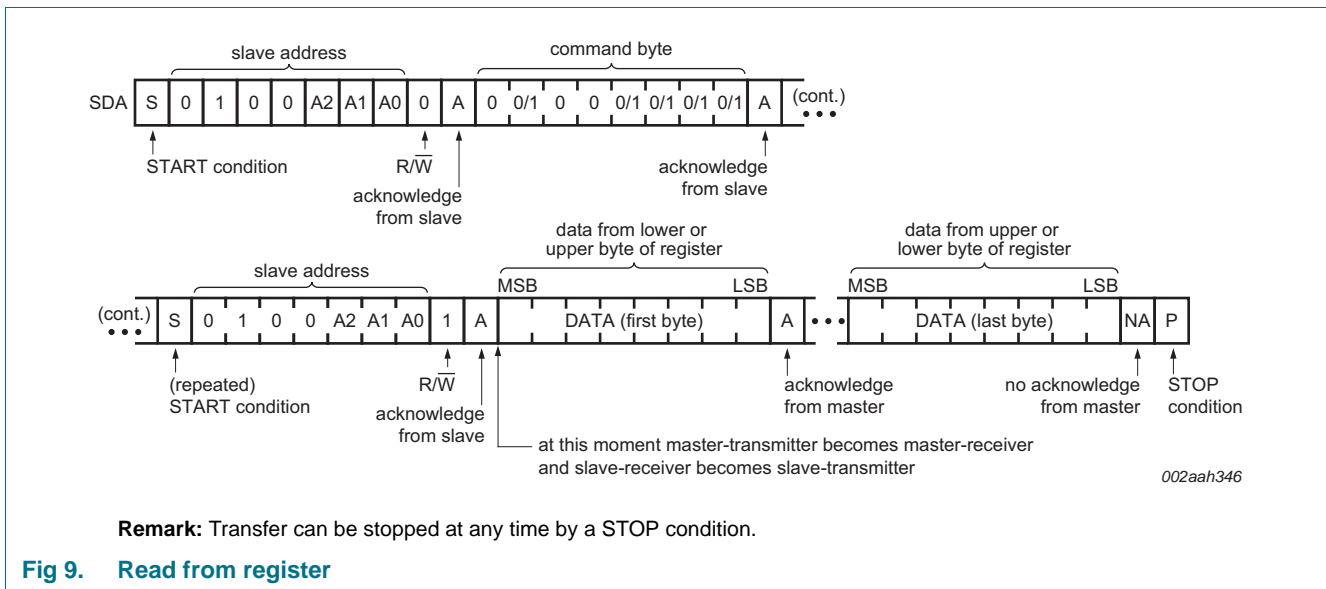


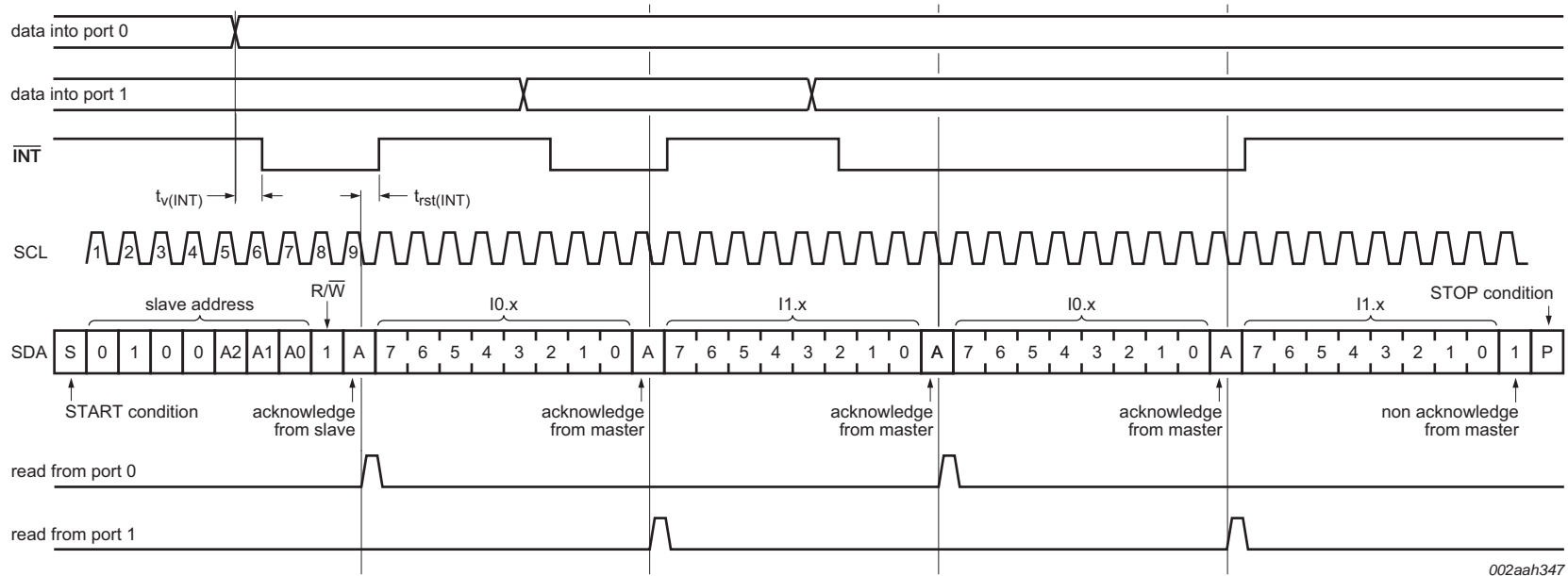
Fig 8. Write to Control registers

### 7.2 Reading the port registers

In order to read data from the PCA9555A, the bus master must first send the PCA9555A address with the least significant bit set to a logic 0 (see [Figure 4 "PCA9555A device address"](#)). The command byte is sent after the address and determines which register will be accessed. After a restart, the device address is sent again, but this time the least significant bit is set to a logic 1. Data from the register defined by the command byte is sent by the PCA9555A (see [Figure 9](#), [Figure 10](#) and [Figure 11](#)). Data is clocked into the register on the falling edge of the acknowledge clock pulse. After the first byte is read, additional bytes may be read but the data now reflects the information in the other register in the pair. For example, if Input Port 1 is read, the next byte read is Input Port 0. There is no limit on the number of data bytes received in one read transmission, but on the final byte received the bus master must not acknowledge the data.

After a subsequent restart, the command byte contains the value of the next register to be read in the pair. For example, if Input Port 1 was read last before the restart, the register that is read after the restart is the Input Port 0.

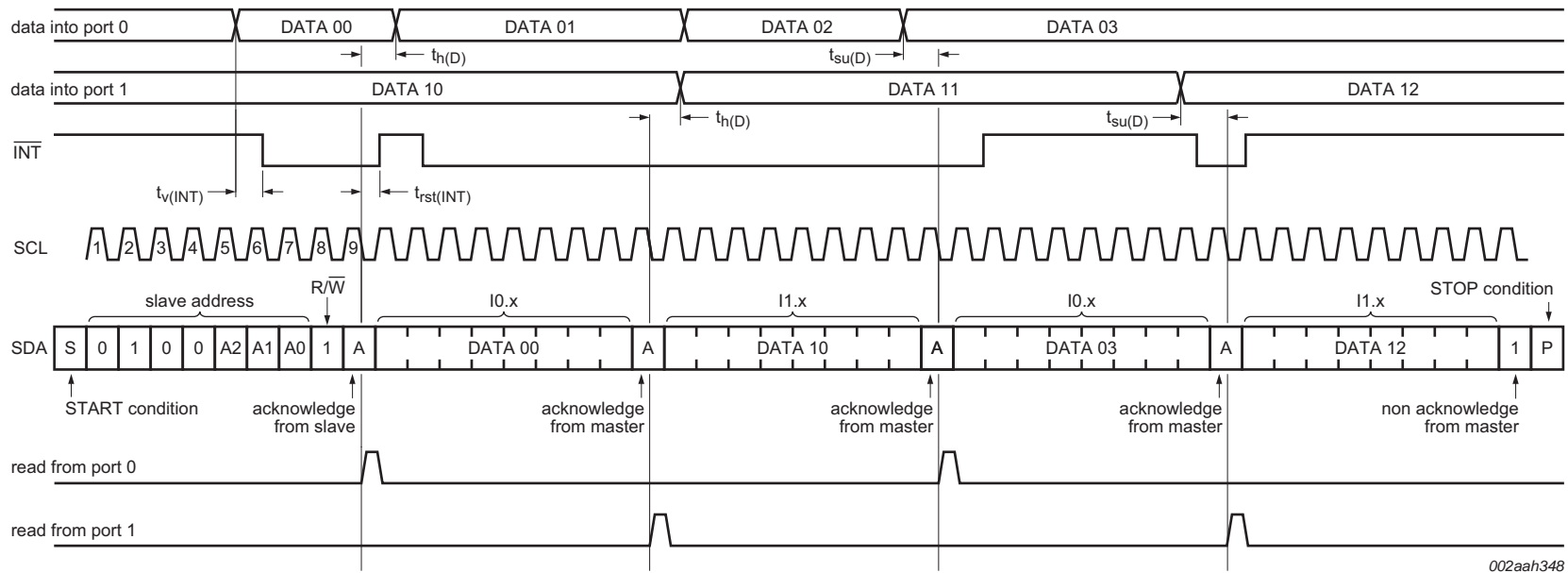




**Remark:** Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read input port register).

This figure eliminates the command byte transfer and a restart between the initial slave address call and the actual data transfer from P port (see [Figure 9](#)).

**Fig 10. Read input port register, scenario 1**

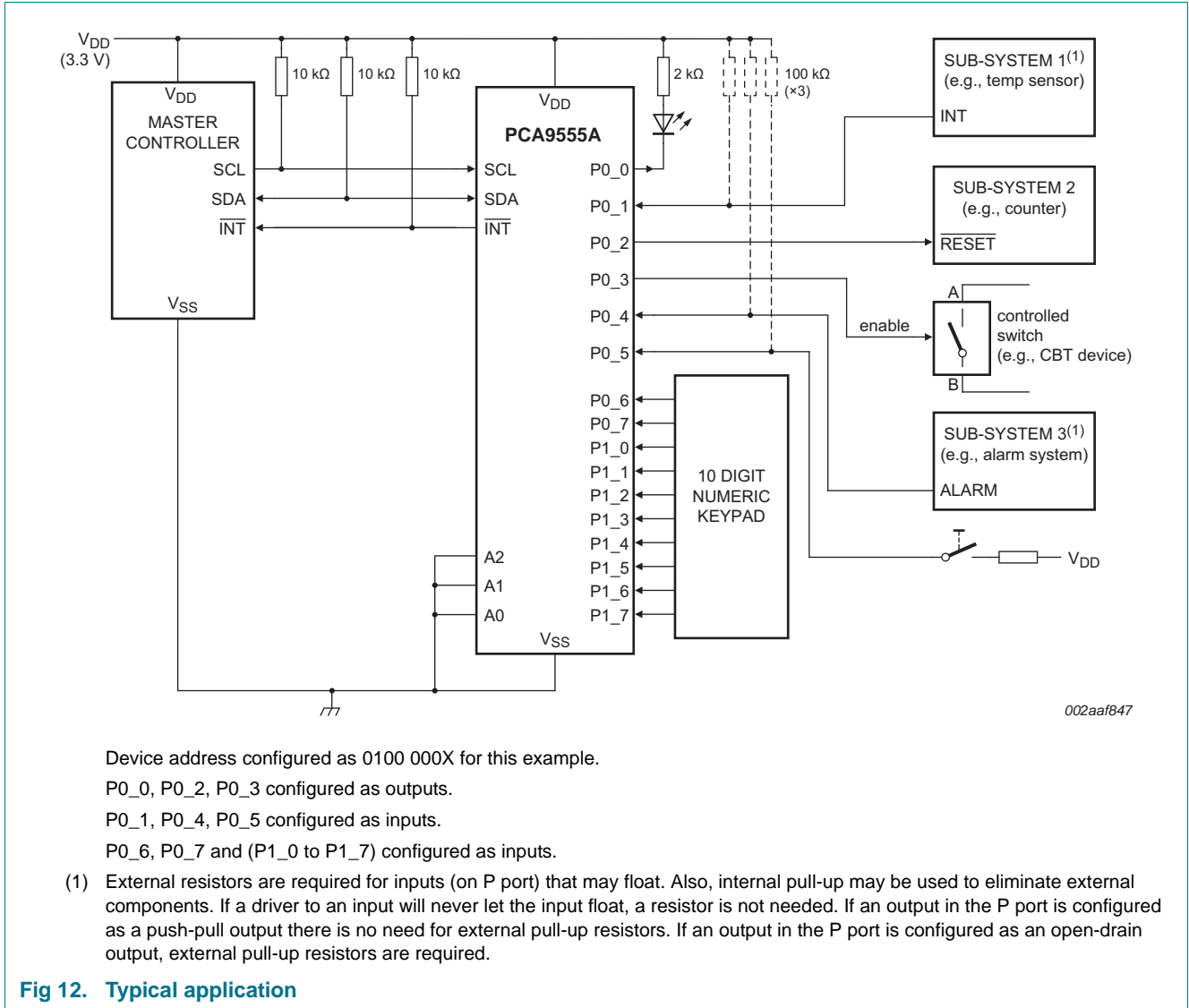


**Remark:** Transfer of data can be stopped at any moment by a STOP condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte has previously been set to '00' (read input port register).

This figure eliminates the command byte transfer and a restart between the initial slave address call and the actual data transfer from P port (see [Figure 9](#)).

**Fig 11. Read input port register, scenario 2**

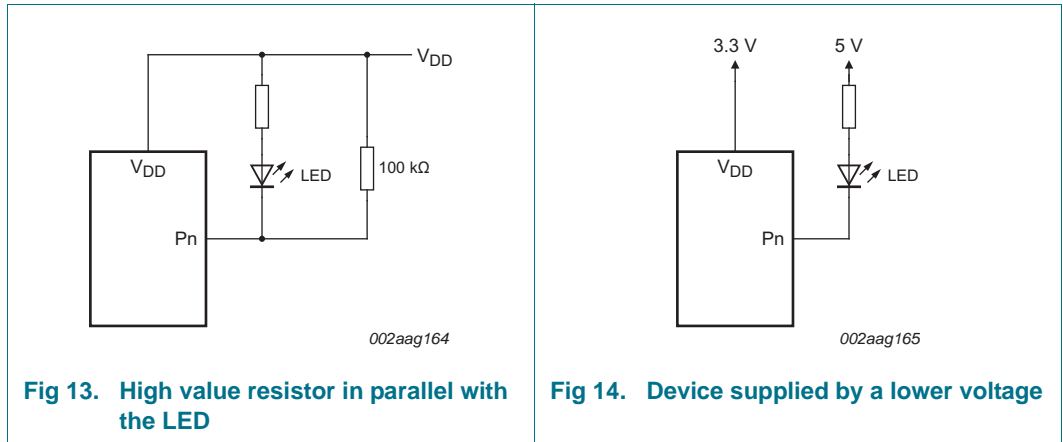
## 8. Application design-in information



### 8.1 Minimizing I<sub>DD</sub> when the I/Os are used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V<sub>DD</sub> through a resistor as shown in Figure 12. Since the LED acts as a diode, when the LED is off the I/O V<sub>I</sub> is about 1.2 V less than V<sub>DD</sub>. The supply current, I<sub>DD</sub>, increases as V<sub>I</sub> becomes lower than V<sub>DD</sub>.

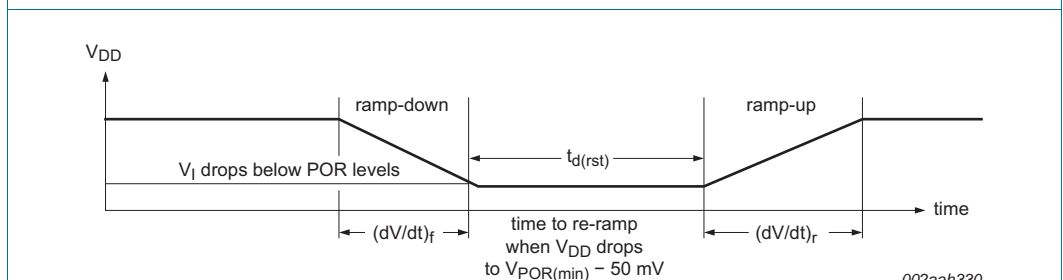
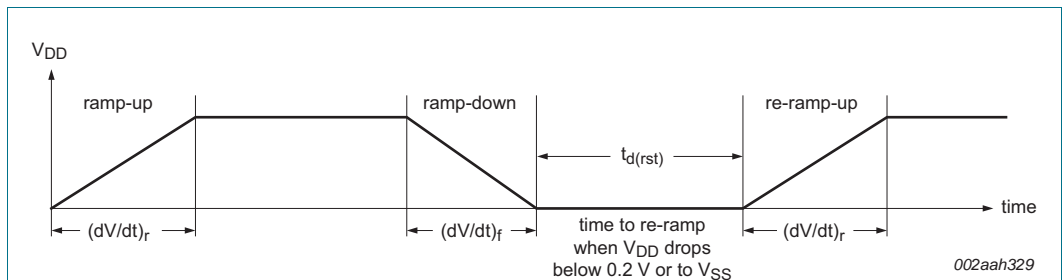
Designs needing to minimize current consumption, such as battery power applications, should consider maintaining the I/O pins greater than or equal to V<sub>DD</sub> when the LED is off. Figure 13 shows a high value resistor in parallel with the LED. Figure 14 shows V<sub>DD</sub> less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V<sub>I</sub> at or above V<sub>DD</sub> and prevents additional supply current consumption when the LED is off.



**8.2 Power-on reset requirements**

In the event of a glitch or data corruption, PCA9555A can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in [Figure 15](#) and [Figure 16](#).



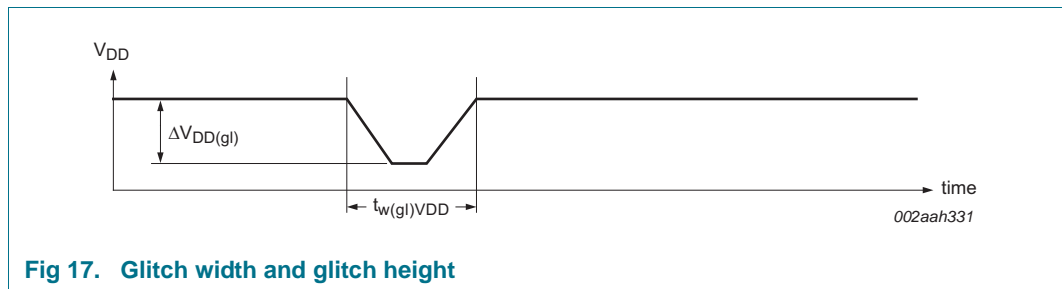
[Table 13](#) specifies the performance of the power-on reset feature for PCA9555A for both types of power-on reset.

**Table 13. Recommended supply sequencing and ramp rates**  
*T<sub>amb</sub> = 25 °C (unless otherwise noted). Not tested; specified by design.*

| Symbol                 | Parameter                         | Condition   | Min | Typ | Max  | Unit |
|------------------------|-----------------------------------|---|-----|-----|------|------|
| (dV/dt) <sub>f</sub>   | fall rate of change of voltage    | <a href="#">Figure 15</a>   | 0.1 | -   | 2000 | ms   |
| (dV/dt) <sub>r</sub>   | rise rate of change of voltage    | <a href="#">Figure 15</a>   | 0.1 | -   | 2000 | ms   |
| t <sub>d(rst)</sub>    | reset delay time                  | <a href="#">Figure 15</a> ; re-ramp time when V <sub>DD</sub> drops below 0.2 V or to V <sub>SS</sub> | 1   | -   | -    | μs   |
|                        |                                   | <a href="#">Figure 16</a> ; re-ramp time when V <sub>DD</sub> drops to V <sub>POR(min)</sub> - 50 mV  | 1   | -   | -    | μs   |
| ΔV <sub>DD(gl)</sub>   | glitch supply voltage difference  | <a href="#">Figure 17</a>   | [1] | -   | 1    | V    |
| t <sub>w(gl)VDD</sub>  | supply voltage glitch pulse width | <a href="#">Figure 17</a>   | [2] | -   | 10   | μs   |
| V <sub>POR(trip)</sub> | power-on reset trip voltage       | falling V <sub>DD</sub>   | 0.7 | -   | -    | V    |
|                        |                                   | rising V <sub>DD</sub>  | -   | -   | 1.4  | V    |

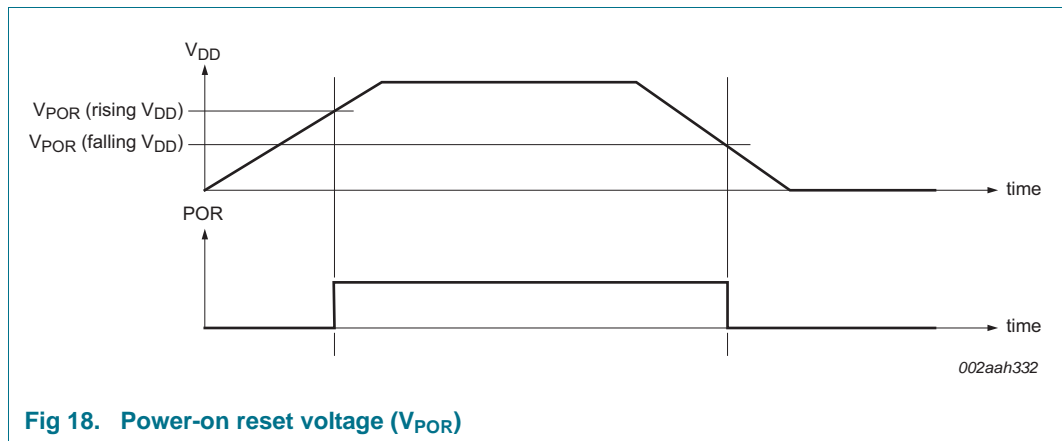
- [1] Level that V<sub>DD</sub> can glitch down to with a ramp rate of 0.4 μs/V, but not cause a functional disruption when t<sub>w(gl)VDD</sub> < 1 μs.
- [2] Glitch width that will not cause a functional disruption when ΔV<sub>DD(gl)</sub> = 0.5 × V<sub>DD</sub>.

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (t<sub>w(gl)VDD</sub>) and glitch height (ΔV<sub>DD(gl)</sub>) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. [Figure 17](#) and [Table 13](#) provide more information on how to measure these specifications.



**Fig 17. Glitch width and glitch height**

V<sub>POR</sub> is critical to the power-on reset. V<sub>POR</sub> is the voltage level at which the reset condition is released and all the registers and the I<sup>2</sup>C-bus/SMBus state machine are initialized to their default states. The value of V<sub>POR</sub> differs based on the V<sub>DD</sub> being lowered to or from 0 V. [Figure 18](#) and [Table 13](#) provide more details on this specification.



**Fig 18. Power-on reset voltage (V<sub>POR</sub>)**



### 8.3 Device current consumption with internal pull-up and pull-down resistors

The PCA9555A integrates pull-up resistors to eliminate external components when pins are configured as inputs and pull-up resistors are required (for example, nothing is driving the inputs to the power supply rails). Since these pull-up resistors are internal to the device itself, they contribute to the current consumption of the device and must be considered in the overall system design.

If the resistor is configured as a pull-up, that is, connected to  $V_{DD}$ , a current will flow from the  $V_{DD}$  pin through the resistor to ground when the pin is held LOW. This current will appear as additional  $I_{DD}$  upsetting any current consumption measurements.

The pull-up resistors are simple resistors and the current is linear with voltage. The resistance specification for these devices spans from 50 k $\Omega$  with a nominal 100 k $\Omega$  value. Any current flow through these resistors is additive by the number of pins held LOW and the current can be calculated by Ohm's law. See [Figure 22](#) for a graph of supply current versus the number of pull-up resistors.

## 9. Limiting values

**Table 14. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol              | Parameter                     | Conditions   | Min      | Max  | Unit |
|---------------------|-------------------------------|--|----------|------|------|
| V <sub>DD</sub>     | supply voltage                |  | -0.5     | +6.5 | V    |
| V <sub>I</sub>      | input voltage                 |  | [1] -0.5 | +6.5 | V    |
| V <sub>O</sub>      | output voltage                |  | [1] -0.5 | +6.5 | V    |
| I <sub>IK</sub>     | input clamping current        | A0, A1, A2, SCL; V <sub>I</sub> < 0 V                            | -        | ±20  | mA   |
| I <sub>OK</sub>     | output clamping current       | $\overline{\text{INT}}$ ; V <sub>O</sub> < 0 V                   | -        | ±20  | mA   |
| I <sub>IOK</sub>    | input/output clamping current | P port; V <sub>O</sub> < 0 V or V <sub>O</sub> > V <sub>DD</sub> | -        | ±20  | mA   |
|                     |                               | SDA; V <sub>O</sub> < 0 V or V <sub>O</sub> > V <sub>DD</sub>    | -        | ±20  | mA   |
| I <sub>OL</sub>     | LOW-level output current      | continuous; I/O port   | -        | 50   | mA   |
|                     |                               | continuous; SDA, $\overline{\text{INT}}$                         | -        | 25   | mA   |
| I <sub>OH</sub>     | HIGH-level output current     | continuous; P port   | -        | 25   | mA   |
| I <sub>DD</sub>     | supply current                |  | -        | 160  | mA   |
| I <sub>SS</sub>     | ground supply current         |  | -        | 200  | mA   |
| P <sub>tot</sub>    | total power dissipation       |  | -        | 200  | mW   |
| T <sub>stg</sub>    | storage temperature           |  | -65      | +150 | °C   |
| T <sub>j(max)</sub> | maximum junction temperature  |  | -        | 125  | °C   |

[1] The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

## 10. Recommended operating conditions

**Table 15. Operating conditions**

| Symbol           | Parameter                 | Conditions               | Min                   | Max                   | Unit |
|------------------|---------------------------|--------------------------|-----------------------|-----------------------|------|
| V <sub>DD</sub>  | supply voltage            |                          | 1.65                  | 5.5                   | V    |
| V <sub>IH</sub>  | HIGH-level input voltage  | SCL, SDA                 | 0.7 × V <sub>DD</sub> | 5.5                   | V    |
|                  |                           | A0, A1, A2, P1_7 to P0_0 | 0.7 × V <sub>DD</sub> | 5.5                   | V    |
| V <sub>IL</sub>  | LOW-level input voltage   | SCL, SDA                 | -0.5                  | 0.3 × V <sub>DD</sub> | V    |
|                  |                           | A0, A1, A2, P1_7 to P0_0 | -0.5                  | 0.3 × V <sub>DD</sub> | V    |
| I <sub>OH</sub>  | HIGH-level output current | P1_7 to P0_0             | -                     | 10                    | mA   |
| I <sub>OL</sub>  | LOW-level output current  | P1_7 to P0_0             | -                     | 25                    | mA   |
| T <sub>amb</sub> | ambient temperature       | operating in free air    | -40                   | +85                   | °C   |

## 11. Thermal characteristics

**Table 16. Thermal characteristics**

| Symbol               | Parameter  | Conditions      | Max    | Unit |
|----------------------|--|-----------------|--------|------|
| Z <sub>th(j-a)</sub> | transient thermal impedance from junction to ambient | TSSOP24 package | [1] 88 | K/W  |
|                      |  | HWQFN24 package | [1] 66 | K/W  |

[1] The package thermal impedance is calculated in accordance with JESD 51-7.

## 12. Static characteristics

**Table 17. Static characteristics**

$T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ;  $V_{DD} = 1.65\text{ V}$  to  $5.5\text{ V}$ ; unless otherwise specified.

| Symbol    | Parameter                 | Conditions   | Min                | Typ <sup>[1]</sup> | Max     | Unit          |
|-----------|---------------------------|--|--------------------|--------------------|---------|---------------|
| $V_{IK}$  | input clamping voltage    | $I_I = -18\text{ mA}$  | -1.2               | -                  | -       | V             |
| $V_{POR}$ | power-on reset voltage    | $V_I = V_{DD}$ or $V_{SS}$ ; $I_O = 0\text{ mA}$                     | -                  | 1.1                | 1.4     | V             |
| $I_{OL}$  | LOW-level output current  | $V_{OL} = 0.4\text{ V}$ ; $V_{DD} = 1.65\text{ V}$ to $5.5\text{ V}$ |                    |                    |         |               |
|           |                           | SDA  | 3                  | -                  | -       | mA            |
|           |                           | $\overline{\text{INT}}$  | 3                  | 15 <sup>[2]</sup>  | -       | mA            |
|           |                           | P port   |                    |                    |         |               |
|           |                           | $V_{OL} = 0.5\text{ V}$ ; $V_{DD} = 1.65\text{ V}$                   | <sup>[3]</sup> 8   | 10                 | -       | mA            |
|           |                           | $V_{OL} = 0.7\text{ V}$ ; $V_{DD} = 1.65\text{ V}$                   | <sup>[3]</sup> 10  | 13                 | -       | mA            |
|           |                           | $V_{OL} = 0.5\text{ V}$ ; $V_{DD} = 2.3\text{ V}$                    | <sup>[3]</sup> 8   | 10                 | -       | mA            |
|           |                           | $V_{OL} = 0.7\text{ V}$ ; $V_{DD} = 2.3\text{ V}$                    | <sup>[3]</sup> 10  | 13                 | -       | mA            |
|           |                           | $V_{OL} = 0.5\text{ V}$ ; $V_{DD} = 3.0\text{ V}$                    | <sup>[3]</sup> 8   | 14                 | -       | mA            |
|           |                           | $V_{OL} = 0.7\text{ V}$ ; $V_{DD} = 3.0\text{ V}$                    | <sup>[3]</sup> 10  | 19                 | -       | mA            |
| $V_{OH}$  | HIGH-level output voltage | P port   |                    |                    |         |               |
|           |                           | $I_{OH} = -8\text{ mA}$ ; $V_{DD} = 1.65\text{ V}$                   | <sup>[4]</sup> 1.2 | -                  | -       | V             |
|           |                           | $I_{OH} = -10\text{ mA}$ ; $V_{DD} = 1.65\text{ V}$                  | <sup>[4]</sup> 1.1 | -                  | -       | V             |
|           |                           | $I_{OH} = -8\text{ mA}$ ; $V_{DD} = 2.3\text{ V}$                    | <sup>[4]</sup> 1.8 | -                  | -       | V             |
|           |                           | $I_{OH} = -10\text{ mA}$ ; $V_{DD} = 2.3\text{ V}$                   | <sup>[4]</sup> 1.7 | -                  | -       | V             |
|           |                           | $I_{OH} = -8\text{ mA}$ ; $V_{DD} = 3.0\text{ V}$                    | <sup>[4]</sup> 2.6 | -                  | -       | V             |
|           |                           | $I_{OH} = -10\text{ mA}$ ; $V_{DD} = 3.0\text{ V}$                   | <sup>[4]</sup> 2.5 | -                  | -       | V             |
|           |                           | $I_{OH} = -8\text{ mA}$ ; $V_{DD} = 4.5\text{ V}$                    | <sup>[4]</sup> 4.1 | -                  | -       | V             |
| $V_{OL}$  | LOW-level output voltage  | P port; $I_{OL} = 8\text{ mA}$                                       |                    |                    |         |               |
|           |                           | $V_{DD} = 1.65\text{ V}$   | -                  | -                  | 0.45    | V             |
|           |                           | $V_{DD} = 2.3\text{ V}$  | -                  | -                  | 0.25    | V             |
|           |                           | $V_{DD} = 3.0\text{ V}$  | -                  | -                  | 0.25    | V             |
|           |                           | $V_{DD} = 4.5\text{ V}$  | -                  | -                  | 0.2     | V             |
| $I_I$     | input current             | $V_{DD} = 1.65\text{ V}$ to $5.5\text{ V}$                           |                    |                    |         |               |
|           |                           | SCL, SDA, $\overline{\text{RESET}}$ ; $V_I = V_{DD}$ or $V_{SS}$     | -                  | -                  | $\pm 1$ | $\mu\text{A}$ |
|           |                           | A0, A1, A2; $V_I = V_{DD}$ or $V_{SS}$                               | -                  | -                  | $\pm 1$ | $\mu\text{A}$ |
| $I_{IH}$  | HIGH-level input current  | P port; $V_I = V_{DD}$ ; $V_{DD} = 1.65\text{ V}$ to $5.5\text{ V}$  | -                  | -                  | 1       | $\mu\text{A}$ |
| $I_{IL}$  | LOW-level input current   | P port; $V_I = V_{SS}$ ; $V_{DD} = 1.65\text{ V}$ to $5.5\text{ V}$  | -                  | -                  | -100    | $\mu\text{A}$ |

Low-voltage 16-bit I<sup>2</sup>C-bus I/O port with interrupt and weak pull-up

Table 17. Static characteristics ...continued

$T_{amb} = -40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ ;  $V_{DD} = 1.65\text{ V}$  to  $5.5\text{ V}$ ; unless otherwise specified.

| Symbol   | Parameter                | Conditions   | Min                                 | Typ <sup>[1]</sup>  | Max | Unit          |  |
|--|--------------------------|--|-------------------------------------|---|-----|---------------|--|
| $I_{DD}$   | supply current           | SDA, P port, A0, A1, A2;<br>$V_I$ on SDA = $V_{DD}$ or $V_{SS}$ ;<br>$V_I$ on P port and A0, A1, A2 = $V_{DD}$ ;<br>$I_O = 0\text{ mA}$ ; I/O = inputs; $f_{SCL} = 400\text{ kHz}$         |                                     |   |     |               |  |
|  |                          | $V_{DD} = 3.6\text{ V}$ to $5.5\text{ V}$  | -                                   | 10  | 25  | $\mu\text{A}$ |  |
|  |                          | $V_{DD} = 2.3\text{ V}$ to $3.6\text{ V}$  | -                                   | 6.5   | 15  | $\mu\text{A}$ |  |
|  |                          | $V_{DD} = 1.65\text{ V}$ to $2.3\text{ V}$   | -                                   | 4   | 9   | $\mu\text{A}$ |  |
|  |                          | SCL, SDA, P port, A0, A1, A2;<br>$V_I$ on SCL, SDA = $V_{DD}$ or $V_{SS}$ ;<br>$V_I$ on P port and A0, A1, A2 = $V_{DD}$ ;<br>$I_O = 0\text{ mA}$ ; I/O = inputs; $f_{SCL} = 0\text{ kHz}$ |                                     |   |     |               |  |
|  |                          | $V_{DD} = 3.6\text{ V}$ to $5.5\text{ V}$  | -                                   | 1.5   | 7   | $\mu\text{A}$ |  |
|  |                          | $V_{DD} = 2.3\text{ V}$ to $3.6\text{ V}$  | -                                   | 1   | 3.2 | $\mu\text{A}$ |  |
|  |                          | $V_{DD} = 1.65\text{ V}$ to $2.3\text{ V}$   | -                                   | 0.5   | 1.7 | $\mu\text{A}$ |  |
|  |                          | Active mode; P port, A0, A1, A2;<br>$V_I$ on P port, A0, A1, A2 = $V_{DD}$ ;<br>$I_O = 0\text{ mA}$ ; I/O = inputs;<br>$f_{SCL} = 400\text{ kHz}$ , continuous register read               |                                     |   |     |               |  |
|  |                          | $V_{DD} = 3.6\text{ V}$ to $5.5\text{ V}$  | -                                   | 60  | 125 | $\mu\text{A}$ |  |
|  |                          | $V_{DD} = 2.3\text{ V}$ to $3.6\text{ V}$  | -                                   | 40  | 75  | $\mu\text{A}$ |  |
|  |                          | $V_{DD} = 1.65\text{ V}$ to $2.3\text{ V}$   | -                                   | 20  | 45  | $\mu\text{A}$ |  |
|  |                          | $\Delta I_{DD}$  | additional quiescent supply current | with pull-ups enabled; P port, A0, A1, A2;<br>$V_I$ on SCL and SDA = $V_{DD}$ or $V_{SS}$ ;<br>$V_I$ on P port = $V_{SS}$ ;<br>$V_I$ on A0, A1, A2 = $V_{DD}$ or $V_{SS}$ ;<br>$I_O = 0\text{ mA}$ ; I/O = inputs with pull-up enabled;<br>$f_{SCL} = 0\text{ kHz}$ |     |               |  |
| $V_{DD} = 1.65\text{ V}$ to $5.5\text{ V}$   | -                        |  |                                     | 1.1   | 1.5 | $\text{mA}$   |  |
| SCL, SDA; one input at $V_{DD} - 0.6\text{ V}$ , other inputs at $V_{DD}$ or $V_{SS}$ ; $V_{DD} = 1.65\text{ V}$ to $5.5\text{ V}$ | -                        |  |                                     | -   | 25  | $\mu\text{A}$ |  |
|  |                          | P port, A0, A1, A2; one input at $V_{DD} - 0.6\text{ V}$ , other inputs at $V_{DD}$ or $V_{SS}$ ;<br>$V_{DD} = 1.65\text{ V}$ to $5.5\text{ V}$  | -                                   | -   | 80  | $\mu\text{A}$ |  |
| $C_i$  | input capacitance        | $V_I = V_{DD}$ or $V_{SS}$ ; $V_{DD} = 1.65\text{ V}$ to $5.5\text{ V}$  | -                                   | 6   | 7   | $\text{pF}$   |  |
| $C_{iO}$   | input/output capacitance | $V_{I/O} = V_{DD}$ or $V_{SS}$ ; $V_D = 1.65\text{ V}$ to $5.5\text{ V}$   | -                                   | 7   | 8   | $\text{pF}$   |  |
|  |                          | $V_{I/O} = V_{DD}$ or $V_{SS}$ ; $V_{DD} = 1.65\text{ V}$ to $5.5\text{ V}$  | -                                   | 7.5   | 8.5 | $\text{pF}$   |  |

[1] For  $I_{DD}$ , all typical values are at nominal supply voltage (1.8 V, 2.5 V, 3.3 V, 3.6 V or 5 V  $V_{DD}$ ) and  $T_{amb} = 25\text{ }^{\circ}\text{C}$ . Except for  $I_{DD}$ , the typical values are at  $V_{DD} = 3.3\text{ V}$  and  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .

[2] Typical value for  $T_{amb} = 25\text{ }^{\circ}\text{C}$ .  $V_{OL} = 0.4\text{ V}$  and  $V_{DD} = 3.3\text{ V}$ . Typical value for  $V_{DD} < 2.5\text{ V}$ ,  $V_{OL} = 0.6\text{ V}$ .

[3] Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 200 mA.

[4] The total current sourced by all I/Os must be limited to 160 mA.

12.1 Typical characteristics

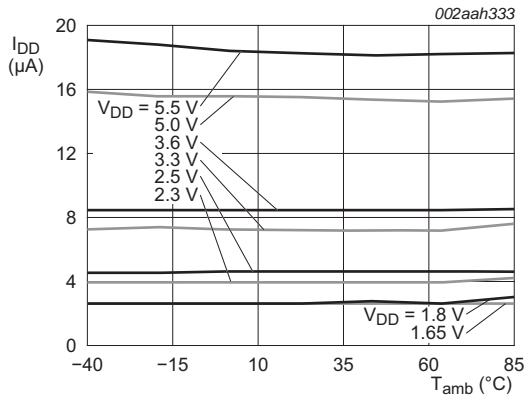


Fig 19. Supply current versus ambient temperature

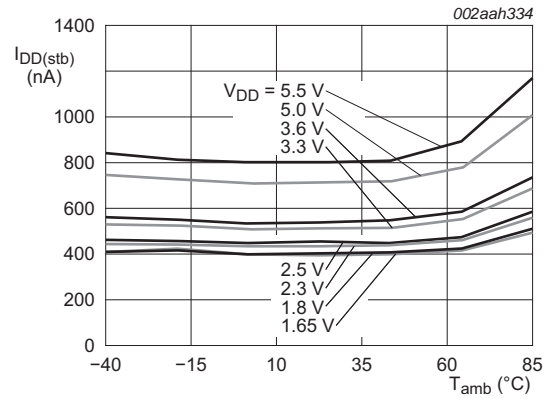


Fig 20. Standby supply current versus ambient temperature

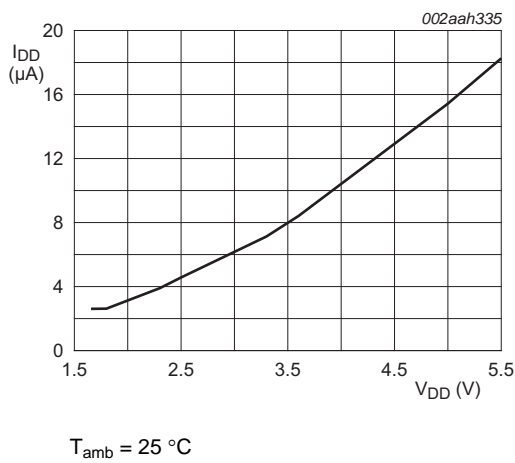


Fig 21. Supply current versus supply voltage

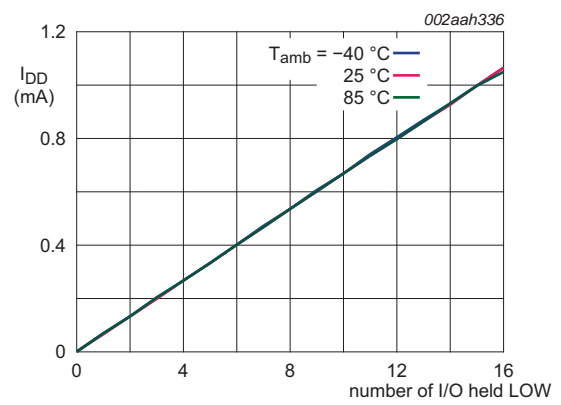
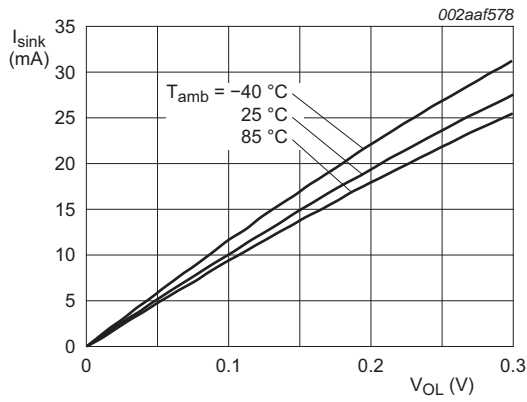
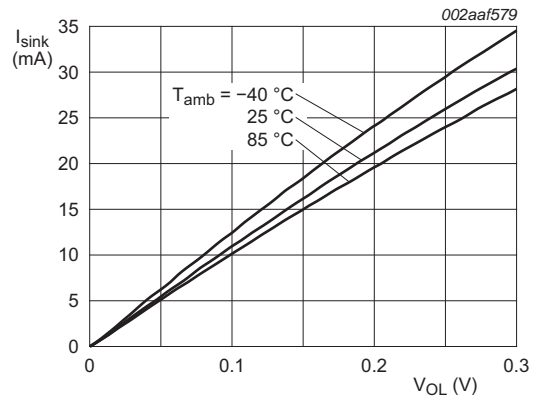


Fig 22. Supply current versus number of I/O held LOW

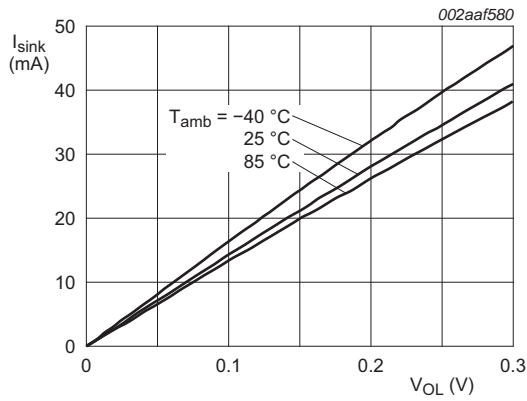
Low-voltage 16-bit I<sup>2</sup>C-bus I/O port with interrupt and weak pull-up



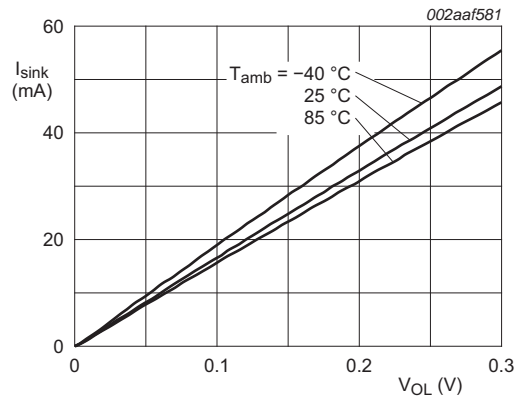
a.  $V_{DD} = 1.65\text{ V}$



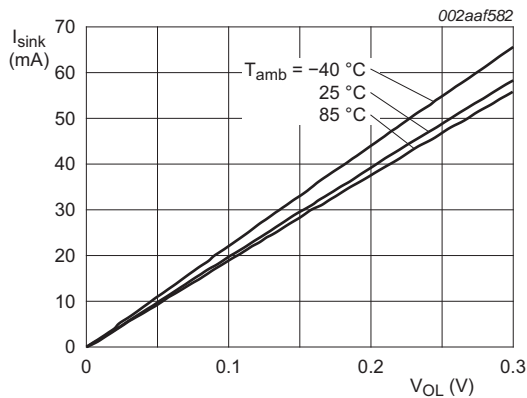
b.  $V_{DD} = 1.8\text{ V}$



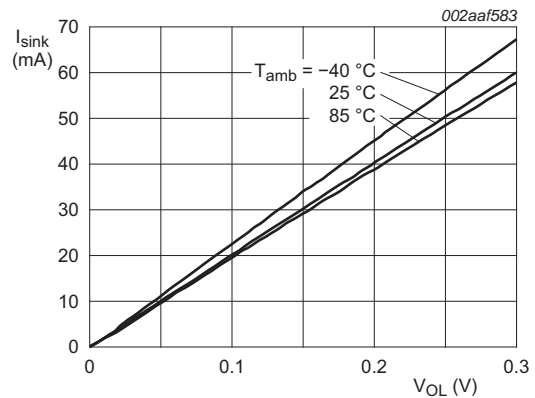
c.  $V_{DD} = 2.5\text{ V}$



d.  $V_{DD} = 3.3\text{ V}$



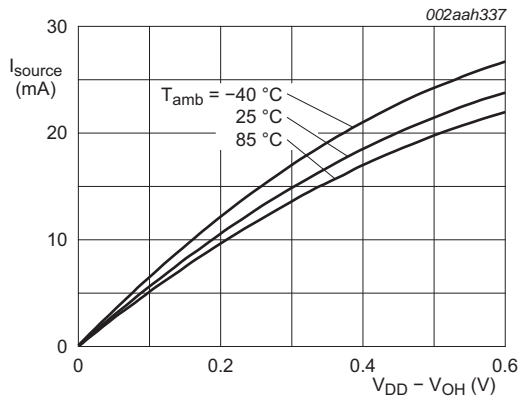
e.  $V_{DD} = 5.0\text{ V}$



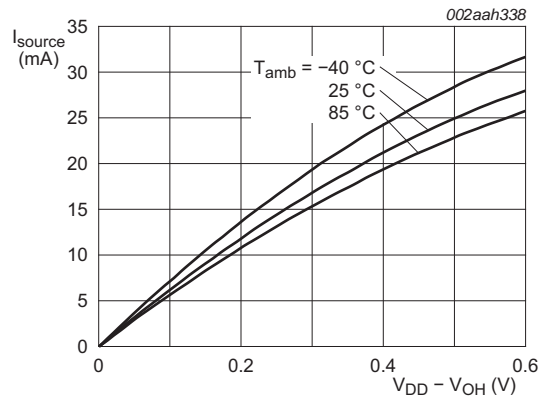
f.  $V_{DD} = 5.5\text{ V}$

Fig 23. I/O sink current versus LOW-level output voltage

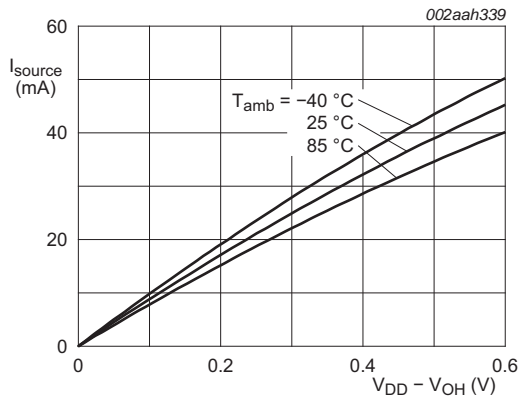
Low-voltage 16-bit I<sup>2</sup>C-bus I/O port with interrupt and weak pull-up



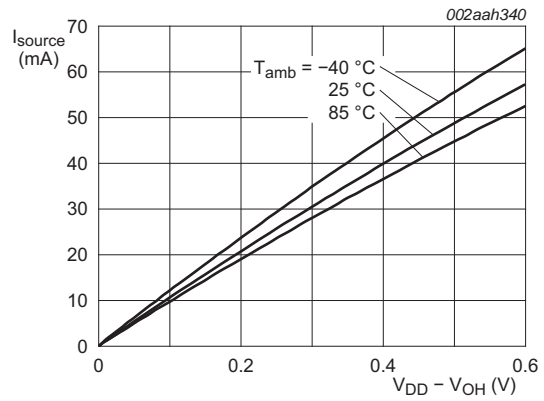
a.  $V_{DD} = 1.65\text{ V}$



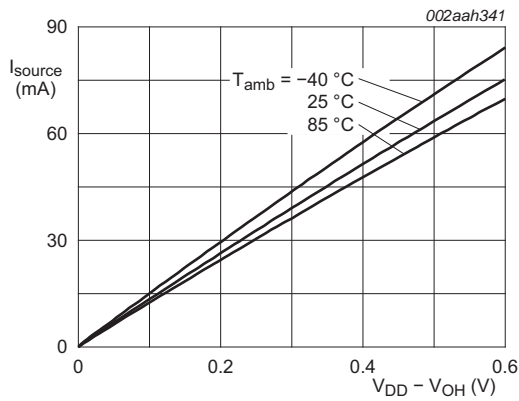
b.  $V_{DD} = 1.8\text{ V}$



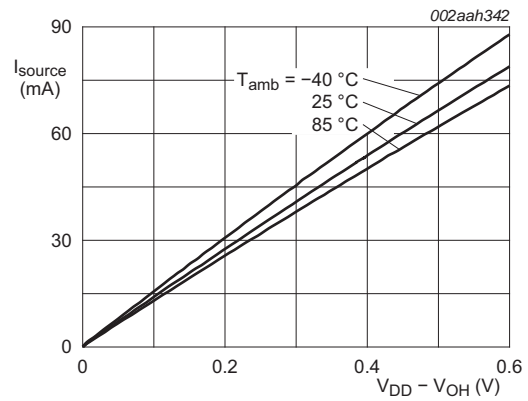
c.  $V_{DD} = 2.5\text{ V}$



d.  $V_{DD} = 3.3\text{ V}$



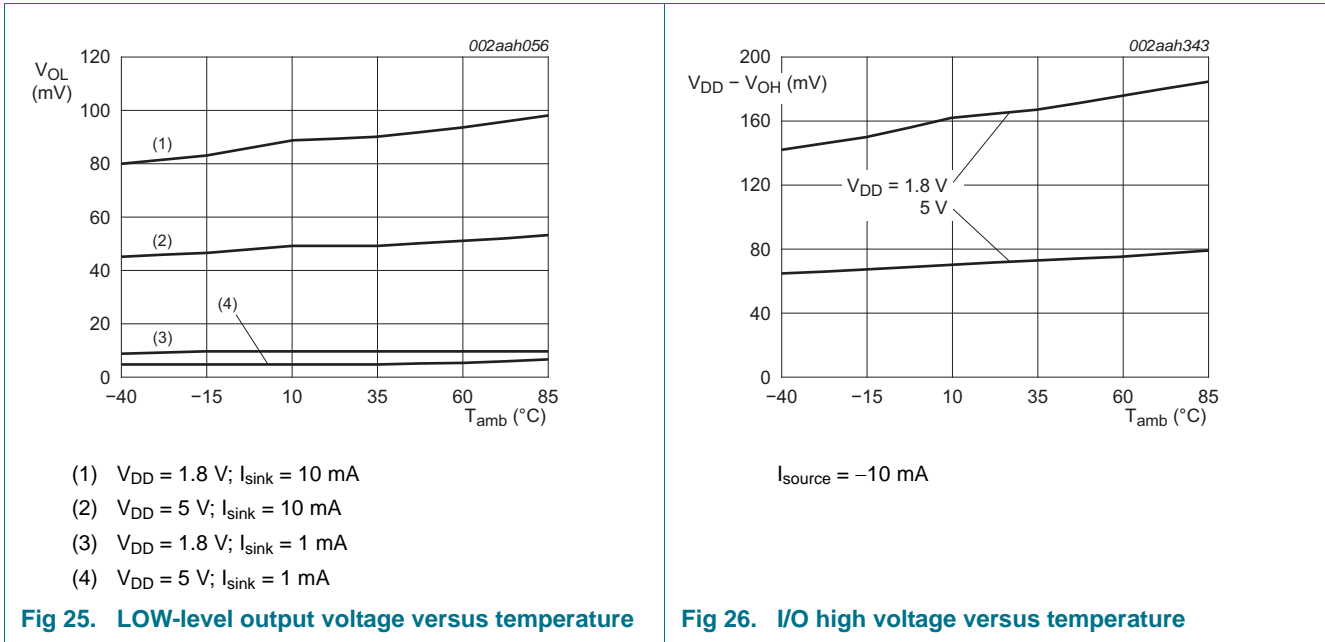
e.  $V_{DD} = 5.0\text{ V}$



f.  $V_{DD} = 5.5\text{ V}$

Fig 24. I/O source current versus HIGH-level output voltage

Low-voltage 16-bit I<sup>2</sup>C-bus I/O port with interrupt and weak pull-up





### 13. Dynamic characteristics

**Table 18. I<sup>2</sup>C-bus interface timing requirements**

Over recommended operating free air temperature range, unless otherwise specified. See [Figure 27](#).

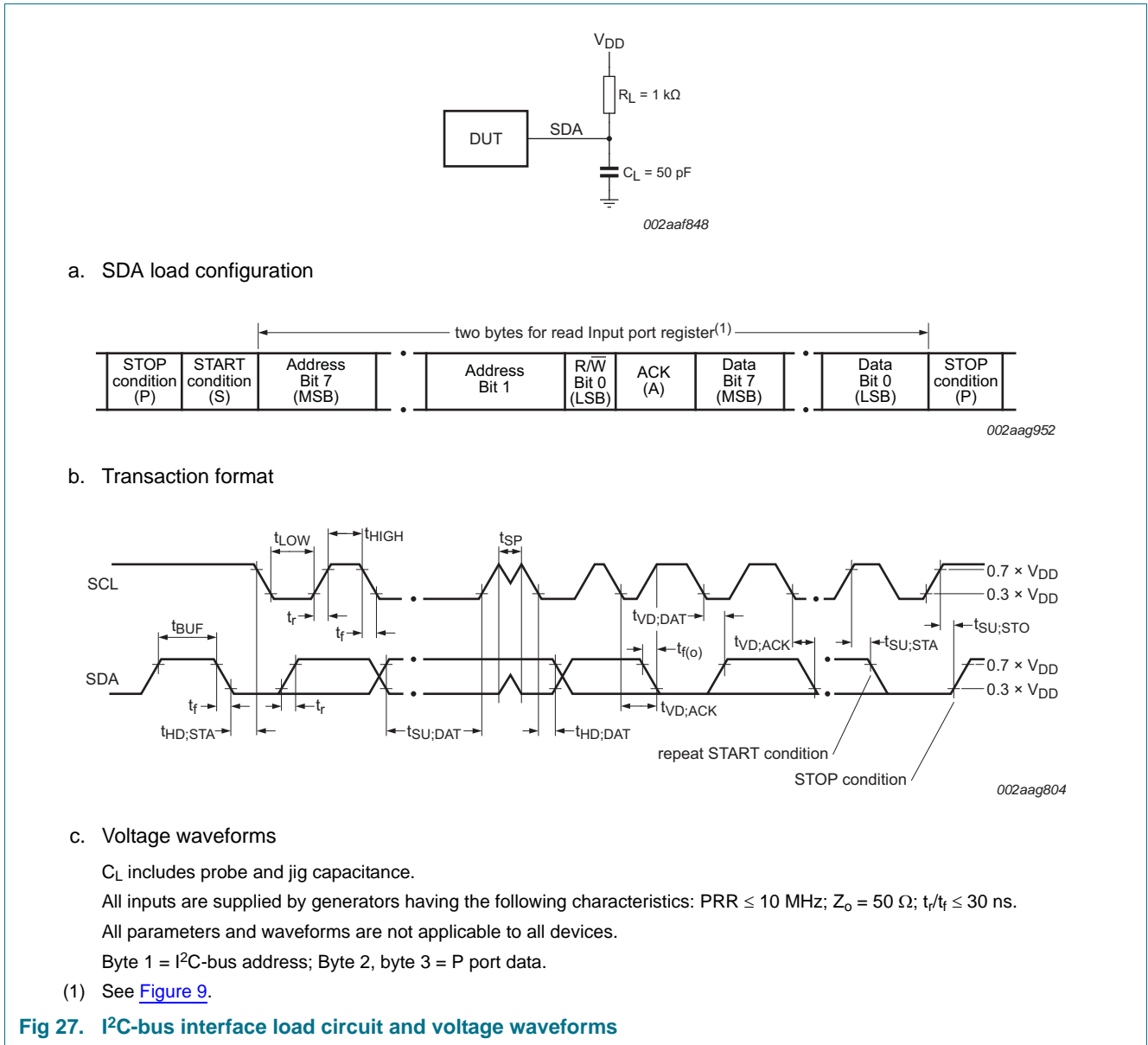
| Symbol              | Parameter   | Conditions                               | Standard-mode I <sup>2</sup> C-bus |      | Fast-mode I <sup>2</sup> C-bus    |     | Unit |
|---------------------|---|--|------------------------------------|------|-----------------------------------|-----|------|
|                     |   |  | Min                                | Max  | Min                               | Max |      |
| f <sub>SCL</sub>    | SCL clock frequency   |  | 0                                  | 100  | 0                                 | 400 | kHz  |
| t <sub>HIGH</sub>   | HIGH period of the SCL clock                                      |  | 4                                  | -    | 0.6                               | -   | μs   |
| t <sub>LOW</sub>    | LOW period of the SCL clock                                       |  | 4.7                                | -    | 1.3                               | -   | μs   |
| t <sub>SP</sub>     | pulse width of spikes that must be suppressed by the input filter |  | 0                                  | 50   | 0                                 | 50  | ns   |
| t <sub>SU;DAT</sub> | data set-up time  |  | 250                                | -    | 100                               | -   | ns   |
| t <sub>HD;DAT</sub> | data hold time  |  | 0                                  | -    | 0                                 | -   | ns   |
| t <sub>r</sub>      | rise time of both SDA and SCL signals                             |  | -                                  | 1000 | 20                                | 300 | ns   |
| t <sub>f</sub>      | fall time of both SDA and SCL signals                             |  | -                                  | 300  | 20 ×<br>(V <sub>DD</sub> / 5.5 V) | 300 | ns   |
| t <sub>BUF</sub>    | bus free time between a STOP and START condition                  |  | 4.7                                | -    | 1.3                               | -   | μs   |
| t <sub>SU;STA</sub> | set-up time for a repeated START condition                        |  | 4.7                                | -    | 0.6                               | -   | μs   |
| t <sub>HD;STA</sub> | hold time (repeated) START condition                              |  | 4                                  | -    | 0.6                               | -   | μs   |
| t <sub>SU;STO</sub> | set-up time for STOP condition                                    |  | 4                                  | -    | 0.6                               | -   | μs   |
| t <sub>VD;DAT</sub> | data valid time   | SCL LOW to SDA output valid              | -                                  | 3.45 | -                                 | 0.9 | μs   |
| t <sub>VD;ACK</sub> | data valid acknowledge time                                       | ACK signal from SCL LOW to SDA (out) LOW | -                                  | 3.45 | -                                 | 0.9 | μs   |

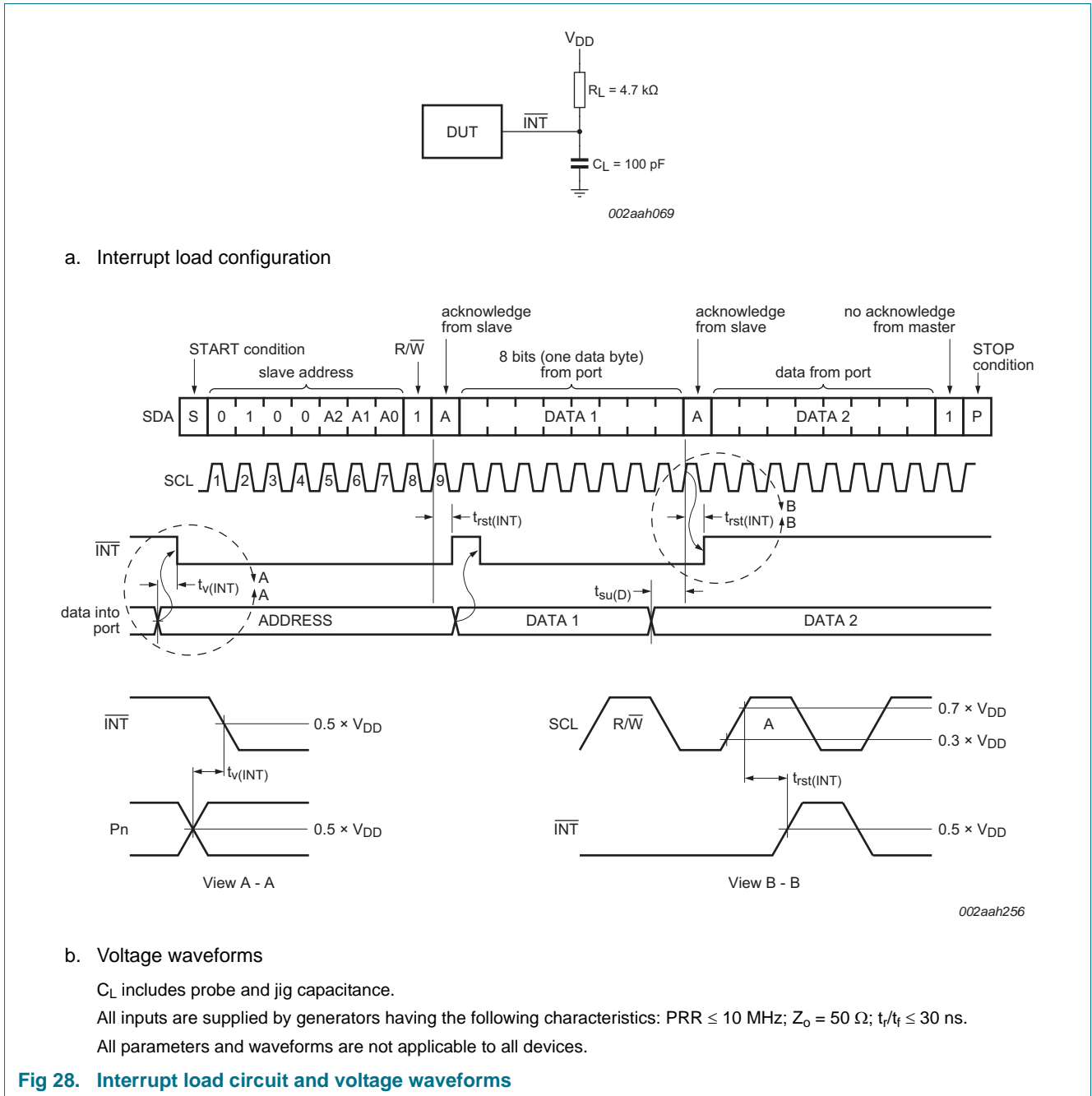
**Table 19. Switching characteristics**

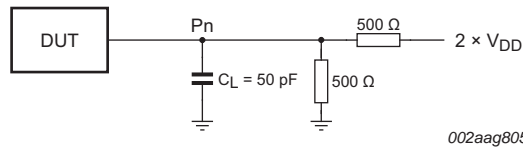
Over recommended operating free air temperature range; C<sub>L</sub> ≤ 100 pF; unless otherwise specified. See [Figure 28](#).

| Symbol                | Parameter                                 | Conditions                             | Standard-mode I <sup>2</sup> C-bus |     | Fast-mode I <sup>2</sup> C-bus |     | Unit |
|-----------------------|---|--|------------------------------------|-----|--------------------------------|-----|------|
|                       |   |  | Min                                | Max | Min                            | Max |      |
| t <sub>V(INT)</sub>   | valid time on pin $\overline{\text{INT}}$ | from P port to $\overline{\text{INT}}$ | -                                  | 1   | -                              | 1   | μs   |
| t <sub>rst(INT)</sub> | reset time on pin $\overline{\text{INT}}$ | from SCL to $\overline{\text{INT}}$    | -                                  | 1   | -                              | 1   | μs   |
| t <sub>V(Q)</sub>     | data output valid time                    | from SCL to P port                     | -                                  | 400 | -                              | 400 | ns   |
| t <sub>SU(D)</sub>    | data input set-up time                    | from P port to SCL                     | 0                                  | -   | 0                              | -   | ns   |
| t <sub>h(D)</sub>     | data input hold time                      | from P port to SCL                     | 300                                | -   | 300                            | -   | ns   |

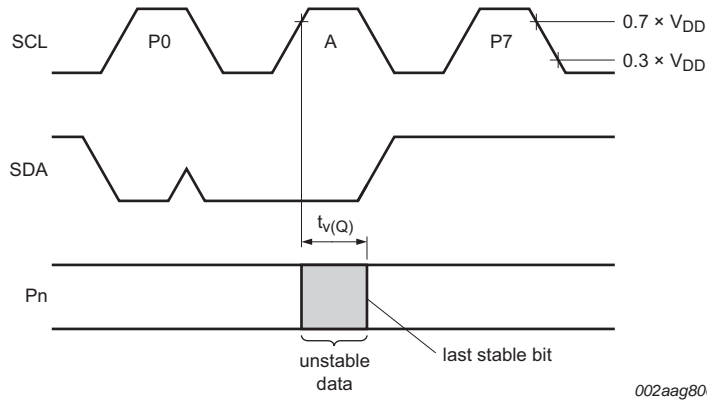
14. Parameter measurement information



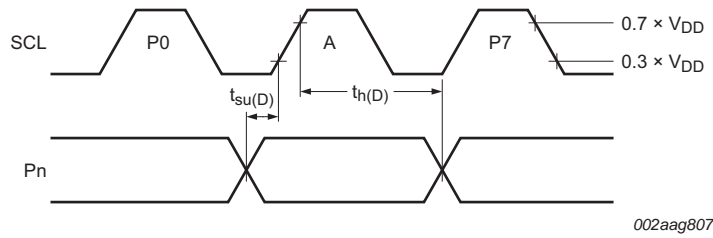




a. P port load configuration



b. Write mode ( $\overline{R/\overline{W}} = 0$ )



c. Read mode ( $\overline{R/\overline{W}} = 1$ )

$C_L$  includes probe and jig capacitance.

$t_{V(Q)}$  is measured from  $0.7 \times V_{DD}$  on SCL to 50 % I/O ( $P_n$ ) output.

All inputs are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz;  $Z_o = 50 \Omega$ ;  $t_r/t_f \leq 30$  ns.

The outputs are measured one at a time, with one transition per measurement.

All parameters and waveforms are not applicable to all devices.

Fig 29. P port load circuit and voltage waveforms

15. Package outline

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

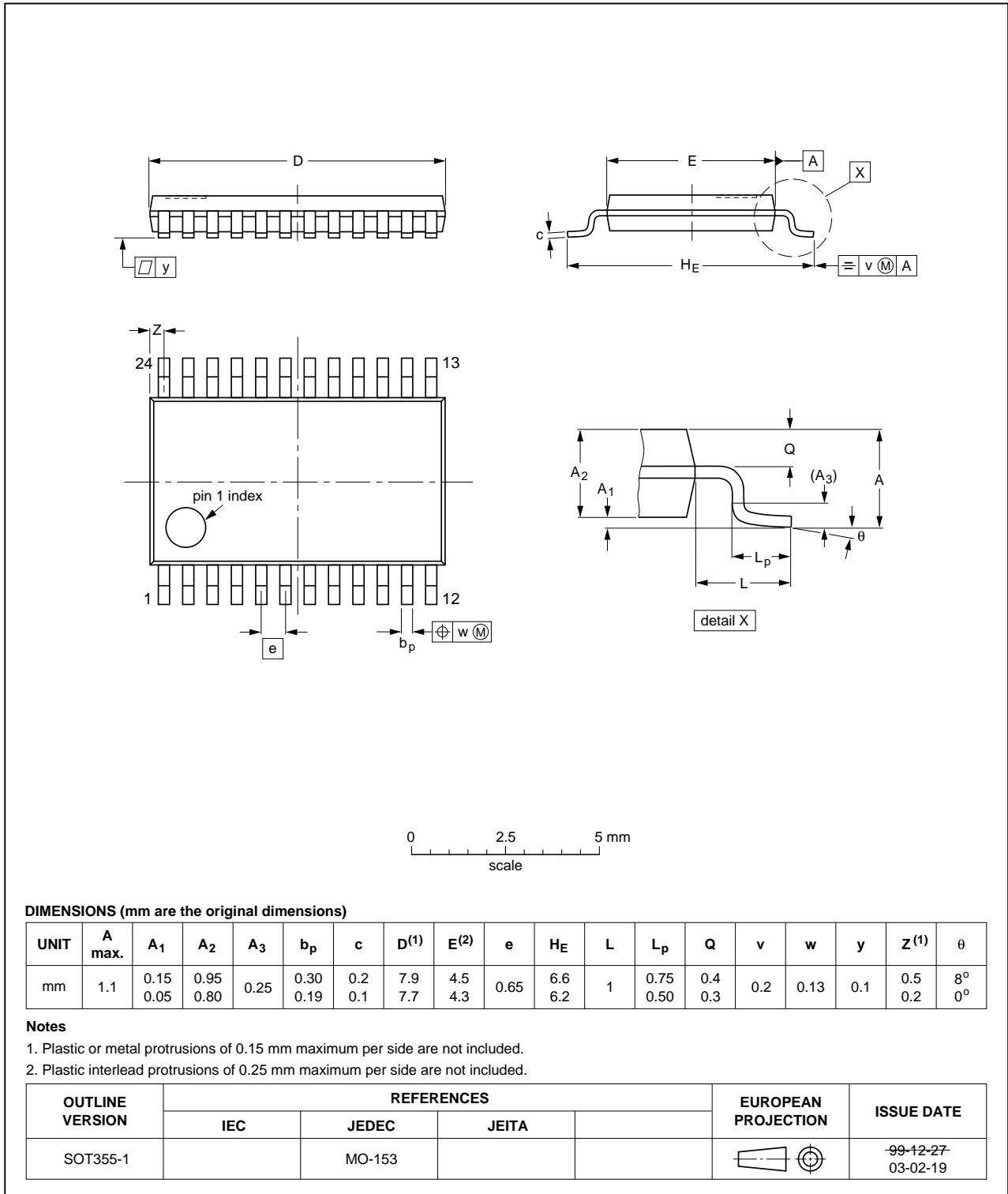


Fig 30. Package outline SOT355-1 (TSSOP24)

HWQFN24: plastic thermal enhanced very very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.75 mm

SOT994-1

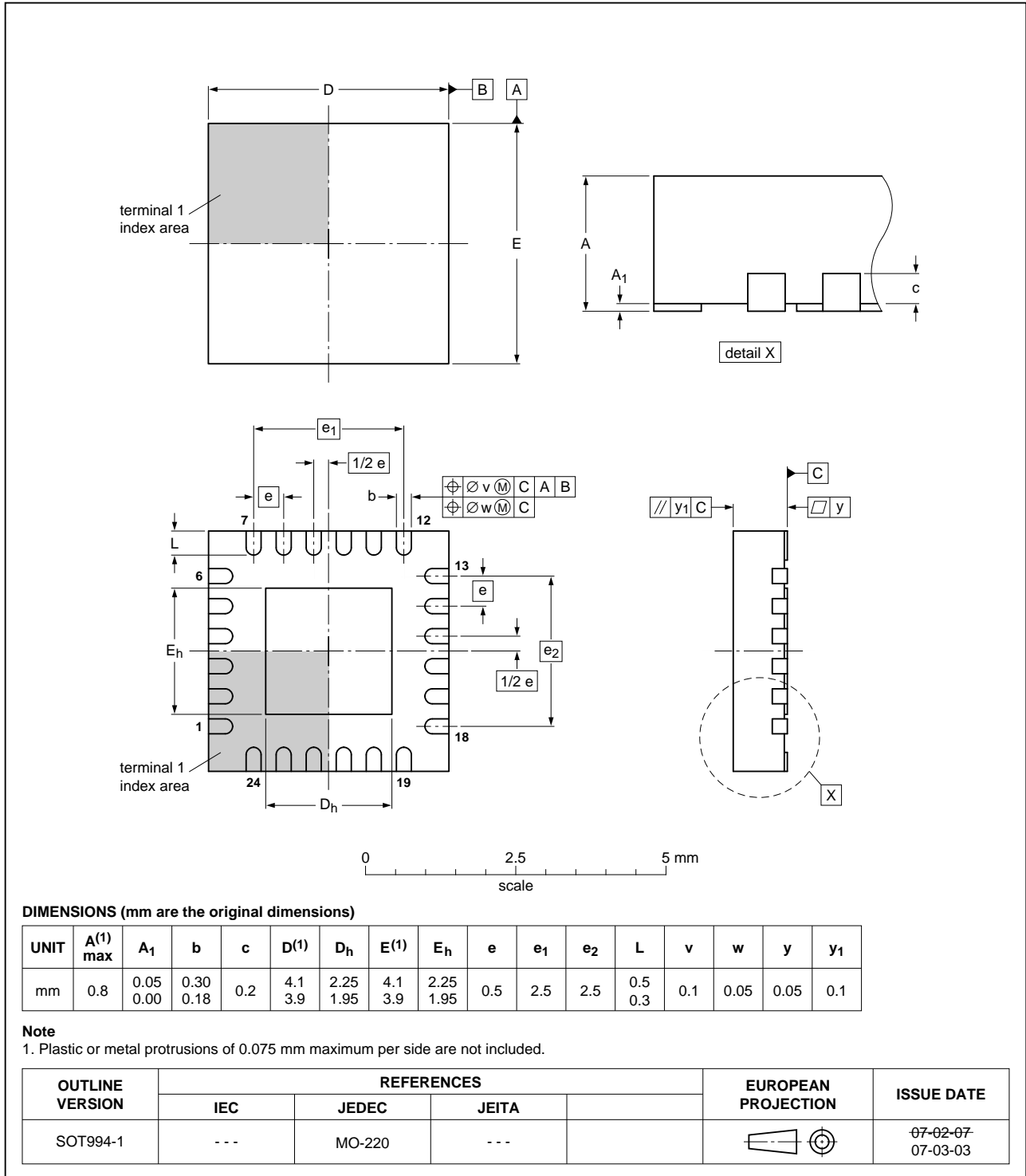


Fig 31. Package outline SOT994-1 (HWQFN24)

## 16. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

## 17. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

### 17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

### 17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

### 17.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

### 17.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 32](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 20](#) and [21](#)

**Table 20. SnPb eutectic process (from J-STD-020C)**

| Package thickness (mm) | Package reflow temperature (°C) |       |
|------------------------|---------------------------------|-------|
|                        | Volume (mm <sup>3</sup> )       |       |
|                        | < 350                           | ≥ 350 |
| < 2.5                  | 235                             | 220   |
| ≥ 2.5                  | 220                             | 220   |

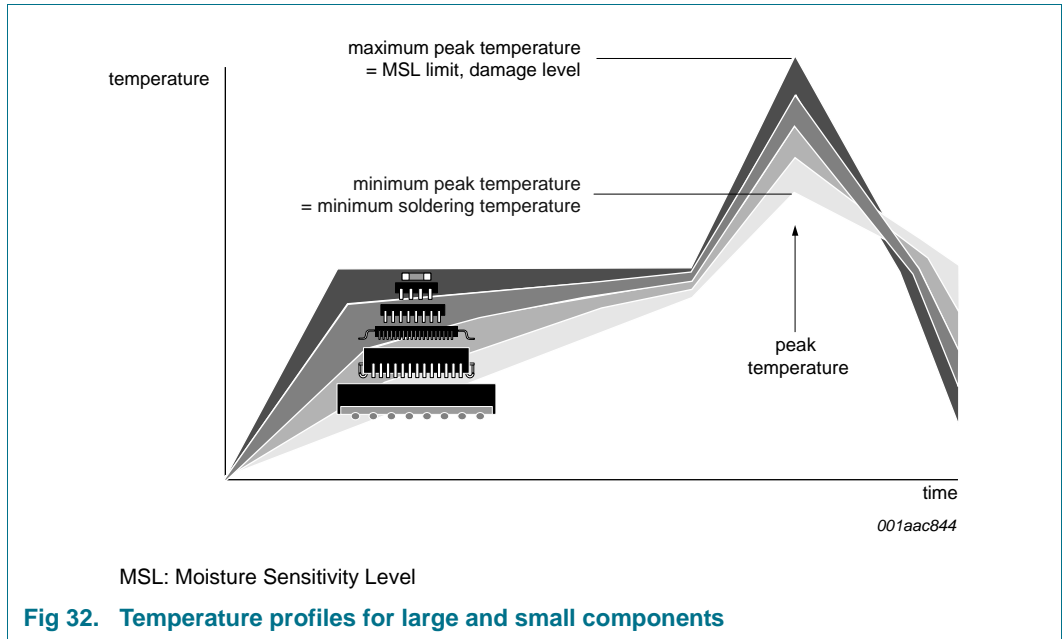
**Table 21. Lead-free process (from J-STD-020C)**

| Package thickness (mm) | Package reflow temperature (°C) |             |        |
|------------------------|---------------------------------|-------------|--------|
|                        | Volume (mm <sup>3</sup> )       |             |        |
|                        | < 350                           | 350 to 2000 | > 2000 |
| < 1.6                  | 260                             | 260         | 260    |
| 1.6 to 2.5             | 260                             | 250         | 245    |
| > 2.5                  | 250                             | 245         | 245    |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 32](#).





For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

18. Soldering: PCB footprints

Footprint information for reflow soldering of TSSOP24 package

SOT355-1

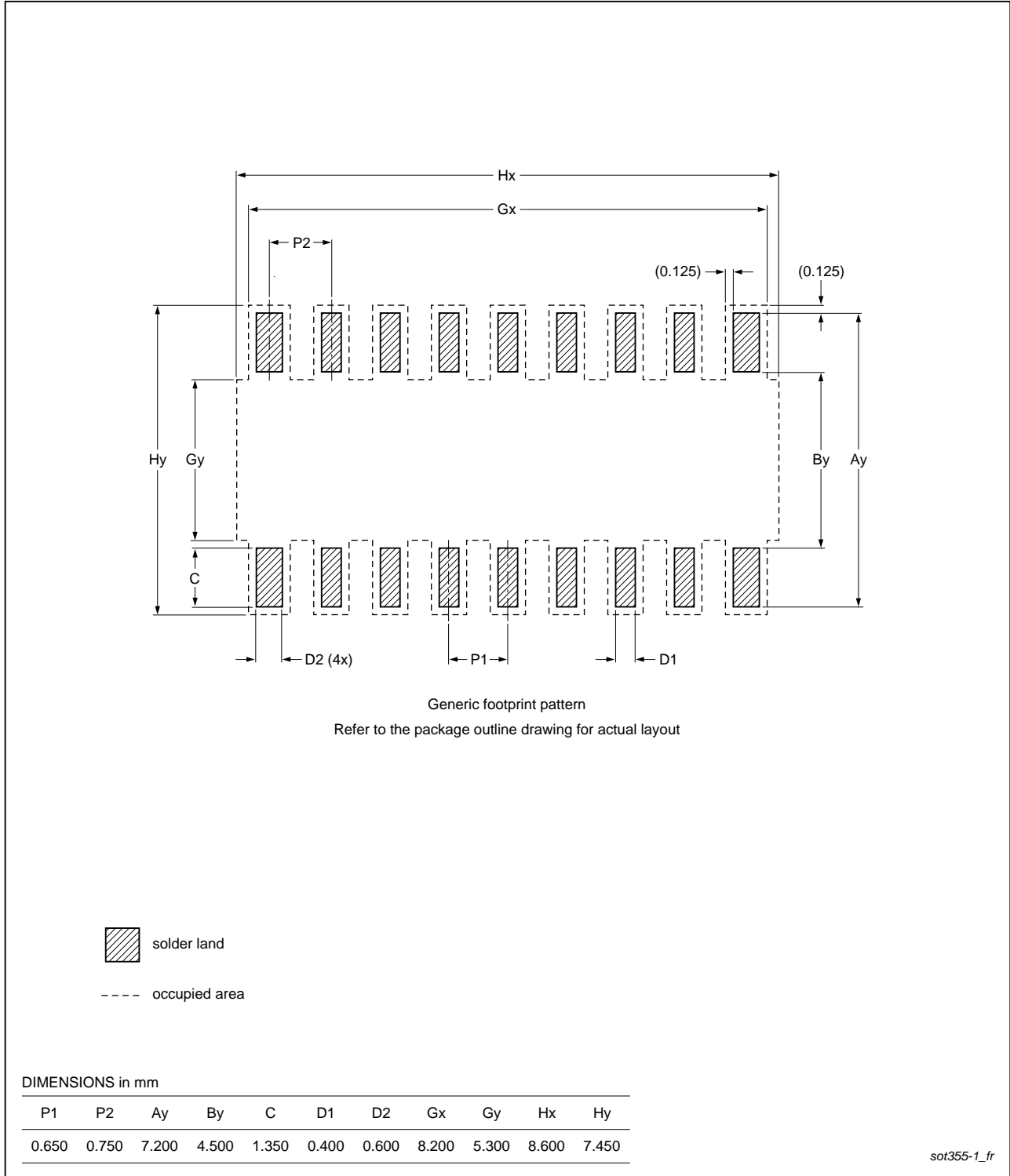


Fig 33. PCB footprint for SOT355-1 (TSSOP24); reflow soldering

Footprint information for reflow soldering of HVQFN24 package

SOT994-1

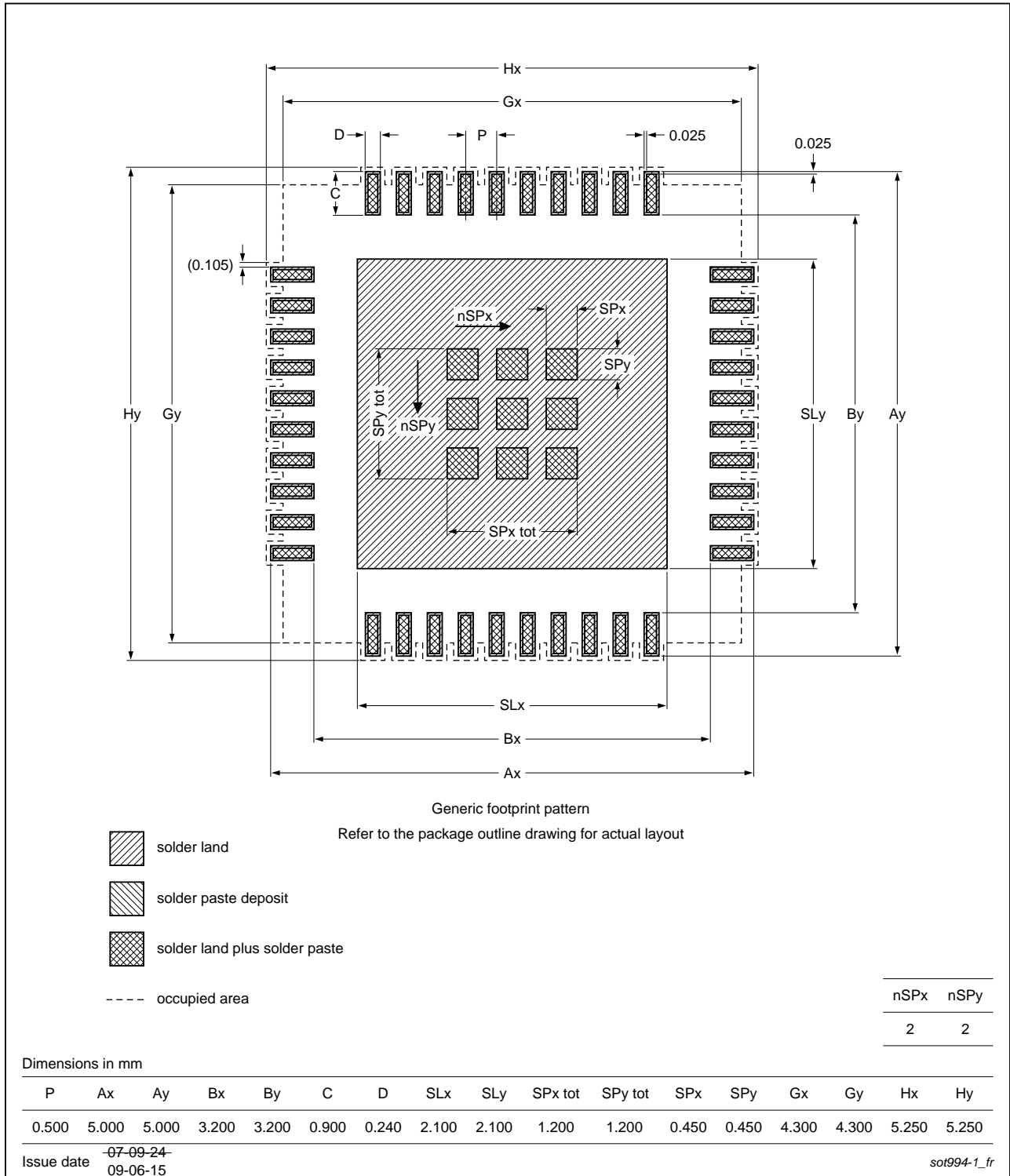


Fig 34. PCB footprint for SOT994-1 (HVQFN24); reflow soldering

## 19. Abbreviations

**Table 22. Abbreviations**

| Acronym              | Description                                |
|----------------------|--|
| ACPI                 | Advanced Configuration and Power Interface |
| CBT                  | Cross-Bar Technology                       |
| CDM                  | Charged-Device Model                       |
| CMOS                 | Complementary Metal-Oxide Semiconductor    |
| ESD                  | ElectroStatic Discharge                    |
| FET                  | Field-Effect Transistor                    |
| FF                   | Flip-Flop                                  |
| GPIO                 | General Purpose Input/Output               |
| HBM                  | Human Body Model                           |
| I <sup>2</sup> C-bus | Inter-Integrated Circuit bus               |
| I/O                  | Input/Output                               |
| LED                  | Light Emitting Diode                       |
| SMBus                | System Management Bus                      |

## 20. Revision history

**Table 23. Revision history**

| Document ID  | Release date | Data sheet status  | Change notice | Supersedes |
|--------------|--------------|--------------------|---------------|------------|
| PCA9555A v.1 | 20120911     | Product data sheet | -             | -          |

## 21. Legal information

### 21.1 Data sheet status

| Document status <sup>[1][2]</sup> | Product status <sup>[3]</sup> | Definition  |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet      | Development                   | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet    | Qualification                 | This document contains data from the preliminary specification.                       |
| Product [short] data sheet        | Production                    | This document contains the product specification.                                     |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 21.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 21.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Non-automotive qualified products** — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's

own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

## 21.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

**I<sup>2</sup>C-bus** — logo is a trademark of NXP B.V.

## 22. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 23. Contents

|           |   |           |           |                                      |           |
|-----------|---|-----------|-----------|--------------------------------------|-----------|
| <b>1</b>  | <b>General description</b> . . . . .  | <b>1</b>  | <b>20</b> | <b>Revision history</b> . . . . .    | <b>36</b> |
| <b>2</b>  | <b>Features and benefits</b> . . . . .  | <b>2</b>  | <b>21</b> | <b>Legal information</b> . . . . .   | <b>37</b> |
| <b>3</b>  | <b>Ordering information</b> . . . . .   | <b>2</b>  | 21.1      | Data sheet status . . . . .          | 37        |
| 3.1       | Ordering options . . . . .  | 2         | 21.2      | Definitions . . . . .                | 37        |
| <b>4</b>  | <b>Block diagram</b> . . . . .  | <b>3</b>  | 21.3      | Disclaimers . . . . .                | 37        |
| <b>5</b>  | <b>Pinning information</b> . . . . .  | <b>3</b>  | 21.4      | Trademarks . . . . .                 | 38        |
| 5.1       | Pinning . . . . .   | 3         | <b>22</b> | <b>Contact information</b> . . . . . | <b>38</b> |
| 5.2       | Pin description . . . . .   | 4         | <b>23</b> | <b>Contents</b> . . . . .            | <b>39</b> |
| <b>6</b>  | <b>Functional description</b> . . . . .   | <b>5</b>  |           |                                      |           |
| 6.1       | Device address . . . . .  | 5         |           |                                      |           |
| 6.2       | Registers . . . . .   | 5         |           |                                      |           |
| 6.2.1     | Pointer register and command byte . . . . .   | 5         |           |                                      |           |
| 6.2.2     | Input port register pair (00h, 01h) . . . . .   | 6         |           |                                      |           |
| 6.2.3     | Output port register pair (02h, 03h) . . . . .  | 6         |           |                                      |           |
| 6.2.4     | Polarity inversion register pair (04h, 05h) . . . . .                                 | 7         |           |                                      |           |
| 6.2.5     | Configuration register pair (06h, 07h) . . . . .                                      | 7         |           |                                      |           |
| 6.3       | I/O port . . . . .  | 8         |           |                                      |           |
| 6.4       | Power-on reset . . . . .  | 9         |           |                                      |           |
| 6.5       | Interrupt output . . . . .  | 9         |           |                                      |           |
| <b>7</b>  | <b>Bus transactions</b> . . . . .   | <b>9</b>  |           |                                      |           |
| 7.1       | Writing to the port registers . . . . .   | 9         |           |                                      |           |
| 7.2       | Reading the port registers . . . . .  | 11        |           |                                      |           |
| <b>8</b>  | <b>Application design-in information</b> . . . . .                                    | <b>14</b> |           |                                      |           |
| 8.1       | Minimizing I <sub>DD</sub> when the I/Os are used<br>to control LEDs . . . . .        | 14        |           |                                      |           |
| 8.2       | Power-on reset requirements . . . . .   | 15        |           |                                      |           |
| 8.3       | Device current consumption with internal<br>pull-up and pull-down resistors . . . . . | 17        |           |                                      |           |
| <b>9</b>  | <b>Limiting values</b> . . . . .  | <b>18</b> |           |                                      |           |
| <b>10</b> | <b>Recommended operating conditions</b> . . . . .                                     | <b>18</b> |           |                                      |           |
| <b>11</b> | <b>Thermal characteristics</b> . . . . .  | <b>18</b> |           |                                      |           |
| <b>12</b> | <b>Static characteristics</b> . . . . .   | <b>19</b> |           |                                      |           |
| 12.1      | Typical characteristics . . . . .   | 21        |           |                                      |           |
| <b>13</b> | <b>Dynamic characteristics</b> . . . . .  | <b>25</b> |           |                                      |           |
| <b>14</b> | <b>Parameter measurement information</b> . . . . .                                    | <b>26</b> |           |                                      |           |
| <b>15</b> | <b>Package outline</b> . . . . .  | <b>29</b> |           |                                      |           |
| <b>16</b> | <b>Handling information</b> . . . . .   | <b>31</b> |           |                                      |           |
| <b>17</b> | <b>Soldering of SMD packages</b> . . . . .  | <b>31</b> |           |                                      |           |
| 17.1      | Introduction to soldering . . . . .   | 31        |           |                                      |           |
| 17.2      | Wave and reflow soldering . . . . .   | 31        |           |                                      |           |
| 17.3      | Wave soldering . . . . .  | 31        |           |                                      |           |
| 17.4      | Reflow soldering . . . . .  | 32        |           |                                      |           |
| <b>18</b> | <b>Soldering: PCB footprints</b> . . . . .  | <b>34</b> |           |                                      |           |
| <b>19</b> | <b>Abbreviations</b> . . . . .  | <b>36</b> |           |                                      |           |

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2012.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 11 September 2012

Document identifier: PCA9555A