DATA SHEET

PCD5002
Advanced POCSAG and APOC-1 Paging Decoder

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Advanced POCSAG and APOC-1 Paging Decoder

PCD5002

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Advanced POCSAG and APOC-1 Paging Decoder

PCD5002

1 FEATURES

- Wide operating supply voltage range: 1.5 to 6.0 V
- EEPROM programming requires only 2.0 V supply
- Low operating current: 50 μA typ. (ON), 25 μA typ. (OFF)
- Temperature range −25 to +70 °C
- *"CCIR radio paging Code No. 1"* (POCSAG) compatible
- Supports Advanced Pager Operator's Code Phase 1 (APOC-1) for extended battery economy
- 512, 1200 and 2400 bits/s data rates using 76.8 kHz crystal
- Built-in data filter (16-times oversampling) and bit clock recovery
- Advanced ACCESS® synchronization algorithm
- 2-bit random and (optional) 4-bit burst error correction
- Up to 6 user addresses (RICs), each with 4 functions/alert cadences
- Up to 6 user address frames, independently programmable
- Standard POCSAG sync word, plus up to 4 user programmable sync words
- Continuous data decoding upon reception of user programmable sync word (optional)
- Received data inversion (optional)
- Call alert via beeper, vibrator or LED
- 2-level acoustic alert using single external transistor
- Alert control: automatic (POCSAG type), via cadence register or alert input pin
- Separate power control of receiver and RF oscillator for battery economy
- Synthesizer set-up and control interface (3-line serial)
- On-chip EEPROM for storage of user addresses (RICs), pager configuration and synthesizer data
- On-chip SRAM buffer for message data
- Slave I^2C-bus interface to microcontroller for transfer of message data, status/control and EEPROM programming (data transfer at up to 100 kbits/s)
- Wake-up interrupt for microcontroller, programmable polarity
- Direct and I^2C-bus control of operating status (ON/OFF)
- Battery-low indication (external detector)
- Out-of-range condition indication
- Real time clock reference output
- On-chip voltage doubler
- Interfaces directly to UAA2080 and UAA2082 paging receivers.

2 APPLICATIONS

- Advanced display pagers (POCSAG and APOC-1)
- Basic alert-only pagers
- Information services
- Personal organizers
- Telepoint
- Telemetry/data transmission.

3 GENERAL DESCRIPTION

The PCD5002 is a very low power pager decoder and controller, capable of handling both standard POCSAG and the advanced APOC-1 code. Continuous data decoding upon reception of a dedicated sync word is available for news pager applications.

Data rates supported are 512, 1200 and 2400 bits/s using a single 76.8 kHz crystal. On-chip EEPROM is programmable using a minimum supply voltage of 2.0 V, allowing 'over-the-air' programming. I^2C-bus compatible.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD5002H	LQFP32	plastic low profile quad flat package; 32 leads; body 7 × 7 × 1.4 mm	SOT358-1
PCD5002U/10	–	film-frame carrier (naked die) 32 pads	–

5 LICENSE

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6 BLOCK DIAGRAM

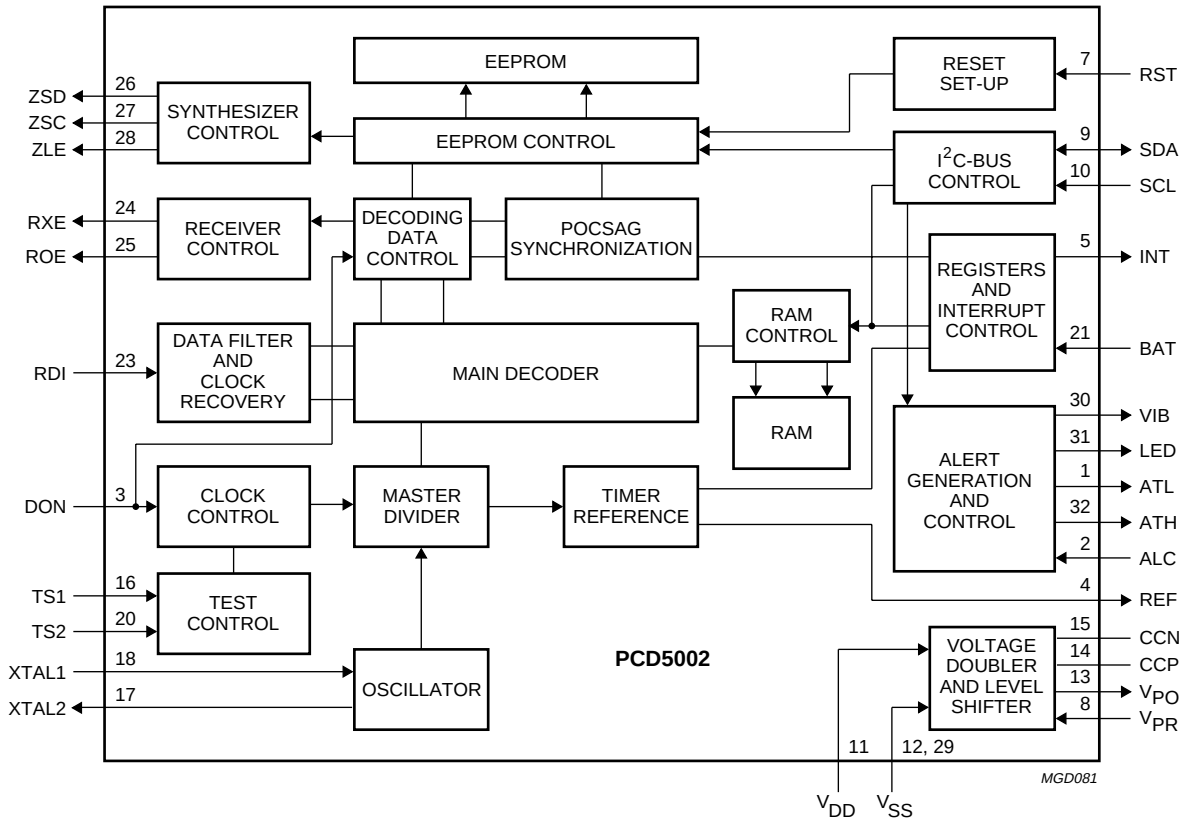


Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN	DESCRIPTION
ATL	1	alert LOW level output
ALC	2	alert control input (normally LOW by internal pull-down)
DON	3	direct ON/OFF input (normally LOW by internal pull-down)
REF	4	real time clock frequency reference output
INT	5	interrupt output
n.c.	6	not connected
RST	7	reset input (normally LOW by internal pull-down)
V_{PR}	8	external positive voltage reference input
SDA	9	I^2C-bus serial data input/output
SCL	10	I^2C-bus serial clock input
V_{DD}	11	main positive supply voltage
V_{SS}	12	main negative supply voltage
V_{PO}	13	voltage converter positive output
CCP	14	voltage converter shunt capacitor (positive side)
CCN	15	voltage converter shunt capacitor (negative side)
TS1	16	test input 1 (normally LOW by internal pull-down)
XTAL2	17	decoder crystal oscillator output
XTAL1	18	decoder crystal oscillator input
n.c.	19	not connected
TS2	20	test input 2 (normally LOW by internal pull-down)
BAT	21	battery sense input
n.c.	22	not connected
RDI	23	received data input (POCSAG or APOC-1)
RXE	24	receiver circuit enable output
ROE	25	receiver oscillator enable output
ZSD	26	synthesizer serial data output
ZSC	27	synthesizer serial clock output
ZLE	28	synthesizer latch enable output
V_{SS}	29	main negative supply voltage
VIB	30	vibrator motor drive output
LED	31	LED drive output
ATH	32	alert HIGH level output

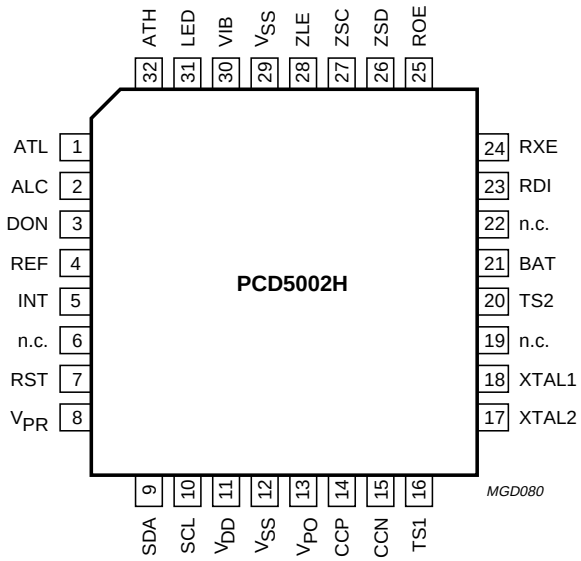


Fig.2 Pin configuration for SOT358-1 (LQFP32).

8 FUNCTIONAL DESCRIPTION

8.1 Introduction

The PCD5002 is a very low power decoder and pager controller specifically designed for use in new generation radio pagers. The architecture of the PCD5002 allows for flexible application in a wide variety of radio pager designs.

The PCD5002 is fully compatible with *"CCIR Radio paging Code No. 1"* (also known as the POCSAG code) operating at data rates of 512, 1200 and 2400 bits/s using a single oscillator crystal of 76.8 kHz.

The PCD5002 also supports the new Advanced Pager Operator's Code Phase 1 (APOC-1). This compatible extension to the POCSAG code improves battery economy by introducing 'cycles' and batch numbering. A cycle consists of 5 or 15 standard POCSAG batches. Each pager will be allocated a batch number in addition to its POCSAG address and it will only search for its address during this batch.

In addition to the standard POCSAG sync word (used also in APOC-1) the PCD5002 is also capable of recognizing up to 4 User Programmable Sync Words (UPSWs). This permits the reception of both private services and POCSAG or APOC-1 transmissions via the same radio channel. As an option reception of a UPSW may activate Continuous Data Decoding (CDD).

Used together with the Philips UAA2080 or UAA2082 paging receiver, the PCD5002 offers a highly sophisticated, miniature solution for the radio paging market. Control of an RF synthesizer circuit is also provided to ease alignment and channel selection.

On-chip EEPROM provides storage for user addresses (Receiver Identity Codes or RICs) and Special Programmed Functions (SPFs) and UPSWs, which eliminates the need for external storage devices and interconnection. For other non-volatile storage 20 bytes of general purpose EEPROM are available. The low EEPROM programming voltage makes the PCD5002 well suited for 'over-the-air' programming/reprogramming.

On request from an external controlling device or automatically (by SPF programming), the PCD5002 will provide standard POCSAG alert cadences by driving a standard acoustic 'beeper'. Non-standard alert cadences may be generated via a cadence register or a dedicated control input.

The PCD5002 can also produce a HIGH level acoustic alert as well as drive an LED indicator and a vibrator motor via external bipolar transistors.

The PCD5002 contains a low-power, high-efficiency voltage converter (doubler) designed to provide a higher voltage supply to LCD drivers or microcontrollers. In addition, an independent level shifted interface is provided allowing communication to a microcontroller operating at a higher voltage than the PCD5002.

Interface to such an external device is provided by an I^2C-bus which allows received call identity and message data, data for the programming of the internal EEPROM, alert control and pager status information to be transferred between the devices. Pager status includes features provided by the PCD5002 such as battery-low and out-of-range indications. A dedicated interrupt line minimizes the required microcontroller activity.

A selectable low frequency timing reference is provided for use in real time clock functions.

Data synchronization is achieved by the Philips patented ACCESS® algorithm ensuring that maximum advantage is made of the POCSAG code structure particularly in fading radio signal conditions. The algorithm allows for data synchronization without preamble detection whilst minimizing battery power consumption. The APOC-1 code uses an extended version of the ACCESS® synchronization algorithm.

Random (and optional) burst error correction techniques are applied to the received data to optimize the call success rate without increasing the falsing rate beyond specified POCSAG levels.

8.2 The POCSAG paging code

A transmission using the *"CCIR Radio paging Code No. 1"* (POCSAG code) is constructed in accordance with the following rules (see Fig.3).

The transmission is started by sending a **preamble**, consisting of at least 576 continuously alternating bits (10101010...). The preamble is followed by an arbitrary number of batch blocks. Only complete batches are transmitted.

Each **batch** comprises 17 codewords of 32 bits each. The first codeword is a synchronization codeword with a fixed pattern. The **sync** word is followed by 8 frames (0 to 7) of 2 codewords each, containing message information. A codeword in a frame can either be an address, message or idle codeword.

Idle codewords also have a fixed pattern and are used to fill empty frames or to separate messages.

Address codewords are identified by an MSB at logic 0 and are coded as shown in Fig.3. A user address or RIC consists of 21 bits. Only the upper 18 bits are encoded in the address codeword (bits 2 to 19). The lower 3 bits designate the frame number (0 to 7) in which the address is transmitted.

Four different call types ('numeric', 'alphanumeric' and two 'alert only' types) can be distinguished. The call type is determined by two function bits in the address codeword (bits 20 and 21), as shown in Table 1.

Alert-only calls consist only of a single address codeword. Numeric and alphanumeric calls have message codewords following the address. A message causes the frame structure to be temporarily suspended. Message codewords are sent until the message is completed, with only the sync words being transmitted in their expected positions.

Message codewords are identified by an MSB at logic 1 and are coded as shown in Fig.3. The message information is stored in a 20-bit field (bits 2 to 21).

The standard data format is determined by the call type: 4 bits per digit for numeric messages and 7 bits per (ASCII) character for alphanumeric messages.

Each codeword is protected against transmission errors by 10 CRC check bits (bits 22 to 31) and an even-parity bit (bit 32). This permits correction of a maximum of 2 random errors or up to 3 errors in a burst of 4 bits (a 4-bit burst error) per codeword.

8.3 The APOC-1 paging code

The APOC-1 paging code is fully POCSAG compatible and involves the introduction of batch grouping and a Batch Zero Identifier. This reserved address codeword indicates the start of a 'cycle' of 5 or 15 batches long and is transmitted immediately after a sync word.

Cycle transmission must be coherent i.e. a transmission starting an integer number of cycle periods after the start of the previous one.

Broadcast message data may be included in a transmission. This information may occupy any number of message codewords and immediately follows the batch zero identifier of the first cycle after preamble.
The presence of data is indicated by the function bits in the batch zero identifier: 1,1 indicates 'no broadcast data'. Any other combination indicates a broadcast message.

The PCD5002 can be configured for POCSAG or APOC-1 operation via SPF programming. The batch zero identifier is programmable and can be stored in any identifier location in EEPROM.

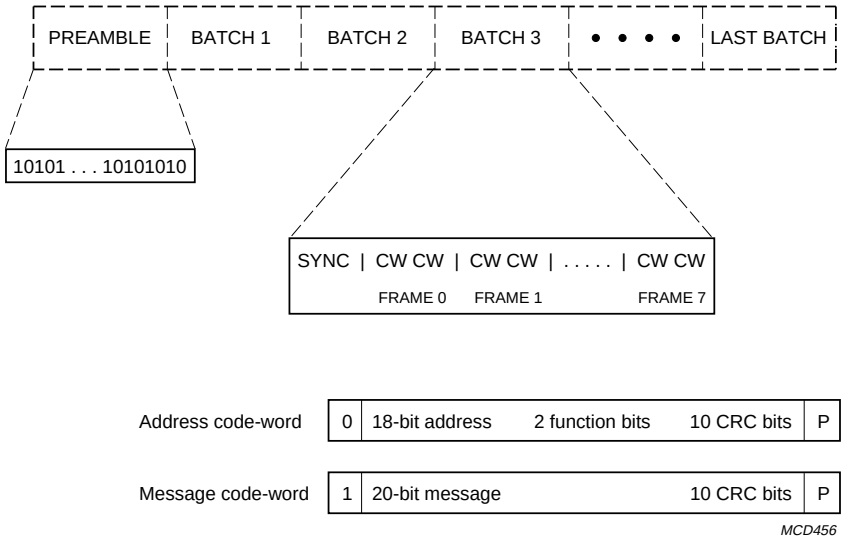


Fig.3 POCSAG code structure.

Table 1 POCSAG recommended call types and function bits

BIT 20 (MSB)	BIT 21 (LSB)	CALL TYPE	DATA FORMAT
0	0	numeric	4-bits per digit
0	1	alert only 1	–
1	0	alert only 2	–
1	1	alphanumeric	7-bits per ASCII character

The POCSAG standard only allows combinations of data formats and function code bits as given in Table 1. However, other (non-standard) combinations will be decoded normally by the PCD5002.

8.4 Error correction

In the PCD5002 error correction methods have been implemented as shown in Table 2.

Random error correction is default for both address and message codewords. In addition, burst error correction can be enabled by SPF programming. Up to 3 erroneous bits in a 4-bit burst can be corrected.

The error type detected for each codeword is identified in the message data output to the microcontroller, allowing rejection of calls with too many errors.

Table 2 Error correction

ITEM	CORRECTION
Preamble	4 random errors in 31 bits
Synchronization codeword	2 random errors in 32 bits
Address codeword	2 random errors, plus 4-bit burst errors (optional)
Message codeword	2 random errors, plus 4-bit burst errors (optional)

8.5 Operating states

The PCD5002 has 2 operating states:

- ON status
- OFF status.

The operating state is determined by a Direct Control input (DON) and bit D4 in the control register (see Table 3).

Table 3 Truth table for decoder operating status

DON INPUT	CONTROL BIT D4	OPERATING STATUS
0	0	OFF
0	1	ON
1	0	ON
1	1	ON

8.6 ON status

In the ON status the decoder pulses the receiver and oscillator enable outputs (RXE and ROE respectively) according to the code structure and the synchronization algorithm. Data received serially at the data input (RDI) is processed for call reception.

The data protocol can be POCSAG or APOC-1. Continuous data decoding upon reception of a special sync word is also supported. The data protocol is selected by SPF programming.

Reception of a valid paging call is signalled to the microcontroller by an interrupt signal. The received address and message data can then be read via the I^2C-bus interface.

8.7 OFF status

In the OFF status the decoder will neither activate the receiver or oscillator enable outputs, nor process any data at the data input. The crystal oscillator remains active to permit communication with the microcontroller.

In both operating states an accurate timing reference is available via the REF output. Using SPF programming the signal periodicity may be selected as 32.768 kHz, 50 Hz, 2 Hz or $1/60$ Hz.

8.8 Reset

The decoder can be reset by applying a positive pulse on input pin RST. For successful reset at power-on, a HIGH level must be present on the RST pin while the device is powering-up.

This can be applied by the microcontroller, or via a suitable RC power-on reset circuit connected to the RST input. Reset circuit details and conditions during and after a reset are described in Chapter 9.

8.9 Bit rates

The PCD5002 can be configured for data rates of 512, 1200 or 2400 bits/s by SPF programming. These data rates are derived from a single 76.8 kHz oscillator frequency.

8.10 Oscillator

The oscillator circuit is designed to operate at 76.8 kHz. Typically, a tuning fork crystal will be used as a frequency source. Alternatively, an external clock signal can be applied to pin XTAL1 (amplitude = V_{DD} to V_{SS}), but a slightly higher oscillator current is consumed. A 2.2 MΩ feedback resistor connected between XTAL1 and XTAL2 is required for proper operation.

To allow easy oscillator adjustment (e.g. by a variable capacitor) a 32.768 kHz reference frequency can be selected at output REF by SPF programming.

8.11 Input data processing

Data input is binary and fully asynchronous. Input bit rates of 512, 1200 and 2400 bits/s are supported. As a programmable option, the polarity of the received data can be inverted before further processing.

The input data is noise filtered by a digital filter. Data is sampled at 16 times the data rate and averaged by majority decision.

The filtered data is used to synchronize an internal clock generator by monitoring transitions. The recovered clock phase can be adjusted in steps of $\frac{1}{8}$ or $\frac{1}{32}$ bit period per received bit.

The larger step size is used when bit synchronization has not been achieved, the smaller when a valid data sequence has been detected (e.g. preamble or sync word).

8.12 Battery saving

Current consumption is reduced by switching off internal decoder sections whenever the receiver is not enabled.

To further increase battery efficiency, reception and decoding of an address codeword is stopped as soon as the uncorrected address field differs by more than 3 bits from the enabled RICs. If the next codeword must be received again, the receiver is re-enabled thus observing the programmed establishment times t_{RXE} and t_{ROE}.

The current consumption of the complete pager can be minimized by separately activating the RF oscillator circuit (using output ROE) before activating the rest of the receiver. This is possible using the UAA2082 receiver which has external biasing for the oscillator circuit.

8.13 POCSAG Synchronization strategy

In the ON status the PCD5002 synchronizes to the POCSAG data stream by the Philips ACCESS® algorithm. A flow diagram is shown in Fig.4. Where ‘sync word’ is used, this implies both the standard POCSAG sync word and any enabled User Programmable Sync Word (UPSW).

Several modes of operation can be distinguished depending on the synchronization state. Each mode uses a different method to obtain or retain data synchronization. The receiver and oscillator enable outputs (RXE and ROE respectively) are switched accordingly, with the appropriate establishment times (t_{RXON} and t_{ROON} respectively).

Before comparing received data with preamble, an enabled sync word or programmed user addresses, the appropriate error correction is applied.

Initially, after switching to the ON status, the decoder is in **switch-on** mode. Here the receiver will be enabled for a period up to 3 batches, testing for preamble and the sync word. Failure to detect preamble or the sync word will cause the device to switch to the ‘carrier off’ mode.

When preamble is detected it will cause the device to switch to the **preamble receive** mode, in which a sync word is searched for. The receiver will remain enabled while preamble is detected. When neither sync word nor preamble is found within a 1 batch duration the ‘carrier off’ mode is entered.

Upon detection of a sync word the **data receive** mode is entered. The receiver is activated only during enabled user address frames and sync word periods. When an enabled user address has been detected, the receiver will be kept enabled for message codeword reception until the call termination criteria are met.

During call reception data bytes are stored in an internal SRAM buffer, capable of storing 2 batches of message data.

Messages are transmitted contiguously, only interrupted by sync words at the beginning of each batch.

When a message extends beyond the end of a batch no testing for sync takes place. Instead, a message data transfer will be initiated by an interrupt to the external controller. Data reception continues normally after a period corresponding to the sync word duration.

If any message codeword is found to be uncorrectable, the 'data fail' mode is entered and no data transfer will be attempted at the next sync word position. Instead, a test for sync word will be carried out.

In the **data fail** mode message reception continues normally for 1 batch duration. When a sync word is detected at the expected position the decoder returns to the 'data receive' mode. If the sync word again fails to appear, then batch synchronization is deemed lost. Call reception is then terminated and the 'fade recovery' mode is entered.

The **fade recovery** mode is intended to scan for sync word and preamble over an extended window (nominal position ± 8 bits). This is performed for a period of up to 15 batches, allowing recovery of synchronization from long fades in the radio signal. Detection of preamble causes switching to the 'preamble receive' mode, while sync word detection causes switching to the 'data receive' mode. When neither is found within a period of 15 batches, the radio signal is considered lost and the 'carrier off' mode is entered.

The purpose of the **carrier off** mode is to detect a valid radio transmission and synchronize to it quickly and efficiently. Because transmissions may start at random, the decoder enables the receiver for 1 codeword in every 18 codewords looking for preamble or sync word.
By using a buffer containing 32 bits (n bits from the current scan, 32 –n from the previous scan) effectively every batch bit position can be tested within a continuous transmission of at least 18 batches. Detection of preamble causes the device to switch to the 'preamble receive' mode, while sync word detection causes the device to switch to the 'data receive' mode.

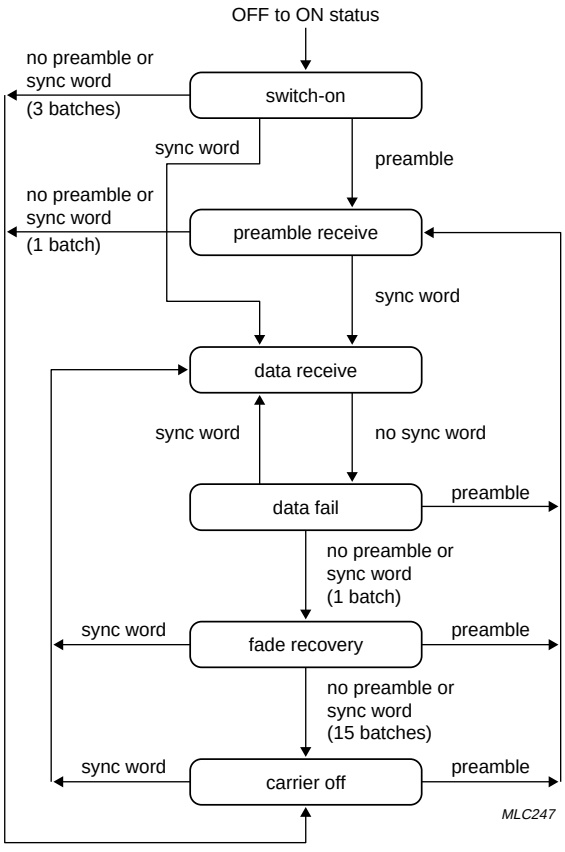


Fig.4 ACCESS® synchronization algorithm for POCSAG.

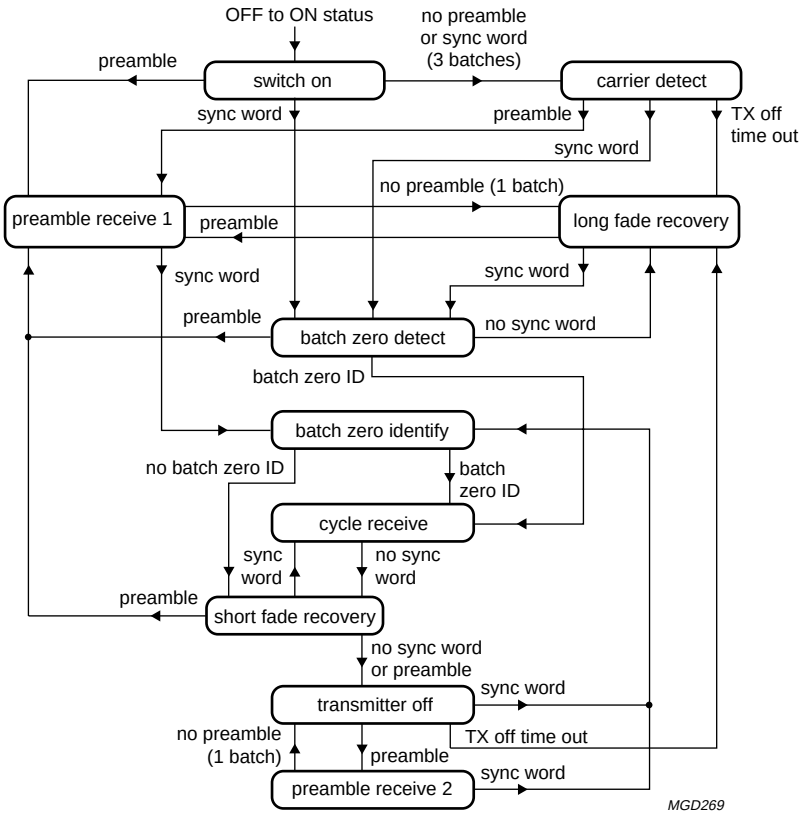


Fig.5 APOC-1 synchronization algorithm.

8.14 APOC-1 synchronization strategy

The synchronization strategy in APOC-1 is an extended version of the ACCESS® scheme and is illustrated in Fig.5. The PCD5002 counts the number of batches in a transmission, starting from the first batch received after preamble. Counter overflow occurs due to the size of a cycle, as determined by SPF programming.

Initially, after switching to the ON status, the decoder will be in the **switch-on** mode. Here the receiver will be enabled for up to 3 batches, testing for preamble and sync word. Detection of preamble causes the device to switch to the ‘preamble receive’ mode, while any enabled sync word enters the ‘batch zero detect’ mode. Failure to detect either will cause the device to switch to the ‘carrier detect’ mode.

In the **preamble receive 1** mode the PCD5002 searches for a sync word, the receiver remaining enabled while preamble is detected. As soon as an enabled sync word is found the ‘batch zero identify’ mode is started.

If preamble is not found within one batch duration then the ‘long fade recovery’ mode is entered.

When in **batch zero detect** mode the PCD5002 switches on every batch to maintain synchronization and check for the batch zero identifier. Detection of the batch zero identifier activates the ‘cycle receive’ mode. When synchronization is lost the ‘long fade recovery’ mode is entered. ‘preamble receive’ mode is entered when preamble is detected.

In the **batch zero identify** mode the first codeword immediately after the sync word of the first batch is compared with the programmed batch zero identifier. Failure to detect the batch zero identifier will cause the device to enter the ‘short fade recovery’ mode.

When this comparison is successful the function bits determine whether any broadcast message will follow. Any function bit combination other than ‘1,1’ will cause the PCD5002 to accept message codewords until terminated by a valid address codeword.

After reception of any broadcast message data the PCD5002 continues to operate in the 'cycle receive' mode.

In the **cycle receive** mode the PCD5002 enables call reception in only one programmed batch per cycle. Sync word detection takes place from 2 bits before to 2 bits after the expected sync word position of this batch. If the sync word is not detected then the position of the current sync word will be maintained and the 'short fade recovery' mode will be entered.

When a valid sync word is found user address codeword detection takes place, as in normal POCSAG code. Any following message codewords are received normally. If a message extends into a subsequent batch containing a batch zero identifier, then the batch zero identifier is detected normally and message reception will continue.

Data reception is suspended after the programmed batch until the same batch position in the next cycle. The exception being when a received call continues into the next batch.

In the **short fade recovery** mode the programmed data receive batch will continue to be checked for user address codewords. In addition the first codeword after the programmed batch is checked for sync word or preamble.

When a valid sync word is detected the 'cycle receive' mode is re-entered, while detection of preamble causes the device to switch to the 'preamble receive' mode. When neither is found then the 'transmitter off' mode is entered.

In the **transmitter off** mode a time-out is set to a pre-programmed duration. This time-out corresponds to the maximum time between subsequent transmissions (preamble to preamble).

The PCD5002 then checks the first batch of every cycle for sync word or preamble. The programmed data receive batch is ignored (unless it is batch 0).

Table 4 Synchronization window tolerance as a function of bit rate

TIME FROM LOSS OF SIGNAL	TOLERANCE		
	512 (bits/s)	1200 (bits/s)	2400 (bits/s)
≤ 30 s	4 bits	4 bits	4 bits
≤ 60 s	4 bits	4 bits	8 bits
≤ 120 s	4 bits	8 bits	16 bits
≤ 240 s	8 bits	16 bits	32 bits

Synchronization checking is performed over a window ranging from 'n' bits before to 'n' bits after the expected sync word position. The window tolerance 'n' depends on the time since the 'transmitter off' mode was entered and on the selected bit rate (see Table 4).

When a sync word is detected in this widened synchronization window the PCD5002 enters the 'batch zero identify' mode. Time-out expiry before a sync word has been detected causes the device to switch to the 'long fade recovery' mode.

Detection of preamble in the 'transmitter off' mode initiates the **preamble receive 2** mode. Operation in this mode is identical to 'preamble receive mode. Failure to detect preamble for one batch period will cause the device to switch back to the 'transmitter off' mode. This prevents inadvertent loss of cycle synchronization due to spurious signals resembling preamble.

The **carrier detect** mode is identical to the 'carrier off' mode in standard POCSAG operation. Upon first entry the transmitter off time-out is started. The receiver is enabled to receive one codeword in every 18 codewords to check for sync word and preamble. This check is performed on the last available 32 bits for every received bit.

The 'preamble receive' mode is entered if preamble is detected. If a valid sync word is found the 'batch zero detect' mode is entered. If neither has been detected and the time-out expires, then the 'long fade recovery' mode is entered.

The **long fade recovery** mode is intended to quickly regain synchronization in fading conditions (not caused by the transmitter switching off between transmissions) or when having been out of range, while maintaining acceptable battery economy.

Initially, the receiver is switched off until one cycle duration after the last enabling in the 'transmitter off' mode. The receiver is then enabled for a 2 codeword period in which each contiguous group of 32 bits is tested for **any decodable** POCSAG codeword (including sync word) and preamble. Single-bit error correction is applied.

If a codeword is detected, the receiver enable period is extended by another codeword duration and the above test is repeated. This process continues while valid codewords are received.

Detection of preamble will cause the device to switch to the 'preamble receive' mode, while sync word detection will cause the device to switch to the 'batch zero detect' mode. When neither is detected during the 2 codeword window or any following 32-bit group, the receiver will be disabled.

If valid codewords are detected but no sync word or preamble is detected over a period of 18 codewords, the receiver is also disabled.

Data sampling, as previously described, is repeated one cycle duration after the moment the receiver was last activated.

8.15 Call termination

Call reception is terminated:

- Upon reception of any address codeword (including Idle codeword but excluding the batch zero identifier in APOC-1 operation) requiring no more than single bit error correction
- In ‘data fail’ mode, when a sync word is not detected at the expected batch position
- When a forced call termination command is received from an external controller.

The last method permits an external controller to stop call reception, depending on the number and type of errors which occurred in a call. After a forced call termination the decoder will enter the ‘data fail’ mode.

The type of error correction as well as the call termination conditions are indicated by status bits in the message data output.

Following call termination, transfer of the data received since the previous sync word period is initiated by an interrupt to the external controller.

8.16 Call data output format

POCSAG call information is stored in the decoder SRAM in blocks of 3 bytes per codeword. Each stored call consists of a call header, followed by message data blocks and a call terminator. In the event of concatenated messages the call terminator is replaced with the call header of the next message. An alert-only call only has a call header and a call terminator.

The formats of a call header, a message data block and a call terminator are shown in Tables 5, 7 and 9.

A **Call Header** contains information on the last sync word received, the RIC which began call reception and the type of error correction performed on the address codeword.

A **Message Data** block contains the data bits from a message codeword plus the type of error correction performed. No deformatting is performed on the data bits: numeric data appear as 4-bit groups per digit, alphanumeric data has a 7-bit ASCII representation.

The **Call Terminator** contains information on the last sync word received, information on the way the call was terminated (forced call termination command, loss of sync word in ‘data fail’ mode) and the type of error correction performed on the terminating codeword.

8.17 Error type indication

Table 11 shows how the different types of detected errors are encoded in the call data output format.

A message codeword containing more than a single bit error (bit E3 = 1) may appear as an address codeword (bit M1 = 0) after error correction. In this event the codeword is processed as message data and does not cause call termination.

8.18 Data transfer

Data transfer is initiated either during sync word periods or as soon as the receiver is disabled after call termination. If the SRAM buffer is full, data transfer is initiated immediately during the next codeword.

When the PCD5002 is ready to transfer received call data an external interrupt will be generated via output INT. Any message data can be read by accessing the RAM output register via the I^2C-bus interface. Bytes will be output starting from the position indicated by the RAM read pointer.

Table 5 Call header format

BYTE NUMBER	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	0	S3	S2	S1	R3	R2	R1	DF
2	0	S3	S2	S1	R3	R2	R1	0
3	X	X	F0	F1	E3	E2	E1	0

Table 6 Call header bit identification

BITS (MSB to LSB)	IDENTIFICATION
S3 to S1	identifier number of sync word for current batch (7 = standard POCSAG)
R3 to R1	identifier number of user address (RIC)
DF	data fail mode indication (1 = data fail mode); note 1
F0 and F1	function bits of received address codeword (bits 20 and 21)
E3 to E1	detected error type; see Table 11; E3 = 0 in a concatenated call header

Note

1. The DF bit in the call header is set:
   a) When the sync word of the batch in which the (beginning of the) call was received, did not match the standard POCSAG or a user-programmed sync word. The sync word identifier (bits S3 to S1) will then be made 0.
   b) When any codeword of a previous call received in the same batch was uncorrectable.

Table 7 Message data format

BYTE NUMBER	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	M2	M3	M4	M5	M6	M7	M8	M9
2	M10	M11	M12	M13	M14	M15	M16	M17
3	M18	M19	M20	M21	E3	E2	E1	M1

Table 8 Message data bit identification

BITS (MSB to LSB)	IDENTIFICATION
M2 to M21	message codeword data bits
E3 to E1	detected error type; see Table 11
M1	message codeword flag

Table 9 Call terminator format

BYTE NUMBER	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	FT	S3	S2	S1	0	0	0	DF
2	FT	S3	S2	S1	0	0	0	X
3	X	X	X	X	E3	E2	E1	0

Table 10 Call terminator bit identification

BITS (MSB to LSB)	IDENTIFICATION
FT	forced call termination (1 = yes)
S3 to S1	identifier number of last sync word
DF	data fail mode indication (1 = data fail mode); note 1
F0 and F1	function bits of received address codeword (bits 20 and 21)
E3 to E1	detected error type; see Table 11; E3 = 0 in a call terminator

Note

1. The DF bit in the call terminator is set:
   a) When any call data codeword in the terminating batch was uncorrectable, while in ‘data receive’ mode.
   b) When the sync word at the start of the terminating batch did not match the standard POCSAG or a user-programmed sync word, while in ‘data fail’ mode.

Table 11 Error type identification (note 1)

E3	E2	E1	ERROR TYPE	NUMBER OF ERRORS
0	0	0	no errors - correct codeword	0
0	0	1	parity bit in error	1
0	1	0	single bit error	1 + parity
0	1	1	single bit error and parity error	1
1	0	0	not used	–
1	0	1	4-bit burst error and parity error	3 (e.g.1101)
1	1	0	2-bit random error	2
1	1	1	uncorrectable codeword	3 or more

Note

1. POCSAG code allows a maximum of 3 bit errors to be detected per codeword.

Successful call termination occurs on reception of a valid address codeword with less than 2 bit errors. Unsuccessful termination occurs when a sync word is not detected while in the ‘data fail’ mode.

It is generally possible to distinguish these two conditions using the sync word identifier number (bits S3 to S1); the identifier number will be non-zero for correct termination, and zero for sync word failure.

Only when a call is received in the ‘data fail’ mode and the call is terminated before the end of the batch, is it not possible to distinguish unsuccessful from successful termination.

Reception of message data can be terminated at any time by transmitting a forced call termination command to the status register via the I^2C-bus. Any call received will then be terminated immediately and the ‘data fail’ mode will be entered.

8.19 Continuous data decoding

Apart from transmissions in the POCSAG or APOC-1 format, the PCD5002 is also capable of decoding continuous transmissions with the same codeword structure. Any user-programmable sync word (UPSW) may be designated to enable continuous data decoding.

When a Continuous Data Decoding (CDD) sync word is detected at any sync word position, the receiver remains enabled from then on. Status bits D1 and D0 show the CDD mode to be active.

All codewords are decoded and their data fields are stored in SRAM. The usual error information is appended. No distinction is made between address and message codewords: codeword bit 0 is treated as a data bit and is stored in bit M1 of the 3-byte output format.

Codewords received at the expected sync word positions (POCSAG batch size) are matched against standard POCSAG sync word, all enabled UPSWs and preamble.

Data output to an external controller is initiated by an interrupt at the next sync word position, after reception of 16 codewords.

The call header preceding the data has a different structure from normal POCSAG or APOC-1 data. The data header format is shown in Table 12.

Continuous data decoding continues until one of the following conditions occur:

- The decoder is switched to the OFF state
- A Forced Call Termination (FCT) command is received via the I^2C-bus
- Preamble is detected at the sync word position
- Standard POCSAG sync word or an enabled non-CDD sync word is detected.

Only a forced call termination command will be indicated in the SRAM data by a call terminator. In the other events continuous data decoding will stop without notification.

Upon forced termination the ‘fade recovery’ mode is entered. Detection of preamble causes the device to switch to the ‘preamble receive’ mode. Detection of a standard sync word or any enabled non-continuous UPSW will cause the device to switch to the ‘data receive’ mode.

Continuous data decoding will continue in the next batch if any enabled CDD sync word is detected or no enabled sync word is detected.

8.20 Receiver and oscillator control

A paging receiver and an RF oscillator circuit can be controlled independently via enable outputs RXE and ROE respectively. Their operating periods are optimized according to the synchronization mode of the decoder. Each enable signal has its own programmable establishment time (see Table 14).

8.21 External receiver control and monitoring

An external controller may enable the receiver control outputs continuously via an I^2C-bus command, overruling the normal enable pattern. Data reception continues normally. This mode can be exited by means of a reset or an I^2C-bus command.

External monitoring of the receiver control output RXE is possible via bit D6 in the status register, when enabled via the control register (D2 = 1). Each change of state of output RXE will generate an external interrupt at output INT.

Table 12 Continuous data header format

BYTE NUMBER	BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
1	0	X	X	X	C3	C2	C1	0
2	0	C3	C2	C1	C3	C2	C1	0
3	X	X	F0	F1	E3	E2	E1	0

Table 13 Data header bit identification

BITS (MSB to LSB)	IDENTIFICATION
C3 to C1	identifier number of continuous data decoding sync word
F0 and F1	function bits of received address codeword (bits 20 and 21)
E3 to E1	detected error type (see Table 11); E3 = 0 in a concatenated call header

8.22 Battery condition input

A logic signal from an external sense circuit, signalling battery condition, can be applied to the BAT input. This input is sampled each time the receiver is disabled (RXE ↓ 0).

When enabled via the control register (D2 = 0), the condition of input BAT is reflected in bit D6 of the status register. Each change of state of bit D6 causes an external interrupt at output INT.

When using the UAA2080 pager receiver a battery-low condition corresponds to a logic HIGH level. With a different sense circuit the reverse polarity can be used as well, because every change of state is signalled to an external controller.

After a reset the initial condition of the battery-low indicator in the status register is zero.

Table 14 Receiver and oscillator establishment times (note 1)

CONTROL OUTPUT	ESTABLISHMENT TIME				UNIT
RXE	5	10	15	30	ms
ROE	20	30	40	50	ms

Note

1. The exact values may differ slightly from the above values, depending on the bit rate (see Table 25).

8.23 Synthesizer control

Control of an external frequency synthesizer is possible via a dedicated 3-line serial interface (outputs ZSD, ZSC and ZLE). This interface is common to a number of available synthesizers. The synthesizer is enabled using the oscillator enable output ROE.

The frequency parameters must be programmed in EEPROM. Two blocks of maximum 24 bits each can be stored. Any unused bits must be programmed at the beginning of a block: only the last bits are used by the synthesizer.

When the function is selected by SPF programming (SPF byte 01, bit D6), data is transferred to the synthesizer each time the PCD5002 is switched from the OFF to the ON status. Transfer takes place serially in two blocks, starting with bit 0 (MSB) of block 1 (see Table 28).

Data bits on ZSD change on the falling edges of ZSC. After clocking all bits into the synthesizer, a latch enable pulse copies the data to the internal divider registers. A timing diagram is illustrated in Fig.6.

The data output timing is synchronous, but has a pause in the bitstream of each block. This pause occurs in the 13th bit while ZSC is LOW. The nominal pause duration t_p depends on the programmed bit rate for data reception and is shown in Table 15. The total duration of the 13th bit is given by $t_{ZCL} + t_p$.

A similar pause occurs between the first and the second data block. The delay between the first latch enable pulse and the second data block is given by $t_{ZDL2} + t_p$.
The complete start-up timing of the synthesizer interface is illustrated in Fig.13.

Table 15 Synthesizer programming pause

BIT RATE (bit/s)	t_p (clocks)	t_p (μs)
512	119	1549
1200	33	430
2400	1	13

8.24 Serial microcontroller interface

The PCD5002 has an I²C-bus serial microcontroller interface capable of operating at 400 kbits/s.
The PCD5002 is a slave transceiver with a 7-bit I²C-bus address 39 (bits A6 to A0 = 0100111).

Data transmission requires 2 lines: SDA (data) and SCL (clock), each with an external pull-up resistor. The clock signal (SCL) for any data transmission must be generated by the external controlling device.

A transmission is initiated by a START condition (S: SCL = 1, SDA = ↓) and terminated by a STOP condition (P: SCL = 1, SDA = ↑).

Data bits must be stable when SCL is HIGH. If there are multiple transmissions, the STOP condition can be replaced with a new START condition.

Data is transferred on a byte basis, starting with a device address and a read/write indicator. Each transmitted byte must be followed by an acknowledge bit A (active LOW). If a receiving device is not ready to accept the next complete byte, it can force a bus wait state by holding SCL LOW.

The general I²C-bus transmission format is illustrated in Fig.7. Formats for master/slave communication are illustrated in Fig.8.

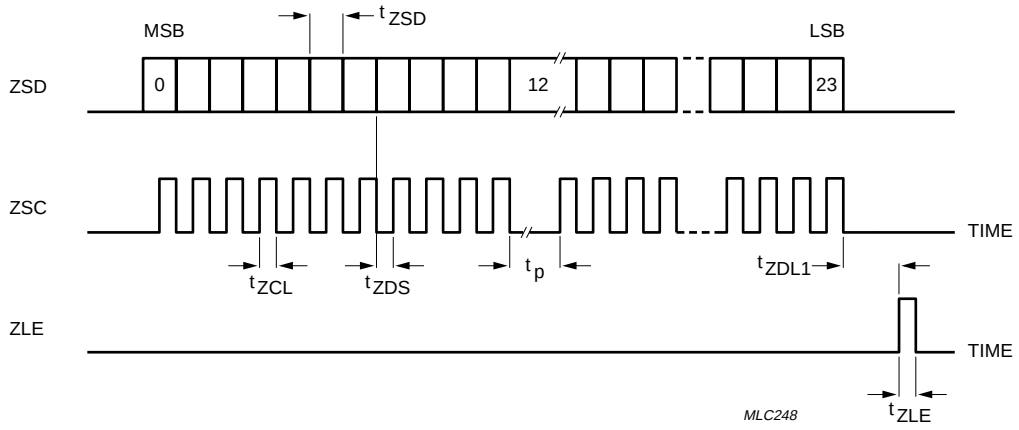


Fig.6 Synthesizer interface timing.

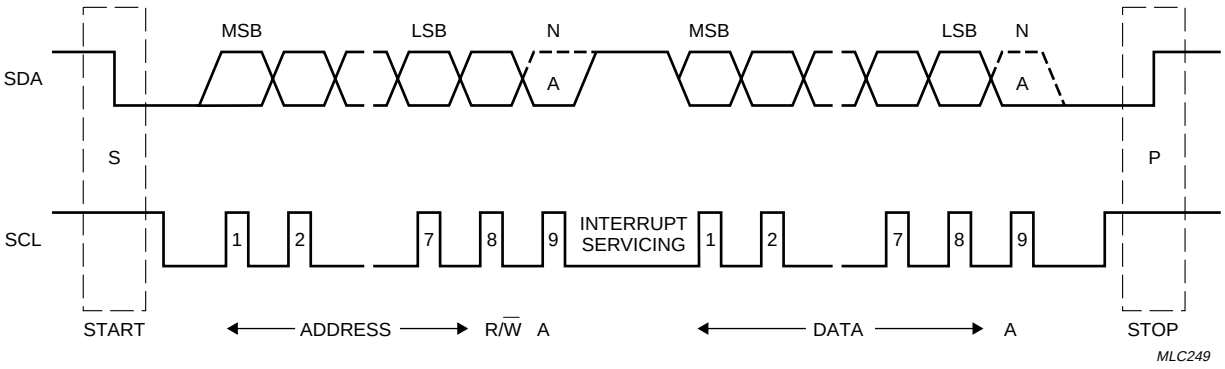
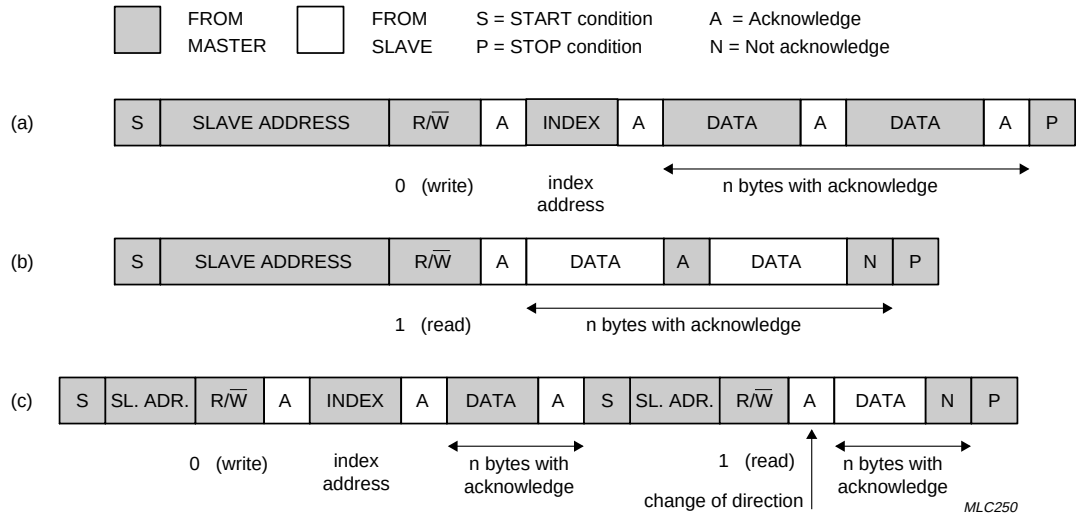


Fig.7 I²C-bus message format.



(a) Master writes to slave.
(b) Master reads from slave.
(c) Combined format (shown: write plus read).

Fig.8 Message types.

8.25 Decoder I²C-bus access

All internal access to the PCD5002 takes place via the I²C-bus interface. For this purpose the internal registers, SRAM and EEPROM have been memory mapped and are accessed via an **index register**. Table 16 shows the index addresses of all internal blocks.

Registers are addressed directly, while RAM and EEPROM are addressed indirectly via address pointers and I/O registers.

Remark: The EEPROM memory map is non-contiguous and is organized as a matrix.
The EEPROM address pointer contains both row and column indicators.

Data written to read-only bits will be ignored. Values read from write-only bits are undefined and must be ignored.

Each I²C-bus write message to the PCD5002 must start with its slave address, followed by the index address of the memory element to be accessed. An I²C-bus read message uses the last written index address as a data source. The different I²C-bus message types are shown in Fig.8.

As a slave the PCD5002 cannot initiate bus transfers by itself. To prevent an external controller from having to monitor the operating status of the decoder, all important events generate an external interrupt on output INT.

Table 16 Index register

ADDRESS(1)	REGISTER FUNCTION	ACCESS
00H	status	R
00H	control	W
01H	real time clock: seconds	R/$\overline{W}$
02H	real time clock: $^1/_{100}$ second	R/$\overline{W}$
03H	alert cadence	W
04H	alert set-up	W
05H	periodic interrupt modulus	W
05H	periodic interrupt counter	R
06H	RAM write address pointer	R
07H	EEPROM address pointer	R/$\overline{W}$
08H	RAM read address pointer	R/$\overline{W}$
09H	RAM data output	R
0AH	EEPROM data input/output	R/$\overline{W}$
0BH to 0FH	unused	note 2

Notes

1. The index register only uses the least significant nibble, the upper 4 bits are ignored.
2. Writing to registers 0B to 0F has no effect, reading produces meaningless data.

8.26 External interrupt

The PCD5002 can signal events to an external controller via an interrupt signal at output INT. The interrupt polarity is programmable via SPF programming. The interrupt source is shown in the status register.

Interrupts are generated by the following events (more than one event is possible):

- Call data available for output (bit D2)
- SRAM pointers becoming equal (bit D3)
- Expiry of periodic time-out (bit D7)
- Expiry of alert time-out (bit D4)
- Change of state in out-of-range indicator (bit D5)
- Change of state in battery-low indicator or in receiver control output RXE (bit D6).

Immediate interrupts are generated by status bits D3, D4, D6 (RXE monitoring) and D7. Bits D2, D5 and D6 (BAT monitoring) generate interrupts as soon as the receiver is disabled (RXE = 0).

When call data is available (D2 = 1) but the receiver remains switched on, an interrupt is generated at the next sync word position.

The interrupt output INT is reset after completion of a status read operation.

8.27 Status/Control register

The status/control register consists of two independent registers, one for reading (status) and one for writing (control).

The status register shows the current operating condition of the decoder and the cause(s) of an external interrupt. The control register activates/deactivates certain functions. Tables 17 and 18 show the bit allocations of both registers.

All status bits will be reset after a status read operation except for the out-of-range, battery-low and receiver enable indicator bits (see note 1 to Table 17).

Table 17 Status register (00H; read)

BIT[1]	VALUE	DESCRIPTION
D1 and D0	0 0	no new call data
	0 1	new call received (POCSAG or APOC-1)
	1 0	continuous decoding data available
	1 1	batch zero data available (APOC-1)
D3 and D2	0 0	no data to be read (default after reset)
	0 1	RAM read/write pointers different; data to be read
	1 0	RAM read/write pointers equal; no more data to read
	1 1	RAM buffer full or overflow
D4	1	alert time-out expired
D5	1	out-of-range
D6	1	BAT input HIGH or RXE output active (selected by control bit D2)
D7	1	periodic timer interrupt

Note

1. After a status read operation bits D3, D4 and D7 are always reset, bits D1 and D0 only when no second call is pending. D2 is reset when the RAM is empty (read and write pointers equal).

Table 18 Control register (00H; write)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	1	forced call termination (automatically reset after termination)
D1	1	EEPROM programming enable
D2	0	BAT input selected for monitoring (status bit D6)
	1	RXE output selected for monitoring (status bit D6)
D3	1	receiver continuously enabled (RXE = 1, ROE = 1)
D4	0	decoder in OFF status (while DON = 0)
	1	decoder in ON status
D5 to D7	X	not used: ignored when written

8.28 Pending interrupts

A secondary status register is used for storing status bits of pending interrupts. This occurs:

- When a new call is received while the previous one was not yet acknowledged by reading the status register
- When an interrupt occurs during a status read operation.

After completion of the status read the primary register is loaded with the contents of the secondary register, which is then reset. An immediate interrupt is then generated, output INT becoming active 1 decoder clock cycle after it was reset following the status read.

Remark: In the event of multiple pending calls, only the status bits of the last call are retained.

8.29 Out-of-range indication

The out-of-range condition occurs when entering the ‘fade recovery’ or ‘carrier off’ mode in POCSAG, or ‘transmitter off’ or ‘carrier detect’ mode in APOC-1. This condition is reflected in bit D5 of the status register. The out-of-range condition is reset when either preamble or a valid sync word is detected.

The out-of-range bit (D5) in the status register is updated each time the receiver is disabled (RXE $\downarrow$ 0). Every change of state in bit D5 generates an interrupt.

8.30 Real time clock

The PCD5002 provides a periodic reference pulse at output REF. The frequency of this signal can be selected by SPF programming:

- 32768 Hz
- 50 Hz (square-wave)
- 2 Hz
- $^1/_{60}$ Hz.

The 32768 Hz signal does not have a fixed period, it consists of 32 pulses distributed over 75 main oscillator cycles at 76.8 kHz. The timing is illustrated in Fig.15.

When programmed for $^1/_{60}$ Hz (1 pulse per minute) the pulse at output REF is held off while the receiver is enabled.

Except for the 50 Hz frequency the pulse width t_{RFP} is equal to one decoder clock period.

The real time clock counter runs continuously irrespective of the operating condition of the PCD5002. It contains a **seconds register** (maximum 59) and a **$^1/_{100}$ second register** (maximum 99), which can be read from or written to via the I²C-bus. The bit allocation of both registers is shown in Tables 19 and 20.

Table 19 Real time clock; seconds register (01H; read/write)

BIT (MSB D7)	VALUE	DESCRIPTION
D0	–	1 s
D1	–	2 s
D2	–	4 s
D3	–	8 s
D4	–	16 s
D5	–	32 s
D6	X	not used: ignored when written, undetermined when read
D7	X	not used: ignored when written, undetermined when read

Table 20 Real time clock; $^1/_{100}$ second register (02H; read/write)

BIT (MSB D7)	VALUE	DESCRIPTION
D0	–	0 01 s
D1	–	0.02 s
D2	–	0.04 s
D3	–	0.08 s
D4	–	0.16 s
D5	–	0.32 s
D6	–	0.64 s
D7	X	not used: ignored when written, undetermined when read

8.31 Periodic interrupt

A periodic interrupt can be realised with the periodic interrupt counter. This 8-bit counter is incremented every $^1/_{100}$ s and produces an interrupt when it reaches the value stored in the periodic interrupt modulus register.
The counter register is then reset and counting continues.

Operation is started by writing a non-zero value to the modulus register. Writing a zero will stop interrupt generation immediately and will halt the periodic interrupt counter after 2.55 s.

The modulus register is write-only, the counter register is read only. Both registers have the same index address (05H).

8.32 Received call delay

Call reception (detection of an enabled RIC) causes both the periodic interrupt modulus and the counter register to be reset.

Since the periodic interrupt counter runs for another 2.55 s after a reset, the received call delay (in $^1/_{100}$ s units) can be determined by reading the counter register.

Table 21 Alert set-up register (04H; write)

BIT (MSB D7)	VALUE	DESCRIPTION
D0	0	call alert via cadence register
	1	POCSAG call alert (pattern selected by D7 and D6)
D1	0	LOW level acoustic alert (ATL), pulsed vibrator alert (25 Hz)
	1	HIGH level acoustic alert (ATL + ATH), continuous vibrator alert
D2	0	normal alerts (acoustic and LED)
	1	warbled alerts: 16 Hz (LED: on/off, ATL/ATH: alternate f_{AWH}, f_{AWL})
D3	1	acoustic alerts enable (ATL, ATH)
D4	1	vibrator alert enabled (VIB)
D5	1	LED alert enabled (LED)
D7 and D6[1]	0 0	POCSAG alert pattern FC = 00, see Fig.9 (a)
	0 1	POCSAG alert pattern FC = 01, see Fig.9 (b)
	1 0	POCSAG alert pattern FC = 10, see Fig.9 (c)
	1 1	POCSAG alert pattern FC = 11, see Fig.9 (d)

Note

1. Bits D7 and D6 correspond to function bits 20 and 21 respectively in the address codeword, which designate the POCSAG call type as shown in Table 1.

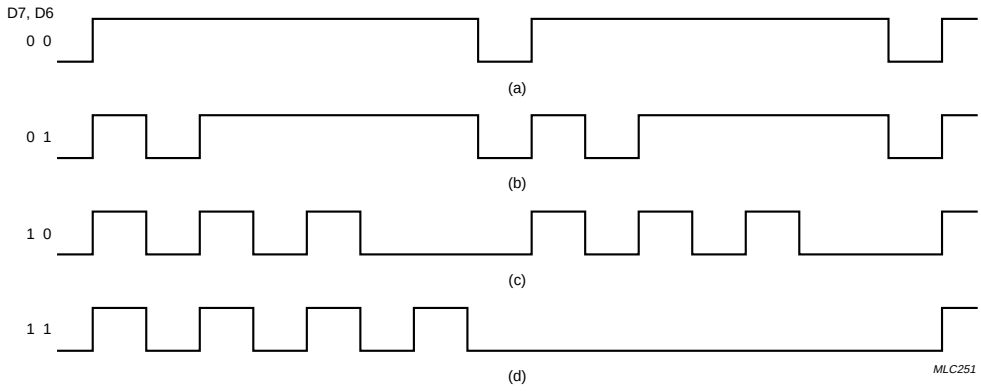


Fig.9 POCSAG alert patterns.

8.33 Alert generation

The PCD5002 is capable of controlling 3 different alert transducers, acoustic beeper (HIGH and LOW level), LED and vibrator motor. The associated outputs are ATH/ATL, LED and VIB respectively. ATL is an open-drain output capable of directly driving an acoustic alerter via a resistor. The other outputs require external transistors.

Each alert output can be individually enabled via the alert set-up register. Alert level and warble can be separately selected. The alert pattern can either be standard POCSAG or determined via the alert cadence register. Direct alert control is possible via input ALC.

The alert set-up register is shown in Table 21.

Standard POCSAG alerts can be selected by setting bit D0 in the alert set-up register, bits D6 and D7 determining the alert pattern used.

8.34 Alert cadence register (03H; write)

When not programmed for POCSAG alerts (alert set-up register bit D0 = 0), the 8-bit alert cadence register determines the alert pattern. Each bit represents a 62.5 ms time slot, a logic 1 activating the enabled alert transducers. The bit pattern is rotated with the MSB (bit D7) being output first and the LSB (bit D0) last.

When the last time slot (bit D0) is initiated an interrupt is generated to allow loading of a new pattern. When the pattern is not changed it will be repeated. Writing a zero to the alert cadence register will halt alert generation within 62.5 ms.

8.35 Acoustic alert

Acoustic alerts are generated via outputs ATL and ATH. For LOW level alerts only ATL is active, while for HIGH level alerts ATH is also active. ATL is driven in counter phase with ATH.

The alert level is controlled by bit D1 in the alert set-up register.

When D1 is reset, for standard POCSAG alerts (D0 = 1) a LOW level acoustic alert is generated during the first 4 s (ATL), followed by 12 s at HIGH level (ATL + ATH). When D1 is set, the full 16 s are at HIGH level. An interrupt is generated after the full alert time has elapsed (indicated by bit D4 in the status register).

When using the alert cadence register, D1 would normally be updated by external control when the alert time-out interrupt occurs at the start of the 8th cadence time slot. Since D1 acts immediately on the alert level, it is advisable to reset the last bit of the previous pattern to prevent unwanted audible level changes.

8.36 Vibrator alert

The vibrator output (VIB) is activated continuously during a standard POCSAG alert or whenever the alert cadence register is non-zero.

Two alert levels are supported, LOW level (25 Hz square-wave) and HIGH level (continuous). The vibrator level is controlled by bit D1 in the alert set-up register.

8.37 LED alert

The LED output pattern corresponds either to the selected POCSAG alert or to the contents of the alert cadence register. No equivalent exists for HIGH/LOW level alerts.

8.38 Warbled alert

When enabled, by setting bit D2 in the alert set-up register, the signals on outputs ATL, ATH and LED are warbled with a 16 Hz modulation frequency. Output LED is switched on and off at the modulation rate, while outputs ATL and ATH switch between f_{AWH} and f_{AWL} alerter frequencies.

8.39 Direct alert control

A direct alert control input (ALC) is available for generating user alarm signals (e.g. battery-low warning). A HIGH level on input ALC activates all enabled alert outputs, overruling any ongoing alert patterns.

8.40 Alert priority

Generation of a standard POCSAG alert (D0 = 1) overrides any alert pattern in the alert cadence register. After completion of the standard alert, the original cadence is restarted from its last position. The alert set-up register will now contain the settings for the standard alert.

The highest priority has been assigned to the alert control input (ALC). All enabled alert outputs will be activated while ALC is set. Outputs are activated/deactivated in synchrony with the decoder clock. Activation requires an extra delay of 1 clock when no alerts are being generated.

When input ALC is reset, acoustic alerting does not cease until the current output frequency cycle has been completed.

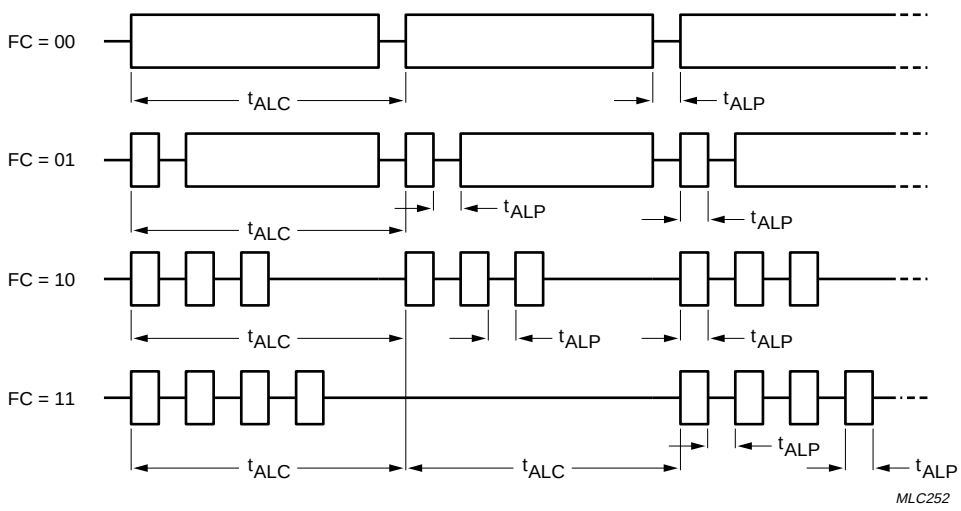


Fig.10 POCSAG alert timing.

8.41 Cancelling alerts

Standard POCSAG alerts (manual or automatic) are cancelled by resetting bit D0 in the alert set-up register. User defined alerts are cancelled by writing a zero to the alert cadence register. Any ongoing alert is cancelled when a reset pulse is applied to input RST.

8.42 Automatic POCSAG alerts

Standard alert patterns have been defined for each POCSAG call type, as indicated by the function bits in the address codeword (see Table 1). The timing of these alert patterns is shown in Fig.10. After completion of the full 16 s alert period an interrupt is generated by status bit D4.

When enabled by SPF programming (SPF byte 03, bit D2) standard POCSAG alerts will be automatically generated at outputs ATL, ATH, LED and VIB upon call reception. The alert pattern matches the call type as indicated by the function bits in the received address codeword.

The original settings of the alert set-up register will be lost. Bit D0 is reset after completion of the alert.

8.43 SRAM access

The on-chip SRAM can hold up to 96 bytes of call data. Each call consists of a call header (3 bytes), message data blocks (3 bytes per codeword) and a call terminator (3 bytes).

The RAM is filled by the decoder and can be read via the I^2C-bus interface. The RAM is accessed indirectly by a read address pointer and a data output register. A write address pointer indicates the position of the last message byte stored.

Status register bit D2 is set when the read and write pointers are different. It is reset only when the SRAM pointers become equal during reading, i.e. when the RAM becomes empty.

Status bit D3 is set when the read and write pointers become equal. This can be due to a RAM empty or a RAM full condition. It is reset after a status read operation.

Interrupts are generated as follows:

- When status bit D2 is set and the receiver is disabled (RXE = 0); data is available for reading
- Immediately when status bit D3 is set: RAM is either empty (status bit D2 = 0) or full (status bit D2 = 1).

To avoid loss of data due to RAM overflow at least 3 bytes of data must be read during reception of the codeword following the ‘RAM full’ interrupt.

8.44 RAM write address pointer (06H; read)

The RAM write address pointer is automatically incremented during call reception, because the decoder writes each data byte to RAM. The RAM write address pointer can only be read. Values range from 00H to 5FH. Bit D7 (MSB) is not used and its value is undefined when read. When a call data byte is written to location 5FH, the write address pointer wraps around to 00H. This does not necessarily imply a RAM full condition.

8.45 RAM read address pointer (08H; read/write)

The RAM read address pointer is automatically incremented after reading a data byte via the RAM output register.

The RAM read address pointer can be accessed for reading and writing.

The values range from 00H to 5FH. When at 5FH a read operation will cause wrapping around to 00H. Bit D7 (MSB) is not used; it is ignored when written to and undefined when read from.

8.46 RAM data output register (09H; read)

The RAM data output register contains the byte addressed by the RAM read address pointer and can only be read. Each read operation causes an increment of the RAM read address pointer.

8.47 EEPROM access

The EEPROM is intended for storage of user addresses (RICs), sync words and special programmed function (SPF) bits representing the decoder configuration.

The EEPROM can store 48 bytes of information and is organized as a matrix of 8 rows by 6 columns.
The EEPROM is accessed indirectly via an address pointer and a data I/O register.

The EEPROM is protected against inadvertent writing by means of the programming enable bit in the control register (bit D1).

The EEPROM memory map is non-contiguous. Figure 11 shows both the EEPROM organization and the access method.

Identifier locations contain RICs or sync words. A total of 20 unassigned bytes are available for general purpose storage.

8.48 EEPROM address pointer (07H; read/write)

An EEPROM location is addressed via the EEPROM address pointer. It is incremented automatically each time a byte is read from or written to via the EEPROM data I/O register.

The EEPROM address pointer contains two counters for the row and the column number. Bits D2 to D0 contain the column number (0 to 5) and bits D5 to D3 the row number (0 to 7). Bits D7 and D6 of the address pointer are not used. Data written to these bits will be ignored, while their values are undefined when read.

The column and row counters are connected in series. Upon overflow of the column counter (column = 5) the row counter is automatically incremented and the column counter wraps to 0. On overflow the row counter wraps from 7 to 0.

8.49 EEPROM data I/O register (0AH; read/write)

The byte addressed by the EEPROM address pointer can be written to or read from via the EEPROM data I/O register. Each access automatically increments the EEPROM address pointer.

8.50 EEPROM access limitations

Since the EEPROM address pointer is used during data decoding, the EEPROM may not be accessed while the receiver is active (RXE = 1). It is advisable to switch to the OFF state before accessing the EEPROM.

The EEPROM cannot be written to unless the EEPROM programming enable bit (bit D1) in the control register is set.

For writing a minimum programmed supply voltage (V_{PG}) is required (2.0 V typ.). The programmed supply current (I_{PG}) required during writing is approximately 500 μA.

8.51 EEPROM read operation

EEPROM read operations must start at a valid address in the non-contiguous memory map. Single byte or block reads are permitted.

8.52 EEPROM write operation

EEPROM write operations must always take place in blocks of 6 bytes, starting at the beginning of a row. Programming a single byte will reset the other bytes in the same row. Modifying a single byte in a row requires re-writing the unchanged bytes with their old contents.

After writing each block a pause of 7.5 ms (max.) is required to complete the internal programming operation. During this time the external microcontroller may generate an I²C-bus STOP condition. If another I²C-bus transfer is initiated the decoder will pull SCL LOW during this pause.

After writing the EEPROM programming enable bit (D1) in, the control register must be reset.

8.53 Invalid write address

When an invalid write address is used, the column counter bits (D2 to D0) are forced to zero before being loaded into the address pointer. The row counter bits are used normally.

8.54 Incomplete programming sequence

A programming sequence may be aborted by an I²C-bus STOP condition. The EEPROM programming enable bit (D1) in the control register must then be reset.

Any bytes received from the last 6-byte block will be ignored and the contents of this (incomplete) EEPROM block will remain unchanged.

8.55 Unused EEPROM locations

A total of 20 EEPROM bytes are available for general purpose storage (see Table 22).

Table 22 Unused EEPROM addresses

ROW	HEX
0	04 and 05(1)
5	28 to 2D
6	30 to 35
7	38 to 3D

Note

1. When using bytes 04H and 05H, care must be taken to preserve the SPF information stored in bytes 00H to 03H.

8.56 Special programmed function allocation

The SPF bit allocation in the EEPROM is shown in Tables 23 to 27. The SPF bits are located in row 0 of the EEPROM and occupy 4 bytes.

Bytes 04H and 05H are not used and are available for general purpose storage.

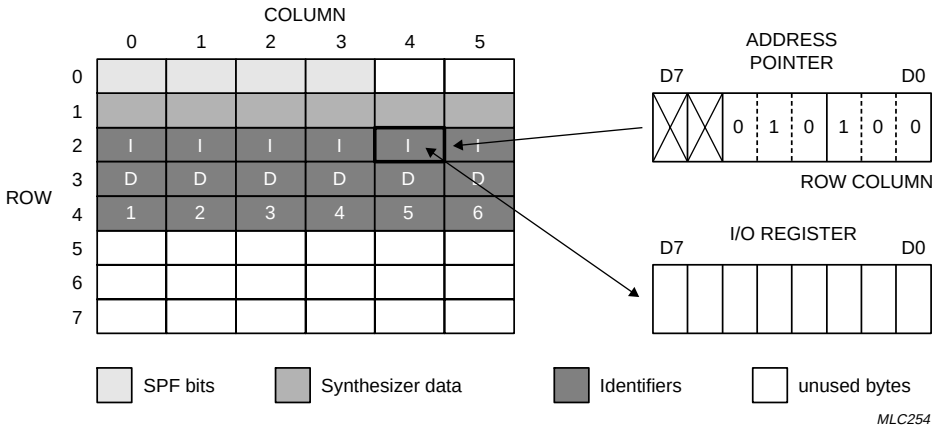


Fig.11 EEPROM organization and access.

Table 23 Special programmed functions (EEPROM address 00H)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	0	POCSAG decoding enabled
	1	APOC-1 decoding enabled
D1	0	cycle length: 5 batches
	1	cycle length: 15 batches
D5 to D2 (MSB: D5)	0 to 4	batch number (D1 = 0, MSB is ignored)
	0 to 14	batch number (D1 = 1)
D6	1	continuous data decoding enabled
D7	1	received data inversion enabled

Table 24 Special programmed functions (EEPROM address 01H)

BIT (MSB: D7)	VALUE	DESCRIPTION
D1 and D0	0 0	5 ms receiver establishment time (nominal); note 1
	0 1	10 ms
	1 0	15 ms
	1 1	30 ms
D3 and D2	0 0	20 ms oscillator establishment time (nominal); note 1
	0 1	30 ms
	1 0	40 ms
	1 1	50 ms
D5 and D4	0 0	512 bits/s received bit rate
	0 1	1024 bits/s (not used in POCSAG)
	1 0	1200 bits/s
	1 1	2400 bits/s
D6	1	synthesizer interface enabled (programming at switch-on)
D7	1	voltage converter enabled

Note

1. Since the exact establishment time is related to the programmed bit rate, Table 25 shows the values for the various bit rates.

Table 25 Establishment time as a function of bit rate

NOMINAL ESTABLISHMENT TIME	ACTUAL ESTABLISHMENT TIME			
	512 (bits/s)	**1024 (bits/s)**	**1200 (bits/s)**	**2400 (bits/s)**
5 ms	5.9 ms (3 bits)	5.9 ms (6 bits)	5 ms (6 bits)	5 ms (12 bits)
10 ms	11.7 ms (6 bits)	11.7 ms (12 bits)	10 ms (12 bits)	10 ms (24 bits)
15 ms	15.6 ms (8 bits)	15.6 ms (16 bits)	16.7 ms (20 bits)	16.7 ms (40 bits)
20 ms	23.4 ms (12 bits)	23.4 ms (24 bits)	20 ms (24 bits)	20 ms (48 bits)
30 ms	31.2 ms (16 bits)	31.2 ms (32 bits)	26.7 ms (32 bits)	26.7 ms (64 bits)
40 ms	39.1 ms (20 bits)	39.1 ms (40 bits)	40 ms (48 bits)	40 ms (96 bits)
50 ms	46.9 ms (24 bits)	46.9 ms (48 bits)	53.3 ms (64 bits)	53.3 ms (128 bits)

Table 26 Special programmed functions (EEPROM address 02H)

BIT (MSB: D7)	VALUE	DESCRIPTION
D0	X	not used
D1	X	not used
D3 and D2	0 0	32768 Hz real time clock reference
	0 1	50 Hz square wave
	1 0	2 Hz
	1 1	$\frac{1}{60}$ Hz
D4	1	signal test mode enabled (REF and INT outputs)
D5	0	burst error correction enabled
D7 and D6	00	30 s (+ 0.5 s max.) transmitter off time-out
	01	60 s (+ 1 s max.)
	10	120 s (+ 2 s max.)
	11	240 s (+ 4 s max.)

Table 27 Special programmed functions (EEPROM address 03H)

BIT (MSB: D7)	VALUE	DESCRIPTION
D1 and D0	0 0	2048 Hz acoustic alerter frequency
	0 1	2731 Hz
	1 0	4096 Hz
	1 1	3200 Hz
D2	1	automatic POCSAG alert generation enabled
D3	X	not used
D4	X	not used
D5	X	not used
D6	0	INT output polarity: active LOW
	1	INT output polarity: active HIGH
D7	X	not used

8.57 Synthesizer programming data

Data for programming a PLL synthesizer via pins ZSD, ZSC and ZLE can be stored in row 1 of the EEPROM. Six bytes are available starting with address 08H.

Data is transferred in two serial blocks of 24 bits each, starting with bit 0 (MSB) of block 1. Any unused bits must be programmed at the beginning of a block.

Table 28 Synthesizer programming data (EEPROM address 08H to 0DH)

ADDRESS (HEX)	BIT (MSB: D7)	DESCRIPTION
08	D7 to D0	bits 0 to 7 of data block 1 (bit 0 is MSB)
09	D7 to D0	bits 8 to 15
0A	D7 to D0	bits 16 to 23
0B	D7 to D0	bits 0 to 7 of data block 2 (bit 0 is MSB)
0C	D7 to D0	bits 8 to 15
0D	D7 to D0	bits 16 to 23

8.58 Identifier storage allocation

Up to 6 different identifiers can be stored in EEPROM for matching with incoming data. The PCD5002 can distinguish two types of identifiers:

- User addresses (RIC)
- User Programmable Sync Words (UPSW)
- Batch zero identifiers
- Continuous data decoding (CDD) sync words.

Identifiers are stored in EEPROM rows 2, 3 and 4. Each identifier location consists of 3 bytes in the same column. The identifier number is equal to the column number + 1.

Each identifier can be individually enabled. The standard POCSAG sync word is always enabled and has identifier number 7.

The identifier type is determined by bits D2 and D0 of identifier byte 3, as shown in Table 31.

Identifiers 1 and 2 always represent RICs or batch zero identifiers. The last 4 identifiers (numbers 3 to 6) can represent any identifier type.

A UPSW represents an unused address and must differ by more than 6 bits from preamble to guarantee detection.

A batch zero identifier marks the start of a new cycle in the APOC-1 protocol. It is only recognized when APOC-1 decoding has been enabled (SPF byte 00, bit D0).

Reception of a CDD sync word initiates continuous data decoding. CDD sync words are only recognized when continuous data decoding has been enabled (SPF byte 00, bit 6).

Table 29 shows the memory locations of the 6 identifiers. The bit allocation per identifier is given in Table 30.

Table 29 Identifier storage allocation (EEPROM address 10H to 25H)

ADDRESS (HEX)	BYTE	DESCRIPTION
10 to 15	1	identifier number 1 to 6
18 to 1D	2	identifier number 1 to 6
20 to 25	3	identifier number 1 to 6

Table 30 Identifier bit allocation

BYTE	BIT (MSB: D7)	DESCRIPTION
1	D7 to D0	bits 2 to 9 of POCSAG codeword (RIC or UPSW); notes 1 and 2
2	D7 to D0	bits 10 to 17
3	D7 and D6	bits 18 and 19
	D5	frame number bit FR3 (RIC); note 3
	D4	frame number bit FR2 (RIC)
	D3	frame number bit FR1 (RIC)
	D2	identifier type selection (0 = UPSW, 1 = RIC); note 4
	D1	identifier enable (1 = enabled)
	D0	batch zero ID/continuous decoding (1 = enabled)

Notes

1. The bit numbering corresponds with the numbering in a POCSAG codeword; bit 1 is the flag bit (0 = address, 1 = message).
2. A UPSW needs 18 bits to be matched for successful identification. Bit 1 (MSB) must be logic 0. Bits 2 to 19 contain the identifier bit pattern, they are followed by 2 predetermined random (function) bits and the UPSW is completed by 10 CRC error correction bits and an even-parity bit.
3. Bits FR3 to FR1 (MSB: FR3) contain the 3 least significant bits of the 21-bit RIC.
4. Identifiers 1 and 2 (RIC only) will be disabled by programming bit D2 as logic 0.

Table 31 Identifier types

BYTE 3, BIT D2	BYTE 3, BIT D0	DESCRIPTION
0	0	user programmable sync word (UPSW)
0	1	continuous data decoding (CDD) sync word
1	0	normal user address (RIC)
1	1	batch zero identifier

8.59 Voltage doubler

An on-chip voltage doubler provides an unregulated DC output for supplying an LCD or a low power microcontroller at output V_{PO}. An external ceramic capacitor of 100 nF (typ.) is required between pins CCN and CCP. The voltage doubler is enabled via SPF programming.

8.60 Level-shifted interface

All interface lines are suited for communication with a microcontroller operating from a higher supply voltage. The external device must have a common reference at V_{SS} of the PCD5002.

The reference voltage for the level-shifted interface must be applied to input V_{PR}. If required this could be the on-chip voltage doubler output V_{PO}. When the microcontroller has a separate (regulated) supply it should be connected to V_{PR}.

The level-shifted interface lines are RST, DON, ALC, REF and INT.

The I^2C-bus interface lines SDA and SCL can be level-shifted independently of V_{PR} by the standard external pull-up resistors.

8.61 Signal test mode

A special ‘signal test’ mode is available for monitoring the performance of a receiver circuit together with the front-end of the PCD5002.

For this purpose the output of the digital noise filter and the recovered bit clock are made available at outputs REF and INT respectively. All synchronization and decoding functions are normally active.

The ‘signal test’ mode is activated/deactivated by SPF programming.

9 OPERATING INSTRUCTIONS

9.1 Reset conditions

When the PCD5002 is reset by applying a HIGH level to input RST, the condition of the decoder is as follows:

- OFF status (irrespective of DON input level)
- REF output frequency 32768 Hz
- All internal counters reset
- Status/control register reset
- INT output at LOW level
- No alert transducers selected
- LED, VIB and ATH outputs at LOW level
- ATL output high-impedance
- SDA and SCL inputs high-impedance
- Voltage converter disabled.

The programmed functions are activated within t_{RSU} after release of the reset condition (RST LOW). The settings affecting the external operation of the PCD5002 are as follows:

- REF output frequency
- Voltage converter
- INT output polarity
- Signal test mode.

When input DON is HIGH, the decoder starts operating in ON status immediately following t_{RSU}.

9.2 Power-on reset circuit

During power-up of the PCD5002 a HIGH level of minimum duration t_{RST} = 50 μs must be applied to pin RST. This is to prevent EEPROM corruption which might otherwise occur because of the undefined contents of the Control register.

The reset signal can be applied by the external microcontroller or by an RC power-on reset circuit on pin RST (C to V_{PR}, R to V_{SS}). Such an RC-circuit should have a time constant of at least $3t_{RST}$ = 150 μs.

Input RST has an internal high-ohmic pull-down resistor (nominal 2 MΩ at 2.5 V supply) which could be used together with a suitable external capacitor connected to V_{PR} to create a power-on reset signal. However, since this pull-down resistor varies considerably with processing and supply voltage, the resulting time constant is inaccurate.

A more accurate reset duration can be realised with an additional external resistor connected to V_{SS}. Recommended minimum values in this case are C = 2.2 nF and R = 100 kΩ (see Fig.16).

9.3 Reset timing

The start-up time for the crystal oscillator may exceed 1 s (typ. 800 ms). It is advisable to apply a reset condition, at least during the first part of this period. The minimum reset pulse duration t_{RST} is 50 μs.

During reset the oscillator is active, but clock signals are inhibited internally. Once the reset condition is released the end of the oscillator start-up period can be detected by a rising edge on output INT.

During a reset the voltage converter clock (V_{clk}) is held at zero. The resulting output voltage drop may cause problems when the external resetting device is powered by the internal voltage doubler. A sufficiently large buffer capacitor connected between output V_{PO} and V_{SS} must be provided to supply the microcontroller during reset. The voltage at V_{PO} will not drop below V_{DD} − 0.7 V.

Immediately after a reset all programmable internal functions will start operating according to a programmed value of 0. During the first 8 full clock cycles (t_{RSU}) all programmed values are loaded from EEPROM.

After reset the receiver outputs RXE and ROE become active immediately, if DON is HIGH and the synthesizer is disabled. When the synthesizer is enabled, RXE and ROE will only become active after the second pulse on ZLE completes the loading of synthesizer data.

The full reset timing is illustrated in Fig.12. The start-up timing including synthesizer programming is illustrated in Fig.13.

9.4 Initial programming

A newly-delivered PCD5002 has EEPROM contents which are undefined. The EEPROM should therefore be programmed, followed by a reset to activate the SPF settings, before any attempt is made to use the device.

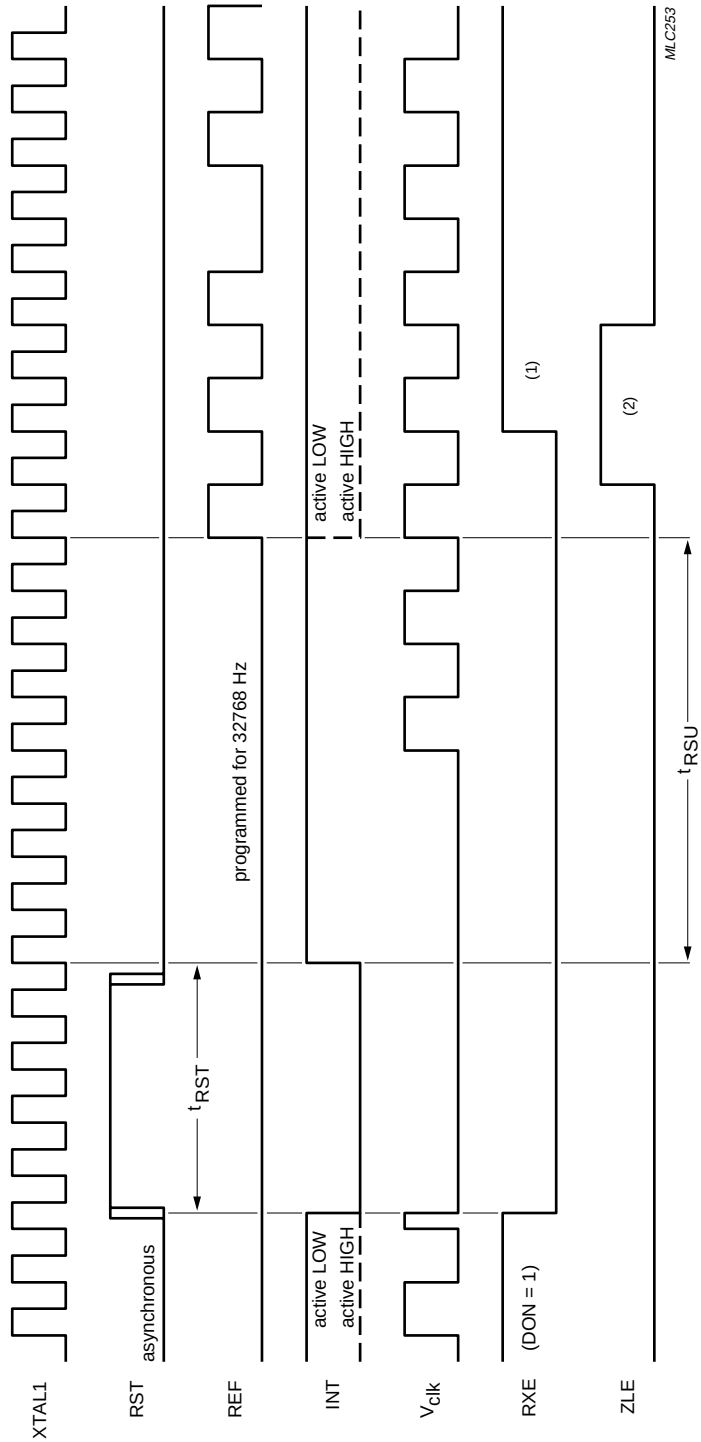


Fig.12 Reset timing.

(1) The RXE output signal is shown for disabled synthesizer. When the synthesizer is enabled RXE is held off until after the second pulse on ZLE (programming complete).
(2) The ZLE output signal is shown for enabled synthesizer and DON = 1. When DON = 0 output ZLE remains HIGH until ON state is entered (DON = 1 or control register bit D4 = 1).

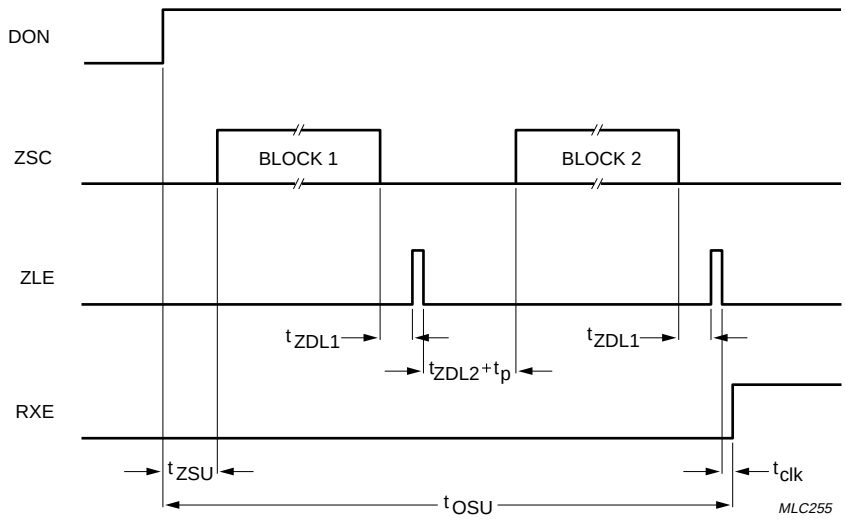


Fig.13 Start-up timing including synthesizer programming.

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage		–0.5	+7.0	V
V_{PR}	external reference voltage input	$V_{PR} \geq V_{DD} - 0.8$ V	–0.5	+7.0	V
V_n	voltage on pins ALC, DON, RST, SDA and SCL	$V_n \leq 7.0$ V	$V_{SS} - 0.8$	$V_{PR} + 0.8$	V
V_{n1}	input voltage on any other pin	$V_{n1} \leq 7.0$ V	$V_{SS} - 0.8$	$V_{DD} + 0.8$	V
P_{tot}	total power dissipation		–	250	mW
P_O	power dissipation per output		–	100	mW
T_{amb}	operating ambient temperature		–25	+70	°C
T_{stg}	storage temperature		–55	+125	°C

11 DC CHARACTERISTICS

V_{DD} = 2.7 V; V_{PR} = 2.7 V; V_{SS} = 0 V; T_{amb} = −25 to +70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	supply voltage	voltage converter disabled	1.5	2.7	6.0	V
V_{PR}	external reference voltage input	$V_{PR} \geq V_{DD} - 0.8$ V	1.5	2.7	6.0	V
I_{DD0}	supply current (OFF)	note 1	–	25.0	40.0	µA
I_{DD1}	supply current (ON)	note 1; DON = V_{DD}	–	50.0	80.0	µA
V_{PG}	programming supply voltage	voltage converter disabled	2.0	–	6.0	V
		voltage converter enabled	2.0	–	3.0	V
I_{PG}	programming supply current		–	–	800	µA
Inputs						
V_{IL}	LOW level input voltage					
	RDI, BAT		V_{SS}	–	$0.3V_{DD}$	V
	DON, ALC, RST		V_{SS}	–	$0.3V_{PR}$	V
	SDA, SCL		V_{SS}	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage					
	RDI, BAT		$0.7V_{DD}$	–	V_{DD}	V
	DON, ALC, RST		$0.7V_{PR}$	–	V_{PR}	V
	SDA, SCL		$0.7V_{DD}$	–	V_{PR}	V
I_{IL}	LOW level input current pins RDI, BAT,TS1, TS2, DON, ALC and RST	T_{amb} = 25 °C; $V_I = V_{SS}$	0	–	–0.5	µA
I_{IH}	HIGH level input current	T_{amb} = 25 °C				
	TS1, TS2	$V_I = V_{DD}$	6	–	20	µA
	RDI, BAT	$V_I = V_{DD}$; RXE = 0	6	–	20	µA
	RDI, BAT	$V_I = V_{DD}$; RXE = 1	0	–	0.5	µA
	DON, ALC, RST	$V_I = V_{PR}$	250	500	850	nA
Outputs						
I_{OL}	LOW level output current	T_{amb} = 25 °C				
	VIB, LED	V_{OL} = 0.3 V	80	–	–	µA
	ATH	V_{OL} = 0.3 V	250	–	–	µA
	INT, REF	V_{OL} = 0.3 V	80	–	–	µA
	ZSD, ZSC, ZLE	V_{OL} = 0.3 V	70	–	–	µA
	ATL	V_{OL} = 1.2 V; note 2	13	27	55	mA
	ROE, RXE	V_{OL} = 0.3 V	80	–	–	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{OH}	HIGH level output current	T_{amb} = 25 °C				
	VIB, LED	V_{OH} = 0.7 V	–0.6	–	–2.4	mA
	ATH	V_{OH} = 0.7 V	–3.0	–	–11.0	mA
	INT, REF	V_{OH} = 2.4 V	–80	–	–	µA
	ZSD, ZSC, ZLE	V_{OH} = 2.4 V	–60	–	–	µA
	ATL	ATL high-impedance; note 3	–	–	–0.5	µA
	ROE, RXE	V_{OH} = 2.4 V	–600	–	–	µA

Notes

1. Inputs: SDA and SCL pulled up to V_{DD}; all other inputs connected to V_{SS}.
   Outputs: RXE and ROE logic 0; REF: $f_{ref} = 1/60$ Hz; all other outputs open-circuit.
   Oscillator: no crystal; external clock f_{osc} = 76800 Hz; amplitude: V_{SS} to V_{DD}.
   Voltage convertor disabled (SPF byte 01, bit D7 = 0; see Table 24).
2. Maximum output current is subject to absolute maximum ratings per output (see Chapter 10).
3. When ATL (open drain output) is not activated it is high impedance.

12 DC CHARACTERISTICS (WITH VOLTAGE CONVERTER)

V_{DD} = 2.7 V; V_{SS} = 0 V; $V_{PR} = V_{PO}$; T_{amb} = –25 to +70 °C; C_s = 100 nF; voltage converter enabled.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage		1.5	–	3.0	V
$V_{PO(0)}$	output voltage; no load	V_{DD} = 2.7; I_{PO} = 0	–	5.4	–	V
V_{PO}	output voltage	V_{DD} = 2 V; I_{PO} = –250 µA	3.0	3.5	–	V
I_{PO}	output current	V_{DD} = 2 V; V_{PO} = 2.7 V	–400	–650	–	µA
		V_{DD} = 3 V; V_{PO} = 4.5 V	–650	–900	–	µA

13 OSCILLATOR CHARACTERISTICS

Quartz crystal type: MX-1V or equivalent.
Quartz crystal parameters: f = 76 800 Hz; $R_{S(max)}$ = 35 kΩ; C_L = 8 pF; C_0 = 1.4 pF; C_1 = 1.5 fF.
Maximum overall tolerance: $\pm 200 \times 10^{-6}$ (includes: cutting, temperature, aging) for POCSAG, $\pm 55 \times 10^{-6}$ for APOC-1 (‘transmitter off’ mode).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{XO}	output capacitance XTAL2		–	10	–	pF
g_m	oscillator transconductance	V_{DD} = 1.5 V	6	12	–	µS

14 AC CHARACTERISTICS

V_{DD} = 2.7 V; V_{SS} = 0 V; V_{PR} = 2.7 V; T_{amb} = 25 °C;. f_{osc} = 76800 Hz.

SYMBOLS	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
System clock						
T_{clk}	system clock period	f_{osc} = 76800 Hz	–	13.02	–	µs
Call alert frequencies						
f_{AL}	alert frequency	SPF byte 03H; bits:				
		D1, D0 = 0 0	–	2048	–	Hz
		D1, D0 = 0 1	–	2731	–	Hz
		D1, D0 = 1 0	–	3200	–	Hz
		D1, D0 = 1 1	–	4096	–	Hz
f_{AW}	warbled alert; modulation frequency	alert set-up bit D2 = 1; outputs ATL, ATH and LED	–	16	–	Hz
f_{AWH}	warbled alert; high acoustic alert frequency	alert set-up bit D2 = 1; outputs ATL and ATH	–	f_{AL}	–	Hz
f_{AWL}	warbled alert; low acoustic alert frequency	alert set-up bit D2 = 1; outputs ATL and ATH	–	$\frac{1}{2}f_{AL}$	–	Hz
f_{VBP}	pulsed vibrator frequency (square wave)	low-level alert	–	25	–	Hz
Call alert duration						
t_{ALT}	alert time-out period		–	16	–	s
t_{ALL}	ATL output time-out period	low-level alert	–	4	–	s
t_{ALH}	ATH output time-out period	high-level alert	–	12	–	s
t_{VBL}	VIB output time-out period	low-level alert	–	4	–	s
t_{VBH}	VIB output time-out period	high-level alert	–	12	–	s
t_{ALC}	alert cycle period		–	1	–	s
t_{ALP}	alert pulse duration		–	125	–	ms
Real time clock reference						
f_{ref}	real time clock reference frequency	SPF byte 02H; bits:				
		D3, D2 = 0 0; note 1	–	32768	–	Hz
		D3, D2 = 0 1; note 2	–	50	–	Hz
		D3, D2 = 1 0	–	2	–	Hz
		D3, D2 = 1 1	–	$\frac{1}{60}$	–	Hz
t_{RFP}	real time clock reference pulse duration	all reference frequencies except 50 Hz (square wave)	–	13.02	–	µs

SYMBOLS	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Receiver control						
t_{RXT}	RXE and ROE transition time	C_L = 5 pF	–	100	–	ns
t_{RXON}	RXE establishment time (nominal values: actual duration is bit rate dependent, see Table 25)	SPF byte 01H; bits:				
		D1, D0 = 0 0	–	5	–	ms
		D1, D0 = 0 1	–	10	–	ms
		D1, D0 = 1 0	–	15	–	ms
		D1, D0 = 1 1	–	30	–	ms
t_{ROON}	ROE establishment time (nominal values: actual duration is bit rate dependent, see Table 25)	SPF byte 01H; bits:				
		D3, D2 = 0 0	–	20	–	ms
		D3, D2 = 0 1	–	30	–	ms
		D3, D2 = 1 0	–	40	–	ms
		D3, D2 = 1 1	–	50	–	ms
I²C-bus interface						
f_{SCL}	SCL clock frequency		0	–	100	kHz
t_{LOW}	SCL clock low period		4.7	–	–	µs
t_{HIGH}	SCL clock HIGH period		4.0	–	–	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		500	–	–	ns
t_r	SDA and SCL rise time		–	–	1000	ns
t_f	SDA and SCL fall time		–	–	300	ns
C_B	capacitive bus line load		–	–	400	pF
$t_{SU;STA}$	START condition set-up time		4.7	–	–	µs
$t_{HD;STA}$	START condition hold time		4.0	–	–	µs
$t_{SU;STO}$	STOP condition set-up time		4.0	–	–	µs
Reset						
t_{RST}	external reset duration		50	–	–	µs
t_{RSU}	set-up time after reset	oscillator running	–	–	105	µs
t_{OSU}	set-up time after switch-on	oscillator running	–	–	4	ms
Data input						
t_{TDI}	data input transition time	see Fig.14	–	–	100	µs
t_{DI1}	data input logic 1 duration	see Fig.14	t_{BIT}	–	∞	
t_{DI0}	data input logic 0 duration	see Fig.14	t_{BIT}	–	∞	
POCSAG data timing (512 bits/s)						
f_{DI}	data input rate	SPF byte 01H; D5 = 0; D4 = 0	–	512	–	bits/s
t_{BIT}	bit duration		–	1.9531	–	ms
t_{CW}	codeword duration		–	62.5	–	ms
t_{PA}	preamble duration		1125	–	–	ms
t_{BAT}	batch duration		–	1062.5	–	ms

SYMBOLS	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
POCSAG data timing (1200 bits/s)						
f_{DI}	data input rate	SPF byte 01H; D5 = 1; D4 = 0	–	1200	–	bits/s
t_{BIT}	bit duration		–	833.3	–	µs
t_{CW}	codeword duration		–	26.7	–	ms
t_{PA}	preamble duration		480	–	–	ms
t_{BAT}	batch duration		–	453.3	–	ms
POCSAG data timing (2400 bits/s)						
f_{DI}	data input rate	SPF byte 01H; D5 = 1; D4 = 1	–	2400	–	bits/s
t_{BIT}	bit duration		–	416.6	–	µs
t_{CW}	codeword duration		–	13.3	–	ms
t_{PA}	preamble duration		240	–	–	ms
t_{BAT}	batch duration		–	226.6	–	ms
APOC-1 batch timing						
t_{SB}	cycle duration	SPF byte 00H; bit D2 = 0 (5 batches)	–	2720	–	bits
		SPF byte 00H; bit D2 = 0 (15 batches)	–	8160	–	bits
Synthesizer control						
t_{ZSU}	synthesizer set-up duration	oscillator running; note 3	1	–	2	bits
f_{ZSC}	output clock frequency	note 4	–	38400	–	Hz
t_{ZCL}	clock pulse duration		–	13.02	–	µs
t_{ZSD}	data bit duration	note 4	–	26.04	–	µs
t_{ZDS}	data bit set-up time		–	13.02	–	µs
t_{ZDL1}	data load enable delay		–	91.15	–	µs
t_{ZLE}	load enable pulse duration		–	13.02	–	µs
t_{ZDL2}	inter block delay		–	117.19	–	µs

Notes

1. 32768 Hz reference signal; 32 pulses per 75 clock cycles, alternately separated by 1 or 2 pulse periods (pulse duration: t_{RFP}). The timing is shown in Fig.15.
2. 50 Hz reference signal: square wave.
3. Duration depends on programmed bit rate; after reset t_{ZSU} = 1.5 bits.
4. Nominal values; pause in 12th data bit (see Table 11).

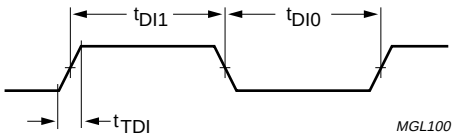


Fig.14 Data input timing.

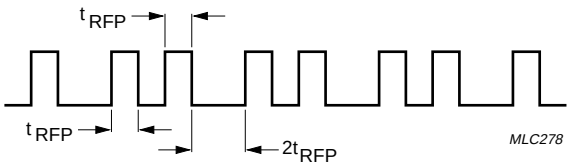


Fig.15 Timing of the 32 768 Hz reference signal.

15 APPLICATION INFORMATION

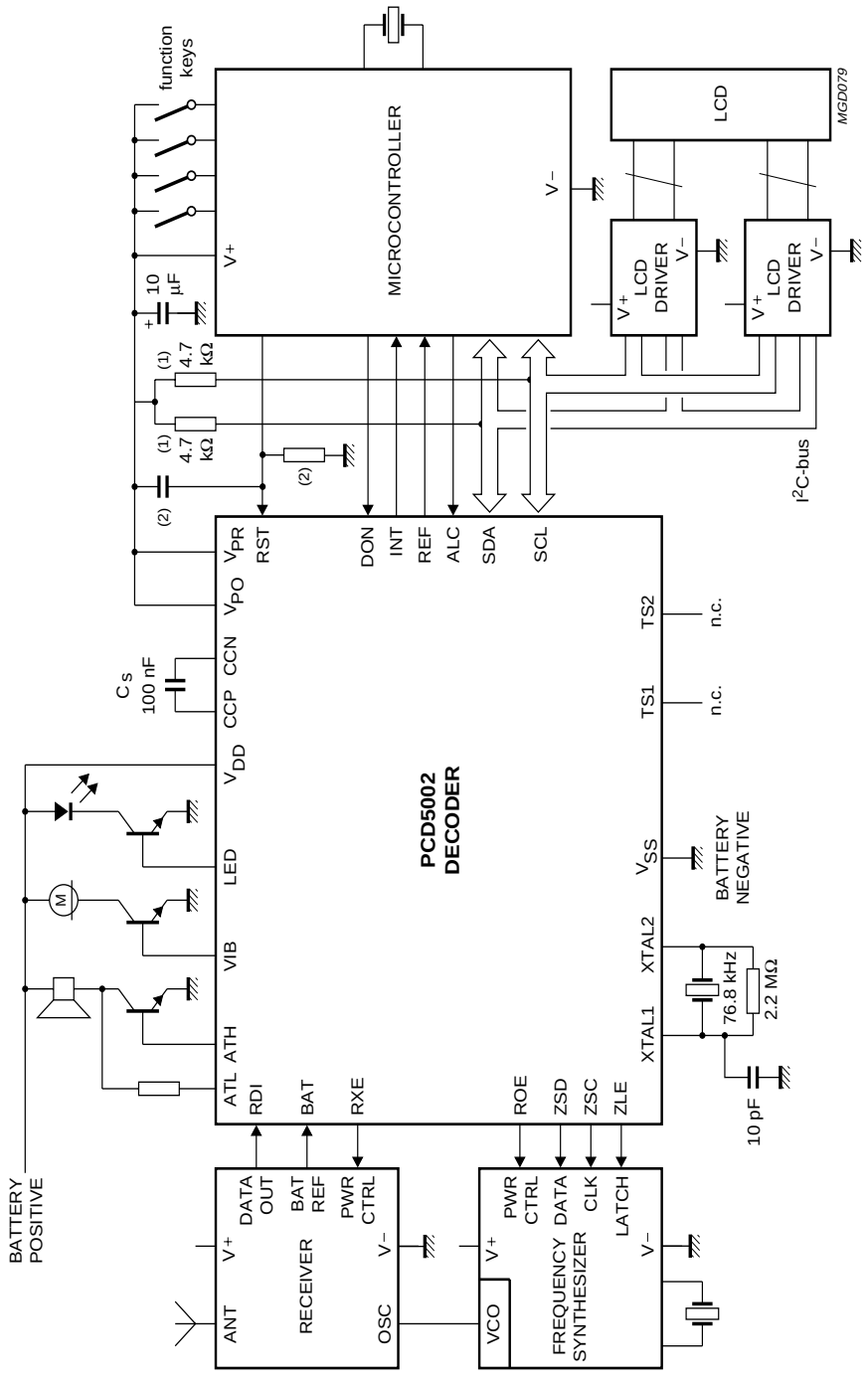
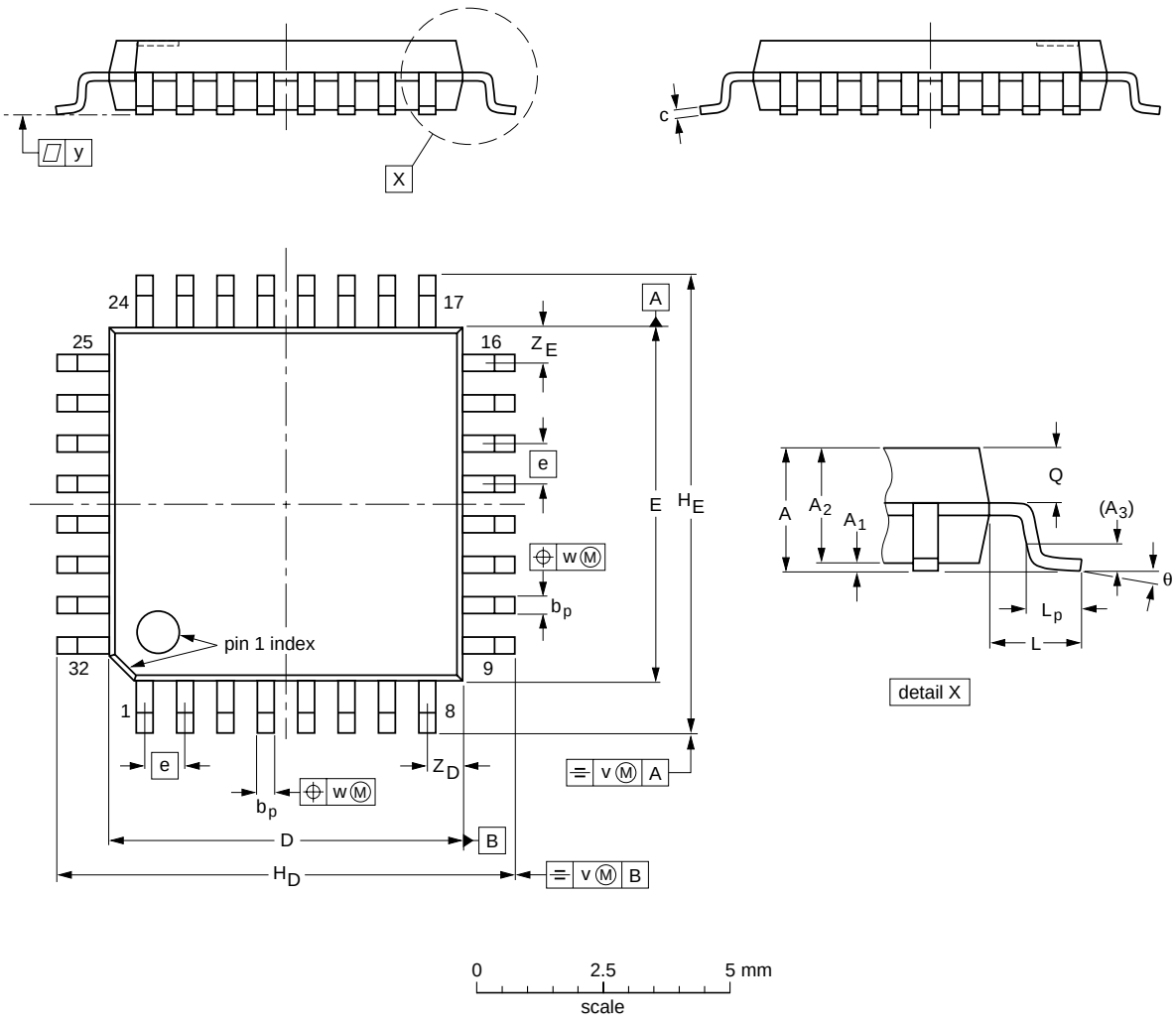


Fig.16 Typical application example (display pager).

(1) Value depends on number of devices attached.
(2) Values should be chosen to give a time constant of at least 150 µs. C = 2.2 nF and R = 100 kΩ are recommended.

16 PACKAGE OUTLINE

LQFP32: plastic low profile quad flat package; 32 leads; body 7 x 7 x 1.4 mm **SOT358-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	Q	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.4 0.3	0.18 0.12	7.1 6.9	7.1 6.9	0.8	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.69 0.59	0.2	0.25	0.1	0.9 0.5	0.9 0.5	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT358 -1						~~93-06-29~~ 95-12-19

17 SOLDERING

17.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

17.2 Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

17.3 Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering LQFP packages LQFP48 (SOT313-2), LQFP64 (SOT314-2) or LQFP80 (SOT315-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

17.4 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

18 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

19 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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