

# DATA SHEET

## **PCF84C21A; PCF84C41A; PCF84C81A** Telecom microcontrollers

Product specification  
Supersedes data of 1995 Jul 14  
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**Telecom microcontrollers****PCF84C21A; PCF84C41A;  
PCF84C81A****CONTENTS**

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## Telecom microcontrollers

PCF84C21A; PCF84C41A;  
PCF84C81A**1 FEATURES**

- Manufactured in silicon gate CMOS process
- 8-bit CPU, ROM, RAM, I/O in a 28-lead package
- 2 kbyte ROM, 64 byte RAM (PCF84C21A)
- 4 kbyte ROM, 128 byte RAM (PCF84C41A)
- 8 kbyte ROM, 256 byte RAM (PCF84C81A)
- I<sup>2</sup>C-bus interface with multi-master capability
- Over 100 instructions (based on MAB8048) all of 1 or 2 cycles
- 20 quasi-bidirectional I/O Port lines
- High sink current capability on the 8 lines of Port 1
- 8-bit programmable timer/event counter 1
- 3 single-level vectored interrupts:
  - external
  - 8-bit programmable timer/event counter 1
  - I<sup>2</sup>C-bus
- Two test inputs, one of which also serves as the external interrupt input
- Stop and Idle modes
- Supply voltage: 2.5 to 5.5 V
- Clock frequency: 1 to 16 MHz
- Operating temperature: –40 to +85 °C.

**2 GENERAL DESCRIPTION**

This data sheet details the specific properties of the PCF84C21A, PCF84C41A and PCF84C81A. The shared properties of the PCF84CxxxA family of microcontrollers are described in the “PCF84CxxxA family” data sheet which should be read in conjunction with this publication.

The PCF84C21A, PCF84C41A and PCF84C81A are general purpose CMOS microcontrollers with 2 kbytes, 4 kbytes and 8 kbytes of program memory and 64, 128 and 256 bytes of RAM, respectively. In addition to 20 I/O port lines, the microcontrollers provide an on-chip I<sup>2</sup>C-bus interface. This two-line serial bus extends the microcontroller capabilities when implemented with the powerful I<sup>2</sup>C-bus peripherals. These include LCD drivers, I/O expanders, telecom circuits, ADC and DAC converters, clock/calendar circuits, EEPROM and RAM and are listed in “Data Handbook IC12, I<sup>2</sup>C Peripherals”.

The instruction set is based on that of the MAB8048 and is a sub-set of that listed in the “PCF84CxxxA family” data sheet.

**3 ORDERING INFORMATION** (see note 1)

| TYPE NUMBER | PACKAGE |  |          |
|-------------|---------|--|----------|
|             | NAME    | DESCRIPTION  | VERSION  |
| PCF84C21AP  | DIP28   | plastic dual in-line package; 28 leads (600 mil)           | SOT117-1 |
| PCF84C41AP  |         |  |          |
| PCF84C81AP  |         |  |          |
| PCF84C21AT  | SO28    | plastic small outline package; 28 leads; body width 7.5 mm | SOT136-1 |
| PCF84C41AT  |         |  |          |
| PCF84C81AT  |         |  |          |

**Note**

1. Please refer to the Order Entry Form (OEF) for these devices for the full type number to use when ordering. This type number will also specify the required program and the ROM mask options.

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4 BLOCK DIAGRAM

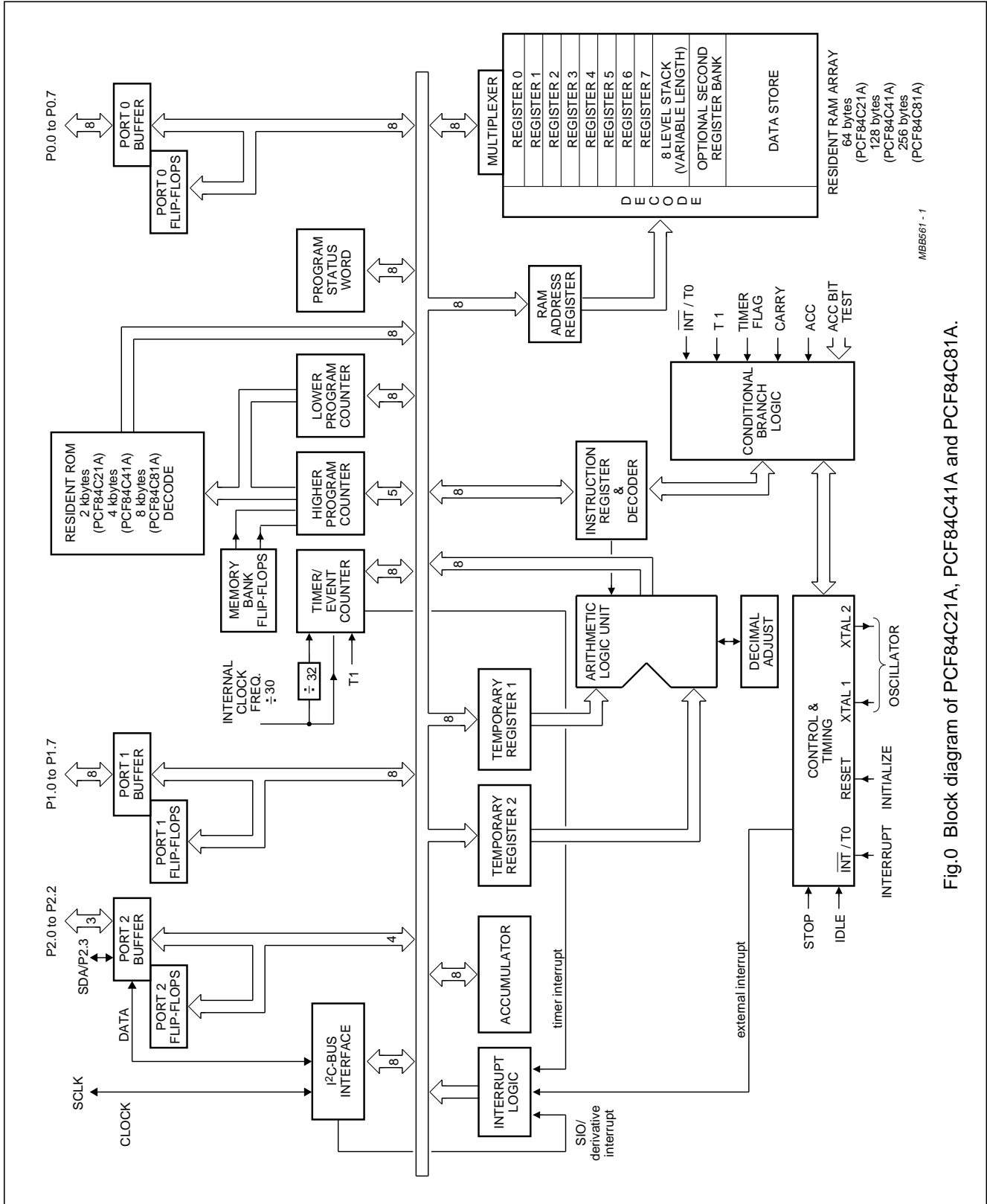


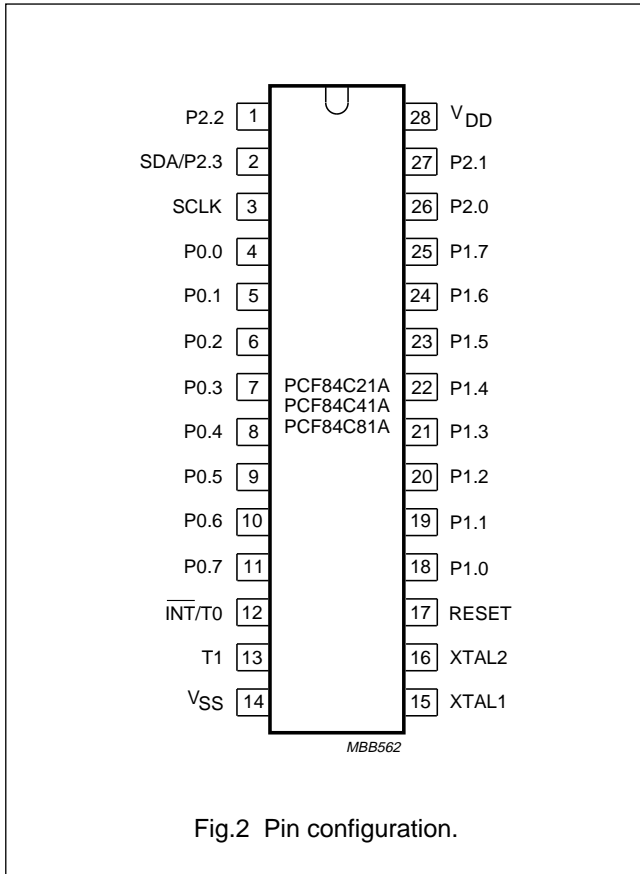
Fig.0 Block diagram of PCF84C21A, PCF84C41A and PCF84C81A.

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5 PINNING INFORMATION

5.1 Pinning



5.2 Pin description

Table 1 DIP28 and SO28 packages

| SYMBOL          | PIN      | FUNCTION  |
|-----------------|----------|---|
| P2.2            | 1        | 1 bit of Port 2: 4-bit quasi-bidirectional I/O port   |
| SDA/P2.3        | 2        | bidirectional data line of the I <sup>2</sup> C-bus interface, or 1 bit of Port 2: 4-bit quasi-bidirectional I/O port |
| SCLK            | 3        | bidirectional clock line of the I <sup>2</sup> C-bus interface  |
| P0.0 to P0.7    | 4 to 11  | 8 bits of Port 0: 8-bit quasi-bidirectional I/O port  |
| INT/T0          | 12       | Interrupt/Test 0  |
| T1              | 13       | Test 1/count input of 8-bit timer/event counter 1   |
| V <sub>SS</sub> | 14       | ground  |
| XTAL1           | 15       | crystal oscillator input or external clock input  |
| XTAL2           | 16       | crystal oscillator output   |
| RESET           | 17       | Reset input   |
| P1.0 to P1.7    | 18 to 25 | 8 bits of Port 1: 8-bit quasi-bidirectional I/O port  |
| P2.0 to P2.1    | 26 to 27 | 2 bits of Port 2: 4-bit quasi-bidirectional I/O port  |
| V <sub>DD</sub> | 28       | positive supply   |

6 INSTRUCTION SET

ROM is restricted to 2 kbytes for the PCF84C21A and 4 kbytes for the PCF84C41A. Therefore, the instructions SEL MB1/2/3 for the PCF84C21A, and the instructions SEL MB2/3 for the PCF84C41A should be avoided, as they would define non-existing program memory banks.

As RAM is limited to 64 bytes for the PCF84C21A and to 128 bytes for the PCF84C41A, care should be taken to avoid accesses to non-existing RAM locations.

See the “PCF84CxxxA family” data sheet for a complete description of the instruction set.

7 HIGH SINK OUTPUT CURRENTS

The Port 1 outputs of these devices are designed for high current drive in the logic 0 state. They are capable of driving 10 mA loads and higher. Applications include drive for small relays and light-emitting diodes (LEDs).

To avoid overload, care should be taken that the total Port 1 current averages less than 80 mA, i.e. an average of 10 mA per Port 1 line. Refer to Chapter “Limiting values” which specifies an upper limit of 100 mA for I<sub>SS</sub>.

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## 8 ROM MASK OPTIONS

| ROM CODE                      | OPTION  |                           |                         |
|-------------------------------|---|---------------------------|-------------------------|
| <b>Program/data</b>           | Any mix of instructions and data up to ROM size of 2 kbytes for the PCF84C21A, 4 kbytes for the PCF84C41A and 8 kbytes for the PCF84C81A. |                           |                         |
| <b>Port Output</b>            |   |                           |                         |
| P0.0 to P0.7                  | standard  | open-drain                | push-pull               |
| P1.0 to P1.7                  | standard  | open-drain                | push-pull               |
| P2.0 to P2.2                  | standard  | open-drain                | push-pull               |
| SDA/P2.3                      | –   | open-drain                | –                       |
| <b>Port State after reset</b> |   |                           |                         |
| P0.0 to P0.7                  | set   | reset                     | –                       |
| P1.0 to P1.7                  | set   | reset                     | –                       |
| P2.0 to P2.2                  | set   | reset                     | –                       |
| SDA/P2.3                      | set   | –                         | –                       |
| <b>Oscillator</b>             |   |                           |                         |
| Transconductance              | LOW (g <sub>mL</sub> )  | MEDIUM (g <sub>mM</sub> ) | HIGH (g <sub>mH</sub> ) |

## 9 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices. See *"Data Handbook IC14, Section: Handling MOS devices"*.

## 10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL           | PARAMETER                                  | MIN. | MAX.                  | UNIT |
|------------------|--|------|-----------------------|------|
| V <sub>DD</sub>  | supply voltage                             | –0.5 | +7                    | V    |
| V <sub>I</sub>   | all input voltages                         | –0.5 | V <sub>DD</sub> + 0.5 | V    |
| I <sub>I</sub>   | DC input current                           | –10  | +10                   | mA   |
| I <sub>O</sub>   | DC output current except Port 1 output LOW | –10  | +10                   | mA   |
| I <sub>O</sub>   | DC output current, Port 1 output LOW       | –10  | +20                   | mA   |
| P <sub>tot</sub> | total power dissipation                    | –    | 125                   | mW   |
| P <sub>O</sub>   | power dissipation per output               | –    | 30                    | mW   |
| I <sub>DD</sub>  | supply current                             | –50  | +50                   | mA   |
| I <sub>SS</sub>  | ground supply current                      | –100 | +50                   | mA   |
| T <sub>stg</sub> | storage temperature range                  | –55  | +150                  | °C   |
| T <sub>j</sub>   | operating junction temperature             | –    | 90                    | °C   |

## Telecom microcontrollers

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PCF84C81A**11 DC CHARACTERISTICS**

$V_{DD} = 2.5$  to  $5.5$  V;  $V_{SS} = 0$  V;  $T_{amb} = -40$  to  $+85$  °C; all voltages with respect to  $V_{SS}$ ; unless otherwise specified.

| SYMBOL                         | PARAMETER  | CONDITIONS   | MIN.             | TYP.                     | MAX.                     | UNIT                 |
|--------------------------------|--|--|------------------|--------------------------|--------------------------|----------------------|
| $V_{DD}$                       | operating supply voltage   | see Fig.3  | 2.5              | –                        | 5.5                      | V                    |
| $I_{DD}$                       | operating supply current   | note 1; see Figs 4 and 5<br>$V_{DD} = 3$ V; $f_{xtal} = 3.58$ MHz ( $g_{mL}$ )<br>$V_{DD} = 5$ V; $f_{xtal} = 10$ MHz ( $g_{mL}$ )<br>$V_{DD} = 5$ V; $f_{xtal} = 16$ MHz ( $g_{mM}$ )<br>$V_{DD} = 5$ V; $f_{xtal} = 16$ MHz ( $g_{mH}$ ) | –<br>–<br>–<br>– | 0.3<br>1.1<br>1.7<br>2.5 | 0.6<br>3.0<br>5.0<br>6.0 | mA<br>mA<br>mA<br>mA |
| $I_{DD(idle)}$                 | supply current (Idle mode)                                       | note 1; see Figs 6 and 7<br>$V_{DD} = 3$ V; $f_{xtal} = 3.58$ MHz ( $g_{mL}$ )<br>$V_{DD} = 5$ V; $f_{xtal} = 10$ MHz ( $g_{mL}$ )<br>$V_{DD} = 5$ V; $f_{xtal} = 16$ MHz ( $g_{mM}$ )<br>$V_{DD} = 5$ V; $f_{xtal} = 16$ MHz ( $g_{mH}$ ) | –<br>–<br>–<br>– | 0.2<br>0.8<br>1.2<br>1.7 | 0.4<br>1.6<br>4.0<br>5.0 | mA<br>mA<br>mA<br>mA |
| $I_{DD(stp)}$                  | supply current (Stop mode)                                       | $V_{DD} = 2.5$ V; notes 1 and 2; see Fig.8   | –                | 1.2                      | 10                       | µA                   |
| <b>Inputs</b>                  |  |  |                  |                          |                          |                      |
| $V_{IL}$                       | LOW level input voltage  |  | 0                | –                        | $0.3V_{DD}$              | V                    |
| $V_{IH}$                       | HIGH level input voltage   |  | $0.7V_{DD}$      | –                        | $V_{DD}$                 | V                    |
| $I_{LI}$                       | input leakage  | $V_{SS} \leq V_I \leq V_{DD}$  | –1               | –                        | +1                       | µA                   |
| <b>Outputs</b>                 |  |  |                  |                          |                          |                      |
| $I_{OL}$                       | LOW level output sink current [except Port 1; SDA/P2.3 and SCLK] | $V_{DD} = 5$ V; $V_O = 0.4$ V; see Fig.9<br>PCF84C21A; PCF84C41A<br>PCF84C81A  | 1.6<br>1.6       | 12<br>5                  | –<br>–                   | mA<br>mA             |
| $I_{OL1}$                      | LOW level output sink current; Port 1                            | $V_{DD} = 5$ V; $V_O = 1.2$ V; see Fig.10<br>PCF84C21A; PCF84C41A<br>PCF84C81A   | 10<br>10         | 30<br>19                 | –<br>–                   | mA<br>mA             |
| $I_{OL2}$                      | LOW level output sink current; SDA/P2.3 and SCLK                 | $V_{DD} = 5$ V; $V_O = 0.4$ V; see Fig.11<br>PCF84C21A; PCF84C41A<br>PCF84C81A   | 3<br>3           | 12<br>6.5                | –<br>–                   | mA<br>mA             |
| $I_{OH}$                       | HIGH level pull-up output source current                         | $V_{DD} = 5$ V; $V_O = 3.5$ V; see Fig.12<br>$V_{DD} = 5$ V; $V_O = 0$ V; see Fig.12   | 40<br>–          | 100<br>–140              | –<br>–400                | µA<br>µA             |
| $I_{OH1}$                      | HIGH level push-pull output source current                       | $V_{DD} = 5$ V; $V_O = 4.6$ V; see Fig.13  | –1.6             | –7                       | –                        | mA                   |
| <b>Oscillator</b> (see Fig.14) |  |  |                  |                          |                          |                      |
| $g_{mL}$                       | LOW transconductance   | $V_{DD} = 5$ V   | 0.2              | 0.4                      | 1.0                      | mS                   |
| $g_{mM}$                       | MEDIUM transconductance  | $V_{DD} = 5$ V   | 0.9              | 1.6                      | 3.2                      | mS                   |
| $g_{mH}$                       | HIGH transconductance  | $V_{DD} = 5$ V   | 3.0              | 4.5                      | 9.0                      | mS                   |
| $R_F$                          | feedback resistor  |  | 0.3              | 1.0                      | 3.0                      | MΩ                   |

**Notes**

- $V_{IL} = V_{SS}$ ;  $V_{IH} = V_{DD}$ ; open drain outputs connected to  $V_{SS}$ ; all other outputs, including XTAL2, open (typical values at 25 °C with crystal connected between XTAL1 and XTAL2).
- $V_{IL} = V_{SS}$ ;  $V_{IH} = V_{DD}$ ; RESET and T1 at  $V_{SS}$ ;  $\overline{INT}/T0$  at  $V_{DD}$ ; crystal connected between XTAL1 and XTAL2; open drain outputs connected to  $V_{SS}$ ; all other outputs open.

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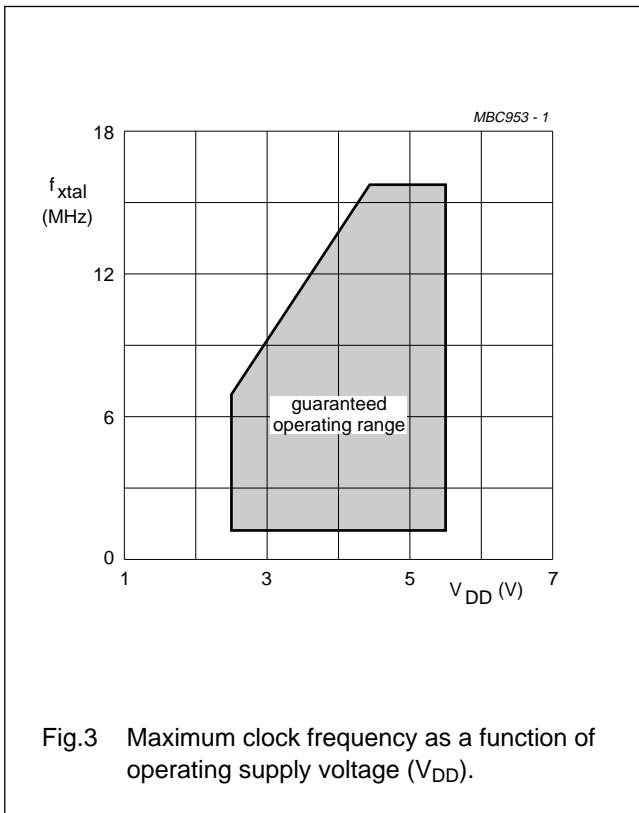
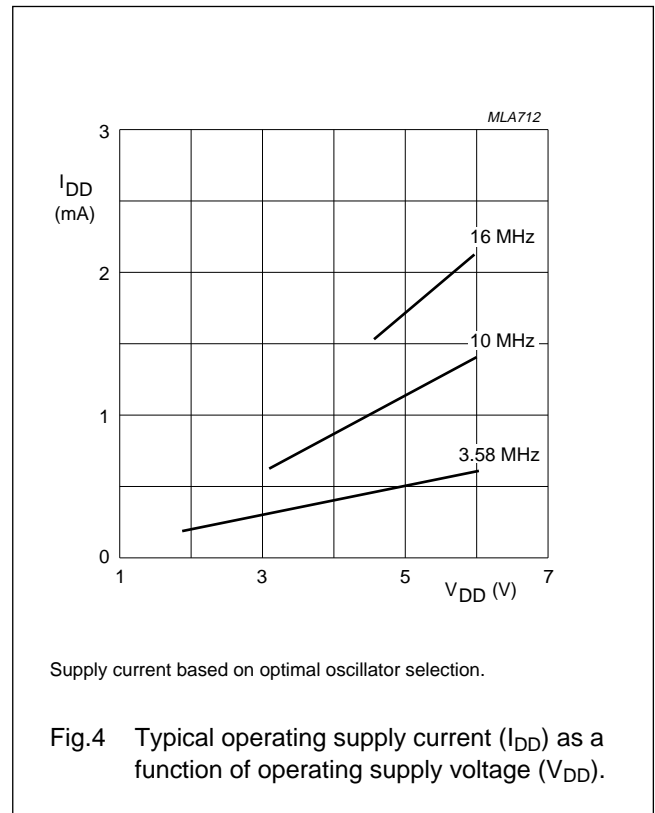
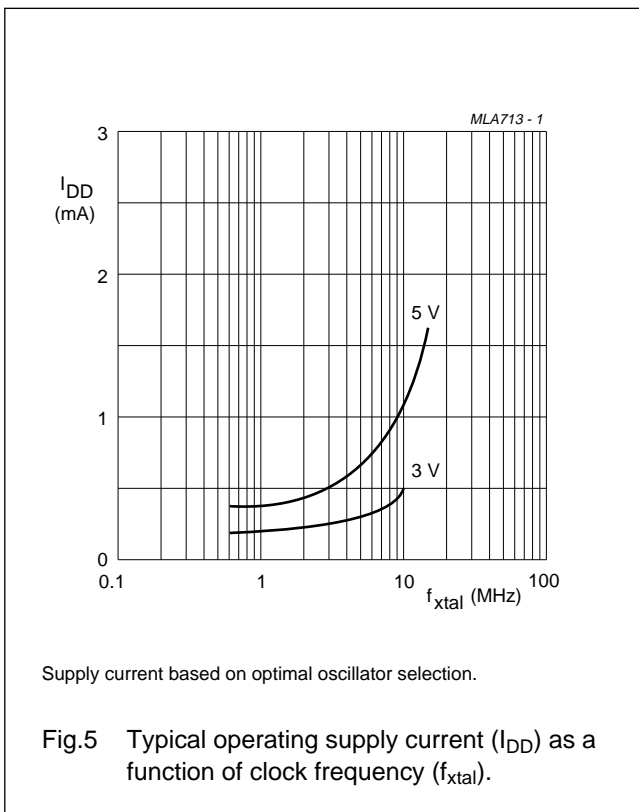


Fig.3 Maximum clock frequency as a function of operating supply voltage ( $V_{DD}$ ).



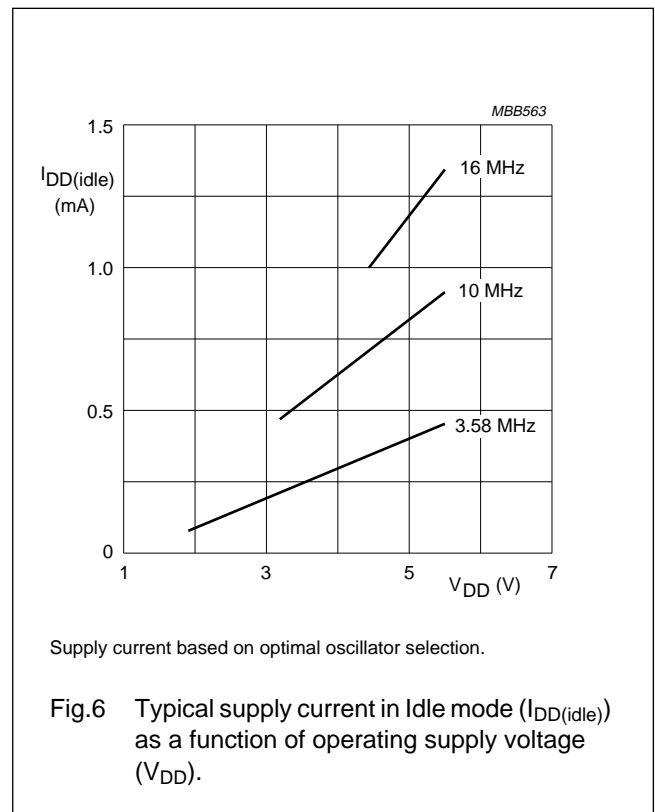
Supply current based on optimal oscillator selection.

Fig.4 Typical operating supply current ( $I_{DD}$ ) as a function of operating supply voltage ( $V_{DD}$ ).



Supply current based on optimal oscillator selection.

Fig.5 Typical operating supply current ( $I_{DD}$ ) as a function of clock frequency ( $f_{xtal}$ ).



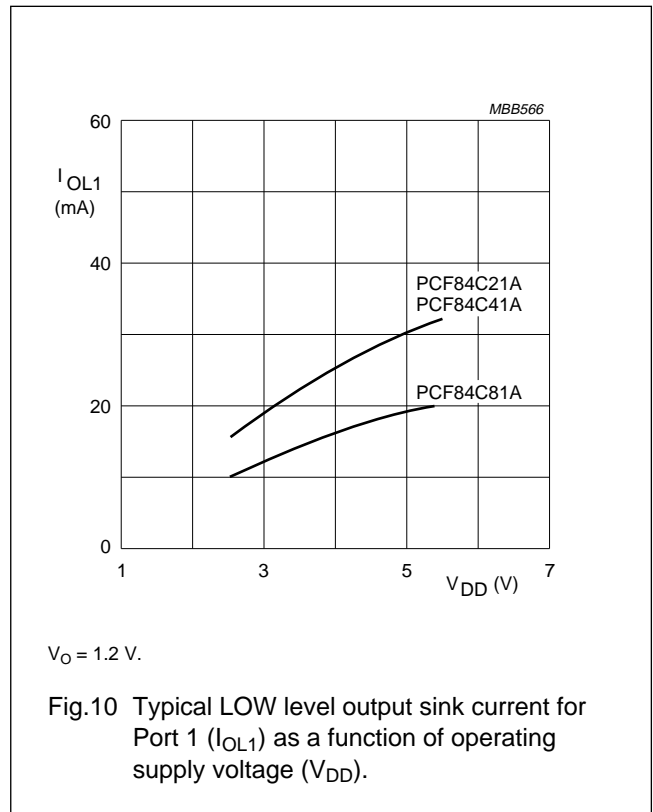
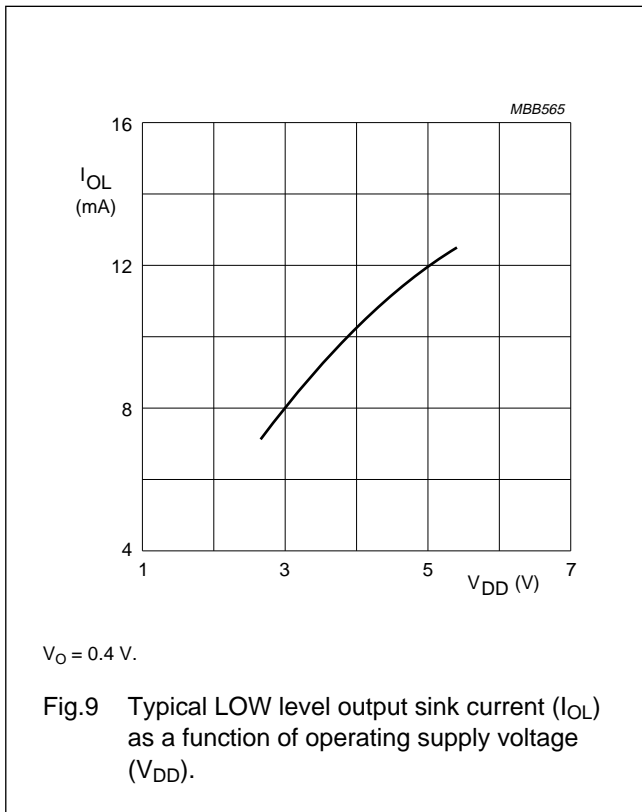
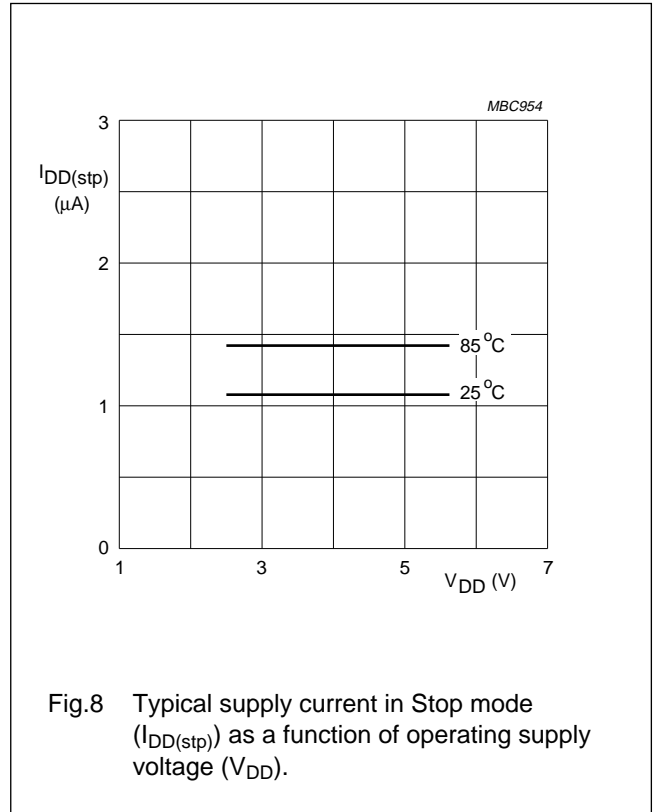
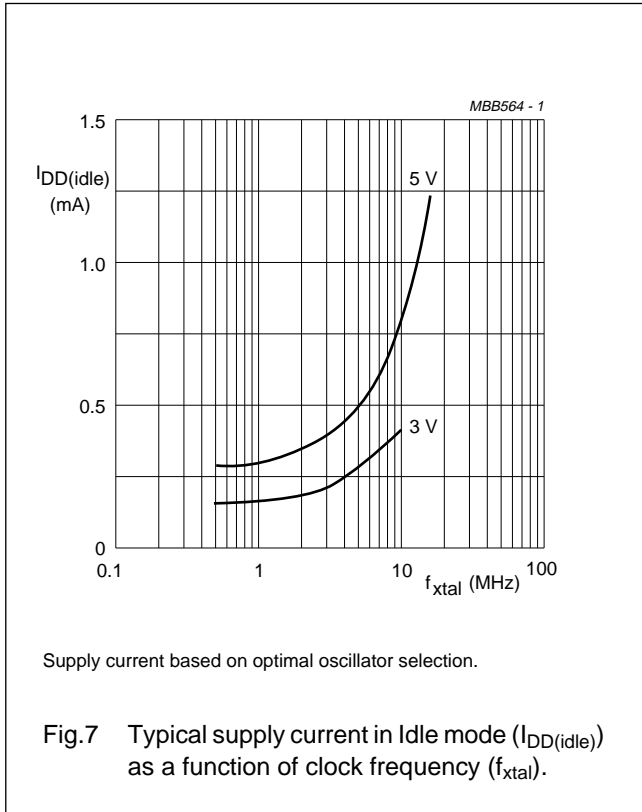
Supply current based on optimal oscillator selection.

Fig.6 Typical supply current in Idle mode ( $I_{DD(idle)}$ ) as a function of operating supply voltage ( $V_{DD}$ ).



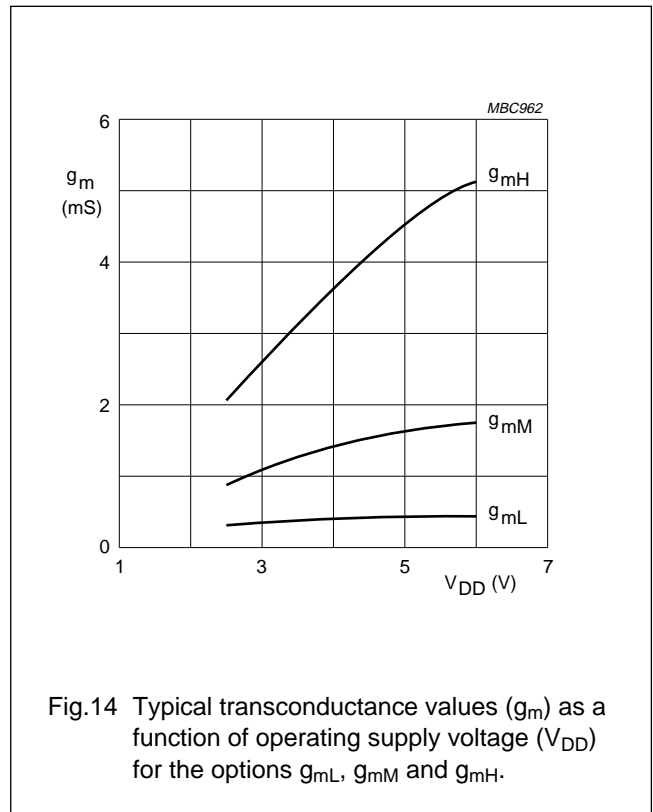
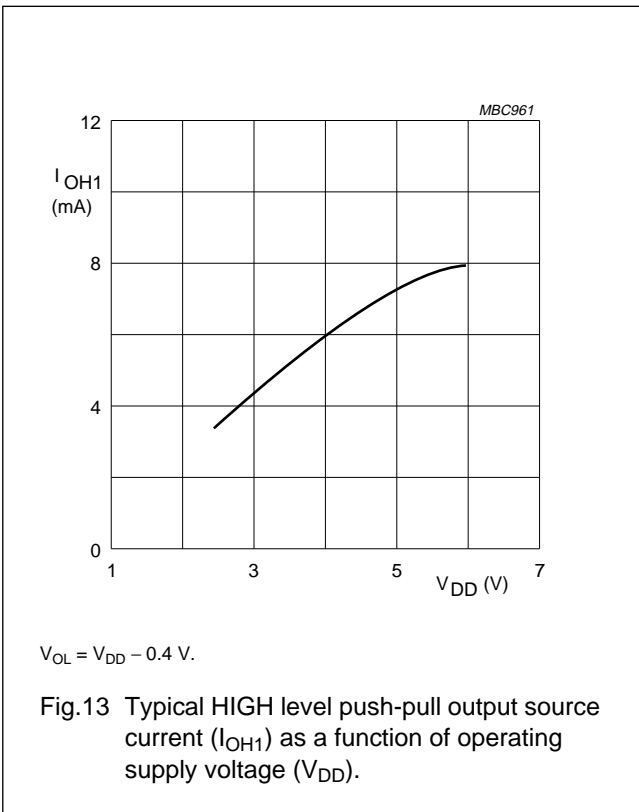
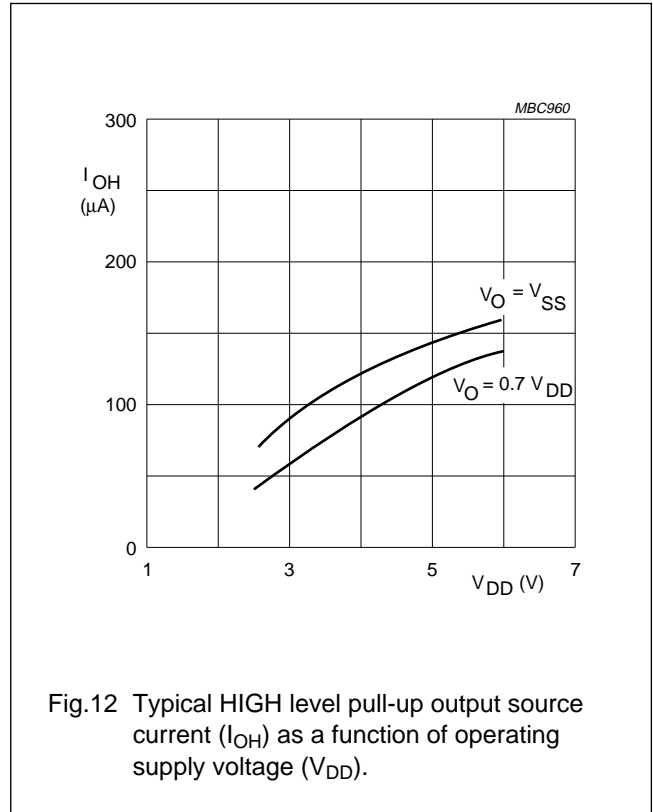
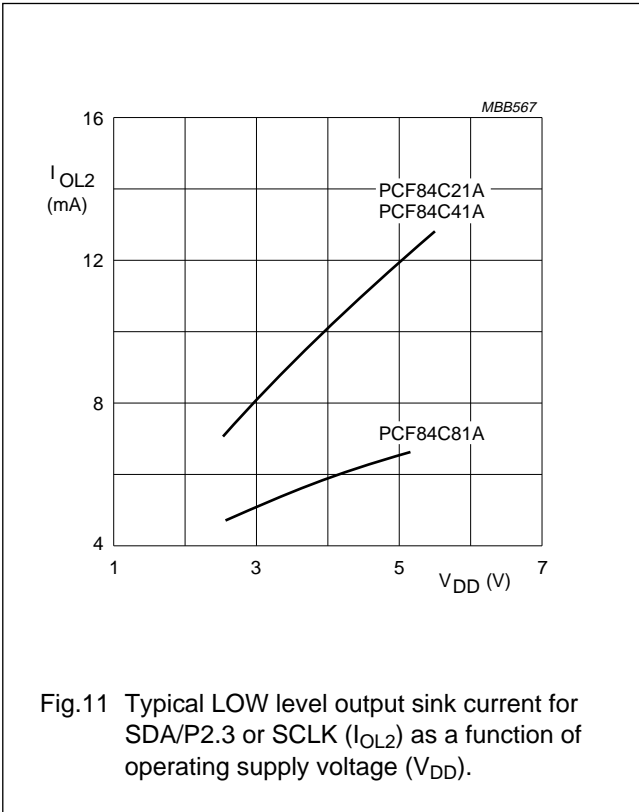
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## Telecom microcontrollers

PCF84C21A; PCF84C41A;  
PCF84C81A**12 AC CHARACTERISTICS**

$V_{DD} = 2.5$  to  $5.5$  V;  $V_{SS} = 0$  V;  $T_{amb} = -40$  to  $+85$  °C; all voltages with respect to  $V_{SS}$ ; unless otherwise specified.

| SYMBOL     | PARAMETER             | CONDITIONS                                       | MIN. | TYP. | MAX. | UNIT |
|------------|-----------------------|--|------|------|------|------|
| $t_r$      | rise time all outputs | $V_{DD} = 5$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF | –    | 30   | –    | ns   |
| $t_f$      | fall time all outputs | $V_{DD} = 5$ V; $T_{amb} = 25$ °C; $C_L = 50$ pF | –    | 30   | –    | ns   |
| $f_{xtal}$ | clock frequency       | see Fig.3  | 1    | –    | 16   | MHz  |

**Table 2** I<sup>2</sup>C-bus timing (see Figs 15 and 16)

| SYMBOL       | PARAMETER                  | INPUT<br>(see Fig.14)      | OUTPUT<br>(see Fig.15; note 1)              |
|--------------|----------------------------|----------------------------|---|
| <b>SCLK</b>  |                            |                            |   |
| $t_{HD;STA}$ | START condition hold time  | $\geq \frac{14}{f_{xtal}}$ | $\frac{DF + 9}{2 \times f_{xtal}}$          |
| $t_{LOW}$    | SCLK LOW time              | $\geq \frac{17}{f_{xtal}}$ | $\frac{DF - 3}{2 \times f_{xtal}}$ ; note 2 |
| $t_{HIGH}$   | SCLK HIGH time             | $\geq \frac{17}{f_{xtal}}$ | $\frac{DF + 3}{2 \times f_{xtal}}$ ; note 2 |
| $t_{RC}$     | SCLK rise time             | $\leq 1$ $\mu$ s           | $\leq 1$ $\mu$ s; note 3                    |
| $t_{FC}$     | SCLK fall time             | $\leq 0.3$ $\mu$ s         | $\leq 0.1$ $\mu$ s; note 4                  |
| <b>SDA</b>   |                            |                            |   |
| $t_{BUF}$    | bus free time              | $\geq \frac{14}{f_{xtal}}$ | $\geq 4.7$ $\mu$ s; note 5                  |
| $t_{SU;DAT}$ | data set-up time           | $\geq 250$ ns              | $\geq \frac{15}{f_{xtal}}$ ; note 6         |
| $t_{HD;DAT}$ | data hold time             | $\geq 0$                   | $\geq \frac{9}{f_{xtal}}$                   |
| $t_{RD}$     | SDA/P2.3 rise time         | $\leq 1$ $\mu$ s           | $\leq 1$ $\mu$ s; note 3                    |
| $t_{FD}$     | SDA/P2.3 fall time         | $\leq 0.3$ $\mu$ s         | $\leq 0.1$ $\mu$ s; note 4                  |
| $t_{SU;STO}$ | STOP condition set-up time | $\geq \frac{14}{f_{xtal}}$ | $\frac{DF - 3}{2 \times f_{xtal}}$          |

**Notes**

1. DF stands for Division Factor: the divisor of  $f_{xtal}$  (see the "PCF84CxxxA family" data sheet).

2. Values given for ASC = 0; for ASC = 1:  $t_{HIGH} = \frac{3(DF + 1)}{4 \times f_{xtal}}$ ;  $t_{LOW} = \frac{DF - 3}{4 \times f_{xtal}}$

3. Determined by I<sup>2</sup>C-bus capacitance ( $C_b$ ) and external pull-up resistor.

4. At maximum allowed I<sup>2</sup>C-bus capacitance  $C_b = 400$  pF.

5. Determined by program.

6. If  $t_{LOW} < \frac{24}{f_{xtal}}$ ,  $t_{SU;DAT} \geq \frac{t_{LOW} - 9}{f_{xtal}}$ , independent of ASC.

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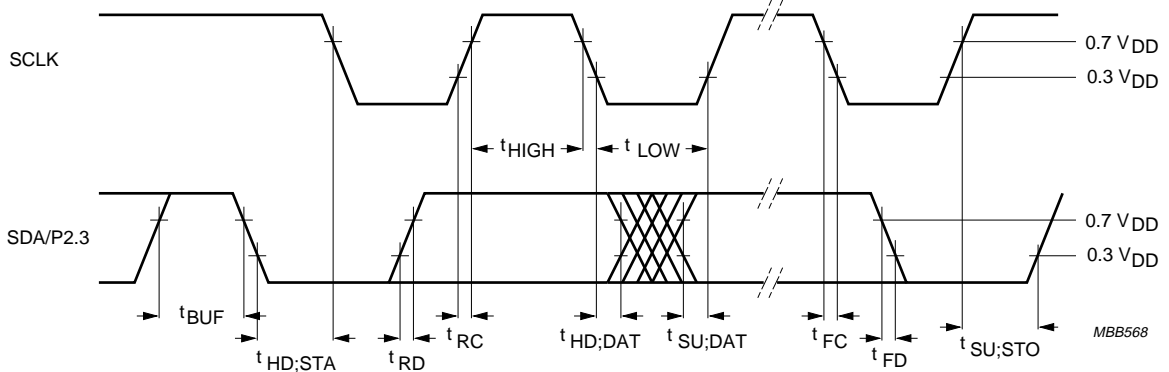


Fig.15 Slave SCLK receiver SDA/P2.3 timing (SCLK and SDA/P2.3 are inputs).

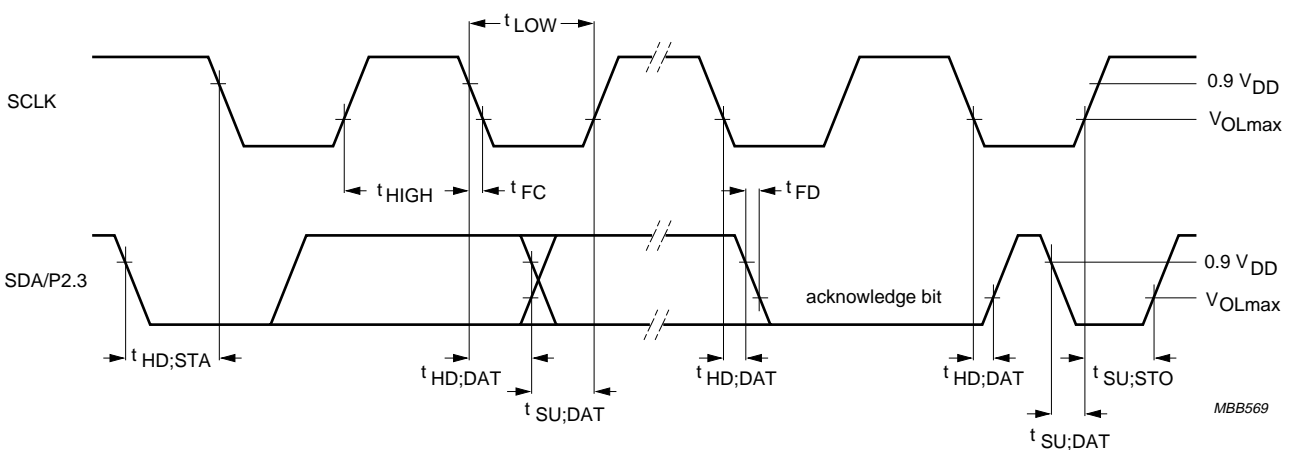


Fig.16 Master SCLK and transmitter SDA/P2,3 timing (SCLK and SDA/P2.3 are outputs).

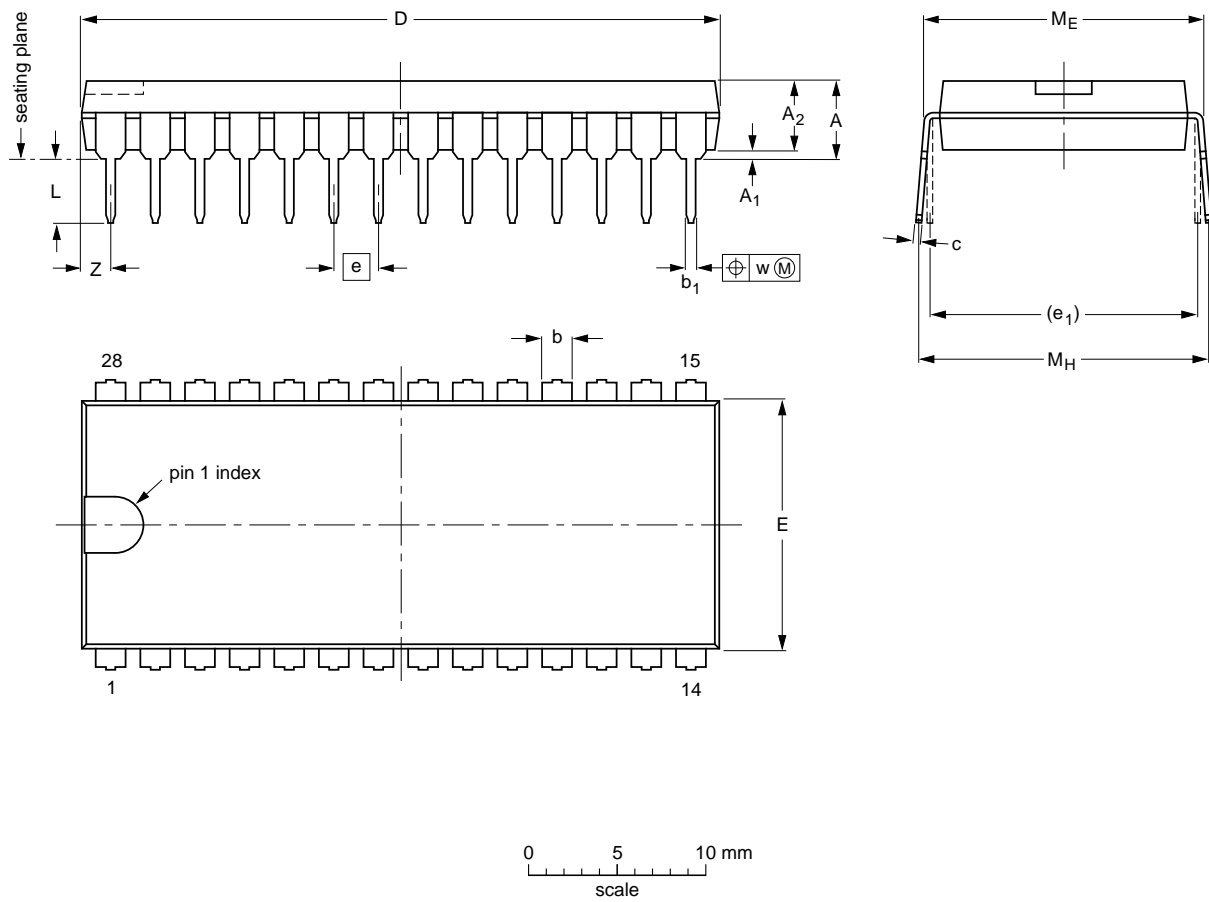
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13 PACKAGE OUTLINES

DIP28: plastic dual in-line package; 28 leads (600 mil)

SOT117-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT   | A max. | A <sub>1</sub> min. | A <sub>2</sub> max. | b              | b <sub>1</sub> | c              | D <sup>(1)</sup> | E <sup>(1)</sup> | e    | e <sub>1</sub> | L            | M <sub>E</sub> | M <sub>H</sub> | w    | Z <sup>(1)</sup> max. |
|--------|--------|---------------------|---------------------|----------------|----------------|----------------|------------------|------------------|------|----------------|--------------|----------------|----------------|------|-----------------------|
| mm     | 5.1    | 0.51                | 4.0                 | 1.7<br>1.3     | 0.53<br>0.38   | 0.32<br>0.23   | 36.0<br>35.0     | 14.1<br>13.7     | 2.54 | 15.24          | 3.9<br>3.4   | 15.80<br>15.24 | 17.15<br>15.90 | 0.25 | 1.7                   |
| inches | 0.20   | 0.020               | 0.16                | 0.066<br>0.051 | 0.020<br>0.014 | 0.013<br>0.009 | 1.41<br>1.34     | 0.56<br>0.54     | 0.10 | 0.60           | 0.15<br>0.13 | 0.62<br>0.60   | 0.68<br>0.63   | 0.01 | 0.067                 |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

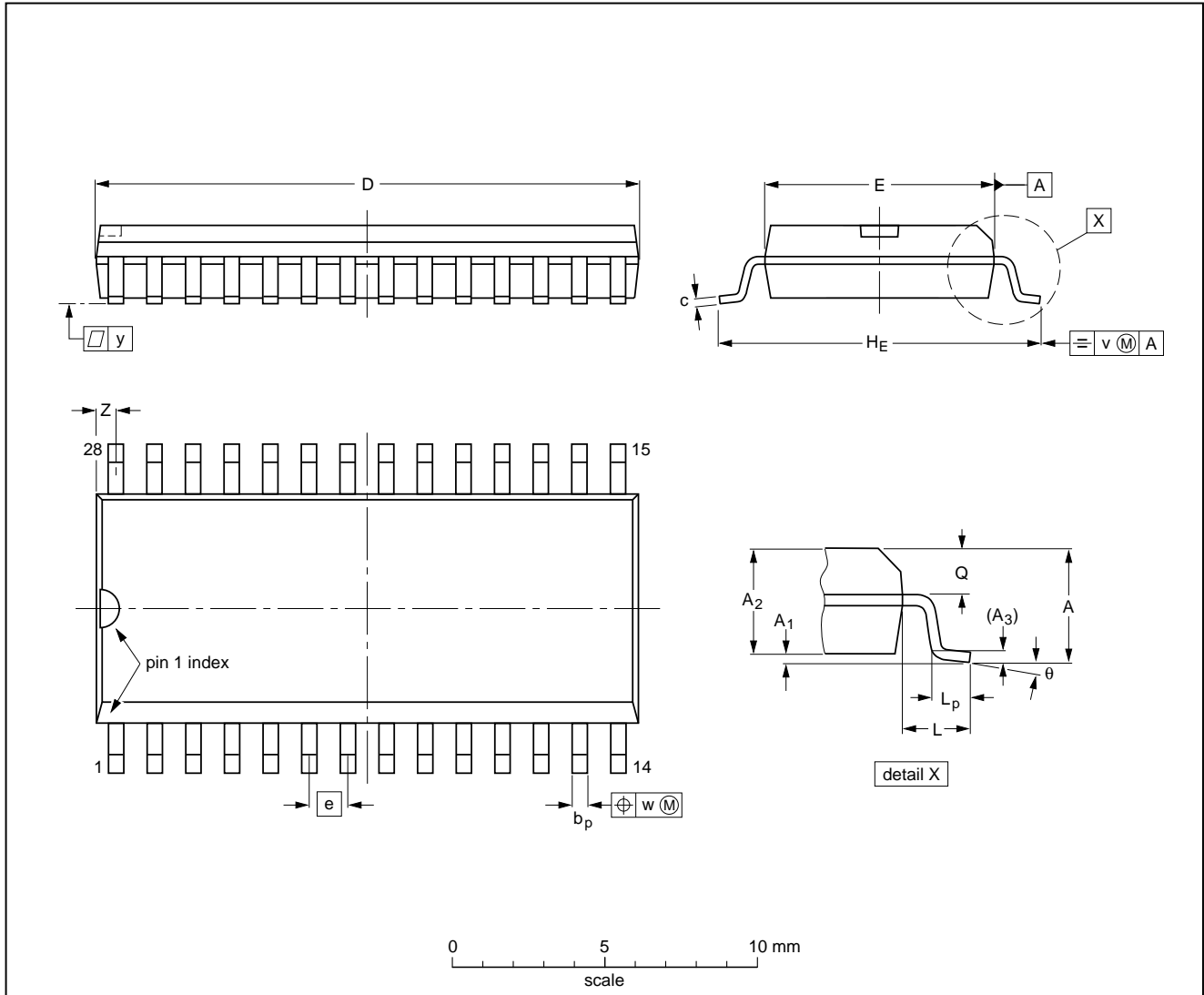
| OUTLINE VERSION | REFERENCES |          |      |  | EUROPEAN PROJECTION | ISSUE DATE           |
|-----------------|------------|----------|------|--|---------------------|----------------------|
|                 | IEC        | JEDEC    | EIAJ |  |                     |                      |
| SOT117-1        | 051G05     | MO-015AH |      |  |                     | 92-11-17<br>95-01-14 |

Telecom microcontrollers

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PCF84C81A

SO28: plastic small outline package; 28 leads; body width 7.5 mm

SOT136-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT   | A max. | A <sub>1</sub> | A <sub>2</sub> | A <sub>3</sub> | b <sub>p</sub> | c              | D <sup>(1)</sup> | E <sup>(1)</sup> | e     | H <sub>E</sub> | L     | L <sub>p</sub> | Q              | v    | w    | y     | Z <sup>(1)</sup> | θ        |
|--------|--------|----------------|----------------|----------------|----------------|----------------|------------------|------------------|-------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm     | 2.65   | 0.30<br>0.10   | 2.45<br>2.25   | 0.25           | 0.49<br>0.36   | 0.32<br>0.23   | 18.1<br>17.7     | 7.6<br>7.4       | 1.27  | 10.65<br>10.00 | 1.4   | 1.1<br>0.4     | 1.1<br>1.0     | 0.25 | 0.25 | 0.1   | 0.9<br>0.4       | 8°<br>0° |
| inches | 0.10   | 0.012<br>0.004 | 0.096<br>0.089 | 0.01           | 0.019<br>0.014 | 0.013<br>0.009 | 0.71<br>0.69     | 0.30<br>0.29     | 0.050 | 0.42<br>0.39   | 0.055 | 0.043<br>0.016 | 0.043<br>0.039 | 0.01 | 0.01 | 0.004 | 0.035<br>0.016   |          |

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES |          |      | EUROPEAN PROJECTION | ISSUE DATE           |
|-----------------|------------|----------|------|---------------------|----------------------|
|                 | IEC        | JEDEC    | EIAJ |                     |                      |
| SOT136-1        | 075E06     | MS-013AE |      |                     | 91-08-13<br>95-01-24 |

## Telecom microcontrollers

## PCF84C21A; PCF84C41A; PCF84C81A

### 14 SOLDERING

#### 14.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

#### 14.2 DIP

##### 14.2.1 SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ( $T_{stg\ max}$ ). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

##### 14.2.2 REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

#### 14.3 SO

##### 14.3.1 REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

##### 14.3.2 WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

##### 14.3.3 REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

## Telecom microcontrollers

PCF84C21A; PCF84C41A;  
PCF84C81A**15 DEFINITIONS**

|   |   |
|---|---|
| <b>Data sheet status</b>  |   |
| Objective specification   | This data sheet contains target or goal specifications for product development.       |
| Preliminary specification   | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification   | This data sheet contains final product specifications.                                |
| <b>Limiting values</b>  |   |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. |   |
| <b>Application information</b>  |   |
| Where application information is given, it is advisory and does not form part of the specification.   |   |

**16 LIFE SUPPORT APPLICATIONS**

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**NOTES**

# Philips Semiconductors – a worldwide company

**Argentina:** see South America

**Australia:** 34 Waterloo Road, NORTH RYDE, NSW 2113,  
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

**Austria:** Computerstr. 6, A-1101 WIEN, P.O. Box 213,  
Tel. +43 1 60 101, Fax. +43 1 60 101 1210

**Belarus:** Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,  
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

**Belgium:** see The Netherlands

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**Bulgaria:** Philips Bulgaria Ltd., Energoproject, 15th floor,  
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Tel. +359 2 689 211, Fax. +359 2 689 102

**Canada:** PHILIPS SEMICONDUCTORS/COMPONENTS,  
Tel. +1 800 234 7381

**China/Hong Kong:** 501 Hong Kong Industrial Technology Centre,  
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,  
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**Colombia:** see South America

**Czech Republic:** see Austria

**Denmark:** Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,  
Tel. +45 32 88 2636, Fax. +45 31 57 1949

**Finland:** Sinikalliontie 3, FIN-02630 ESPOO,  
Tel. +358 9 615800, Fax. +358 9 61580/xxx

**France:** 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,  
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

**Germany:** Hammerbrookstraße 69, D-20097 HAMBURG,  
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

**Greece:** No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,  
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

**Hungary:** see Austria

**India:** Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd.  
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**Indonesia:** see Singapore

**Ireland:** Newstead, Clonskeagh, DUBLIN 14,  
Tel. +353 1 7640 000, Fax. +353 1 7640 200

**Israel:** RAPAC Electronics, 7 Kehilat Saloniki St, TEL AVIV 61180,  
Tel. +972 3 645 0444, Fax. +972 3 649 1007

**Italy:** PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,  
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

**Japan:** Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,  
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

**Korea:** Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,  
Tel. +82 2 709 1412, Fax. +82 2 709 1415

**Malaysia:** No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,  
Tel. +60 3 750 5214, Fax. +60 3 757 4880

**Mexico:** 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,  
Tel. +9-5 800 234 7381

**Middle East:** see Italy

**Netherlands:** Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,  
Tel. +31 40 27 82785, Fax. +31 40 27 88399

**New Zealand:** 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,  
Tel. +64 9 849 4160, Fax. +64 9 849 7811

**Norway:** Box 1, Manglerud 0612, OSLO,  
Tel. +47 22 74 8000, Fax. +47 22 74 8341

**Philippines:** Philips Semiconductors Philippines Inc.,  
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,  
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

**Poland:** Ul. Lukiska 10, PL 04-123 WARSZAWA,  
Tel. +48 22 612 2831, Fax. +48 22 612 2327

**Portugal:** see Spain

**Romania:** see Italy

**Russia:** Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,  
Tel. +7 095 247 9145, Fax. +7 095 247 9144

**Singapore:** Lorong 1, Toa Payoh, SINGAPORE 1231,  
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**Slovakia:** see Austria

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**South Africa:** S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,  
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,  
Tel. +27 11 470 5911, Fax. +27 11 470 5494

**South America:** Rua do Rocio 220, 5th floor, Suite 51,  
04552-903 São Paulo, SÃO PAULO - SP, Brazil,  
Tel. +55 11 821 2333, Fax. +55 11 829 1849

**Spain:** Balmes 22, 08007 BARCELONA,  
Tel. +34 3 301 6312, Fax. +34 3 301 4107

**Sweden:** Kottbygatan 7, Akalla, S-16485 STOCKHOLM,  
Tel. +46 8 632 2000, Fax. +46 8 632 2745

**Switzerland:** Allmendstrasse 140, CH-8027 ZÜRICH,  
Tel. +41 1 488 2686, Fax. +41 1 481 7730

**Taiwan:** PHILIPS TAIWAN Ltd., 23-30F, 66,  
Chung Hsiao West Road, Sec. 1, P.O. Box 22978,  
TAIPEI 100, Tel. +886 2 382 4443, Fax. +886 2 382 4444

**Thailand:** PHILIPS ELECTRONICS (THAILAND) Ltd.,  
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Tel. +66 2 745 4090, Fax. +66 2 398 0793

**Turkey:** Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,  
Tel. +90 212 279 2770, Fax. +90 212 282 6707

**Ukraine:** PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,  
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

**United Kingdom:** Philips Semiconductors Ltd., 276 Bath Road, Hayes,  
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

**United States:** 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,  
Tel. +1 800 234 7381

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**Yugoslavia:** PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,  
Tel. +381 11 625 344, Fax. +381 11 635 777

**For all other countries apply to:** Philips Semiconductors, Marketing & Sales Communications,  
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