PARADIGM®

PDM4M4040

128K x 32 CMOS Static RAM Module

Features

- ☐ High density 4 megabit Static RAM module
- ☐ Low profile 64-pin ZIP (Zig-zag In-line vertical Package) or 64-pin SIMM (Single In-line Memory Module)
- ☐ Fast access time: 12 ns (max.)
- ☐ Surface mounted plastic components on an epoxy laminate (FR-4) substrate
- ☐ Single 5V (±10%) power supply
- ☐ Multiple V_{SS} pins and decoupling capacitors for maximum noise immunity
- ☐ Inputs/outputs directly TTL compatible

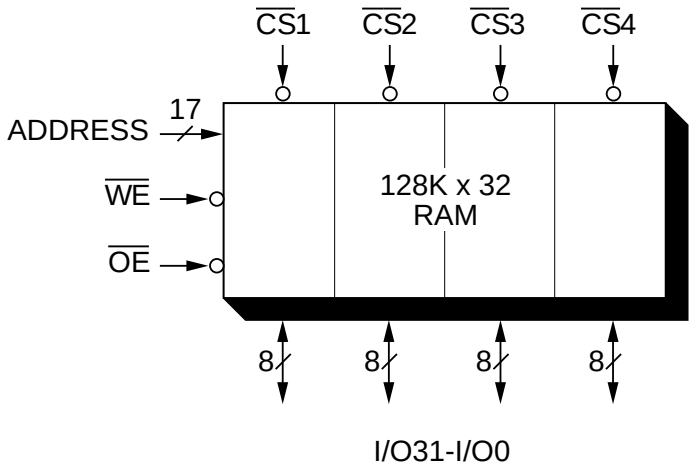
Description

The PDM4M4040 is a 128K x 32 static RAM module constructed on an epoxy laminate (FR-4) substrate using four 128K x 8 static RAMs in plastic SOJ packages. The PDM4M4040 is available with access times as fast as 12 ns with minimal power consumption.

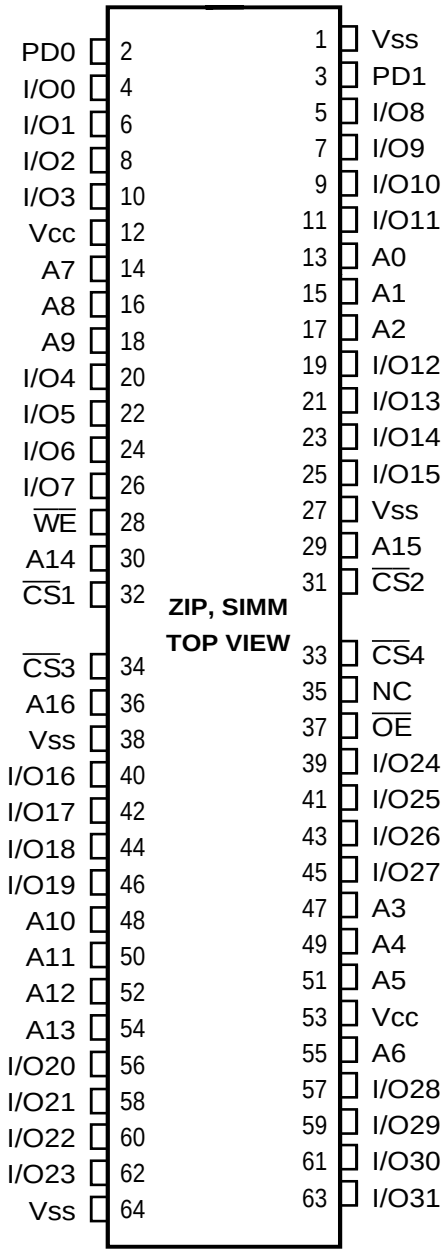
The PDM4M4040 is packaged in a 64-pin FR-4 ZIP (Zig-zag In- line vertical Package) or a 64-pin SIMM (Single In-line Memory Module). The ZIP configuration allows 64 pins to be placed on a package 3.65″ long and 0.21″ wide. At only 0.60″ high, this low-profile package is ideal for systems with minimum board spacing. The SIMM configuration allows use of edge mounted sockets to secure the module.

All inputs and outputs of the PDM4M4040 are TTL compatible and operate from a single 5V supply. Full asynchronous circuitry requires no clock or refresh for operation and provides equal access and cycle times for ease of use.

Functional Block Diagram



Pin Configuration(1)



PD0 - Vss
PD1 - NC

Pin Assignment

Pin	Signal
I/O31-I/O0	Data Inputs/Outputs
A16-A0	Addresses
$\overline{CS4}$-$\overline{CS1}$	Chip Selects
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power
V_{SS}	Ground
NC	No Connect

Truth Table

Mode	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Output	Power
Deselect/ Power-down	H	X	X	High-Z	Standby
Read	L	L	H	$DATA_{OUT}$	Active
Write	L	X	L	$DATA_{IN}$	Active
Deselect	L	H	H	High-Z	Active

Absolute Maximum Ratings(1)

Symbol	Rating	Com'l.	Ind.	Unit
V_{TERM}	Terminal Voltage with Respect to V_{SS}	–0.5 to +7.0	–0.5 to +7.0	V
T_{BIAS}	Temperature Under Bias	–10 to +85	–10 to +85	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
T_A	Operating Temperature	0 to +70	0 to +70	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
V_{SS}	Supply Voltage	0	0	0	V
Commercial	Ambient Temperature	0	25	70	°C

DC Electrical Characteristics (V_{CC} = 5.0V ± 5%, T_A = 0°C to 70°C)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
I_{LI}	Input Leakage Current (Address $\overline{WE}$, and $\overline{OE}$)	V_{CC} = Max.,V_{IN} = V_{SS} to V_{CC}	—	40	µA
I_{LI}	Input Leakage Current (Data and $\overline{CS}$)	V_{CC} = Max., V_{IN} = V_{SS} to V_{CC}	—	10	µA
I_{LO}	Output Leakage Current	V_{OUT} = V_{SS} to V_{CC}, V_{CC} = Max., $\overline{CS}$ = V_{IH}	—	10	µA
V_{OL}	Output Low Voltage	I_{OL} = 8 mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OL} = –4 mA, V_{CC} = Min.	2.4	—	V
V_{IH}	Input High Voltage		2.2	5.8	V
V_{IL}	Input Low Voltage		–0.5[1]	0.8	V

NOTE 1. V_{IL} = –3.0V for pulse widths less than 10 ns, once per cycle.

Power Supply Characteristics

Symbol	Parameter	Max[1]	Unit
I_{CC}	Operating Current $\overline{CS}$ = V_{IL}, V_{CC} = Max., f = f_{MAX}, Outputs Open	680	mA
I_{SB}	Standby Current $\overline{CS}$ ≥ V_{IH}, V_{CC} = Max., f = f_{MAX}, Outputs Open	160	mA
I_{SB1}	Full Standby Current $\overline{CS}$ ≥ V_{CC} – 0.2V, f = 0, V_{IN} > V_{CC} – 0.2V or < 0.2V	60	mA

NOTE 1. Preliminary specification only.

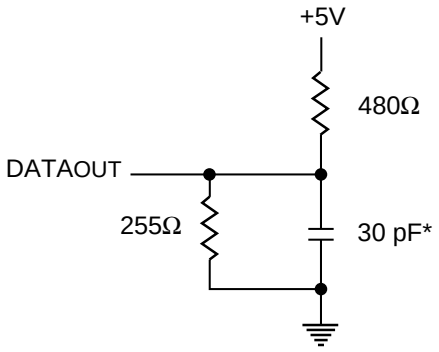
Capacitance[1] (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Max.	Unit
$C_{IN(D)}$	Input Capacitance, (Data and $\overline{CS}$) V_{IN} = 0V	12	pF
$C_{IN(A)}$	Input Capacitance, (Address, $\overline{WE}$, and $\overline{OE}$) V_{IN} = 0V	40	pF
C_{OUT}	Output Capacitance, V_{OUT} = 0V	12	pF

NOTE 1. This parameter is determined by device characteristics but is not production tested.

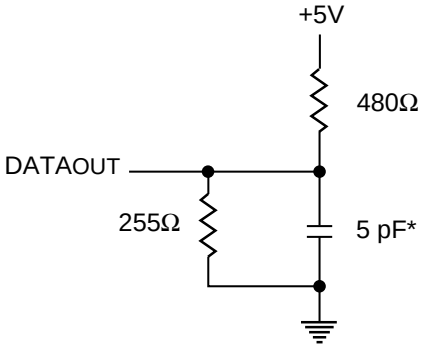
AC Test Conditions

Input Pulse Levels	V_{SS} to 3.0V
Input Rise/Fall Times	5 ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2



* Including scope and jig capacitances

Figure 1. Output Load



* Including scope and jig capacitances

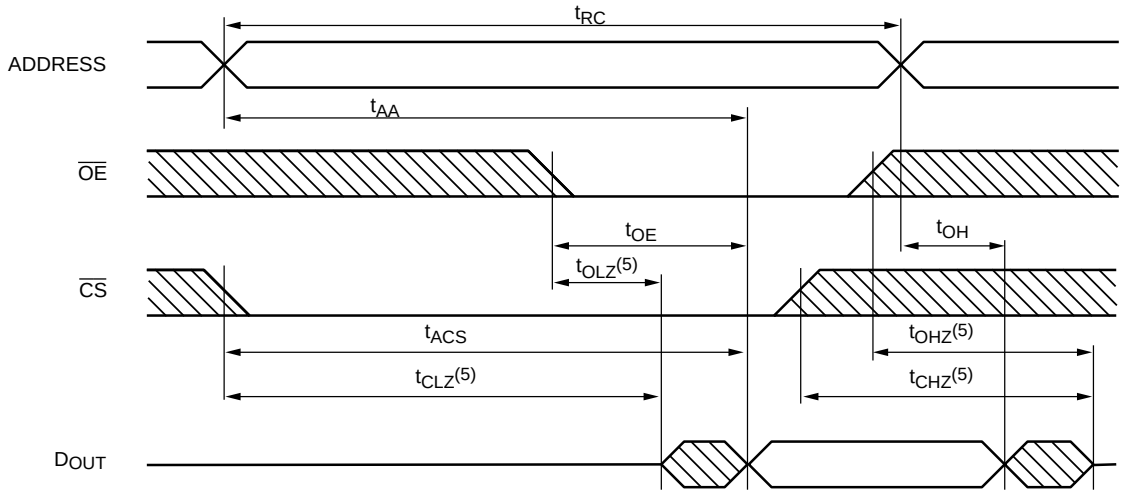
Figure 2. Output Load
(for t_{OHZ}, t_{CHZ}, t_{OLZ}, and t_{CLZ})

AC Electrical Characteristics (Vcc = 5V ± 5%, T_A = 0°C to +70°C)

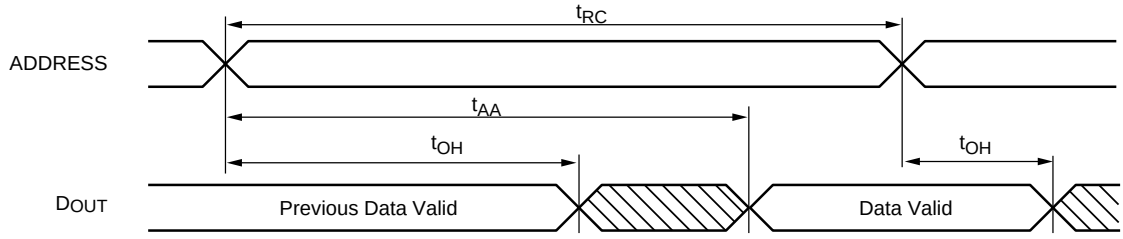
Symbol	Parameter	PDM4M4040SXXZ, PDM4M4040SXXM								Unit
		-12 ns		-15 ns		-20 ns		-25 ns		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{RC}	Read Cycle Time	12	—	15	—	20	—	25	—	ns
t_{AA}	Address Access Time	—	12	—	15	—	20	—	25	ns
t_{ACS}	Chip Select Access Time	—	12	—	15	—	20	—	25	ns
t_{CLZ}(1)	Chip Select to Output in Low-Z	2	—	3	—	3	—	3	—	ns
t_{OE}	Output Enable to Output Valid	—	7	—	8	—	10	—	12	ns
t_{OLZ}(1)	Output Enable to Output in Low-Z	0	—	0	—	0	—	0	—	ns
t_{CHZ}(1)	Chip Deselect to Output in High-Z	—	7	—	10	—	12	—	15	ns
t_{OHZ}(1)	Output Disable to Output in High-Z	—	7	—	10	—	12	—	15	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	3	—	ns
t_{PU}(1)	Chip Select to Power-Up Time	0	—	0	—	0	—	0	—	ns
t_{PD}(1)	Chip Deselect to Power-Down Time	—	12	—	15	—	20	—	25	ns
Write Cycle										
t_{WC}	Write Cycle Time	12	—	15	—	20	—	25	—	ns
t_{CW}	Chip Select to End of Write	10	—	13	—	18	—	20	—	ns
t_{AW}	Address Valid to End of Write	11	—	13	—	18	—	20	—	ns
t_{AS}	Address Setup Time	1	–	0	–	0	—	0	—	ns
t_{WP}	Write Pulse Width	10	—	13	—	18	—	20	—	ns
t_{WR}	Write Recovery Time	0	—	3	—	3	—	3	—	ns
t_{WHZ}(1)	Write Enable to Output in High-Z	—	7	—	11	—	13	—	15	ns
t_{DW}	Data to Write Time Overlap	7	—	10	—	12	—	15	—	ns
t_{DH}	Data Hold from Write Time	1	—	0	—	0	—	0	—	ns
t_{OW}(1)	Output Active from End of Write	2	—	0	—	0	—	0	—	ns

NOTE 1. This parameter is determined by device characteristics but is not production tested.

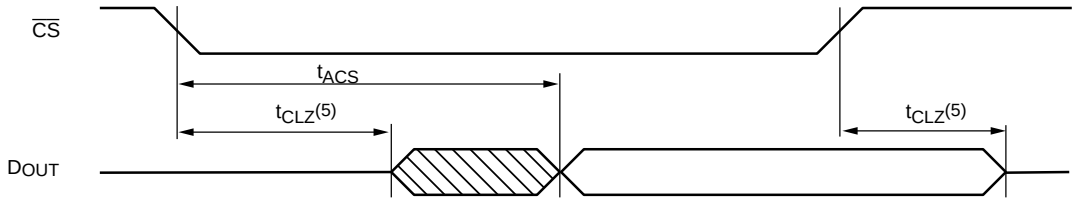
Timing Waveforms of Read Cycle No.1(1)



Timing Waveforms of Read Cycle No.2(1,2,4)

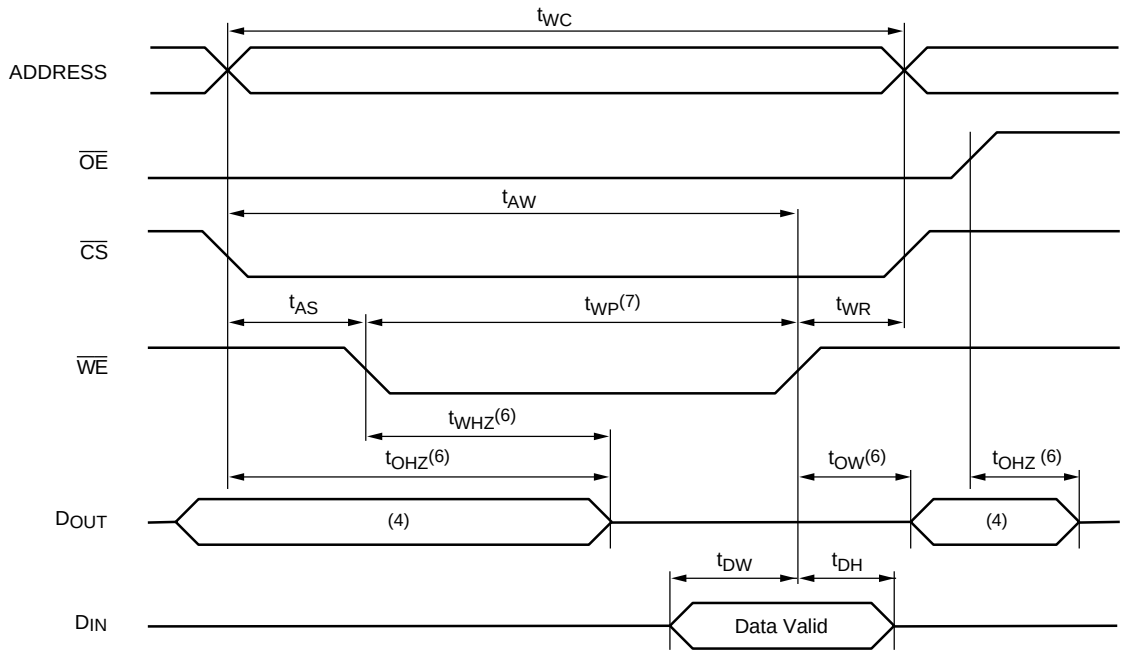


Timing Waveforms of Read Cycle No.3(1,3,4)

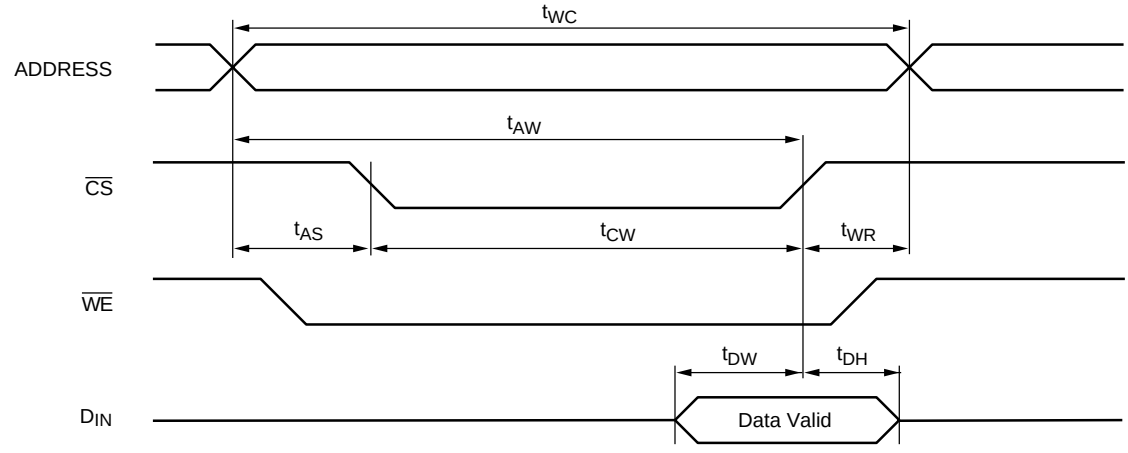


NOTES 1. $\overline{WE}$ is HIGH for Read Cycle.
2. Device is continuously selected. $\overline{CS} = V_{IL}$.
3. Address valid prior to or coincident with $\overline{CS}$ transition LOW.
4. $\overline{OE} = V_{IL}$.
5. Transition is measured ±200 mV for steady state. This parameter is determined by device characteristics but is not production tested.

Timing Waveforms of Write Cycle No.1 ($\overline{WE}$ Controlled)(1,2,3,7)



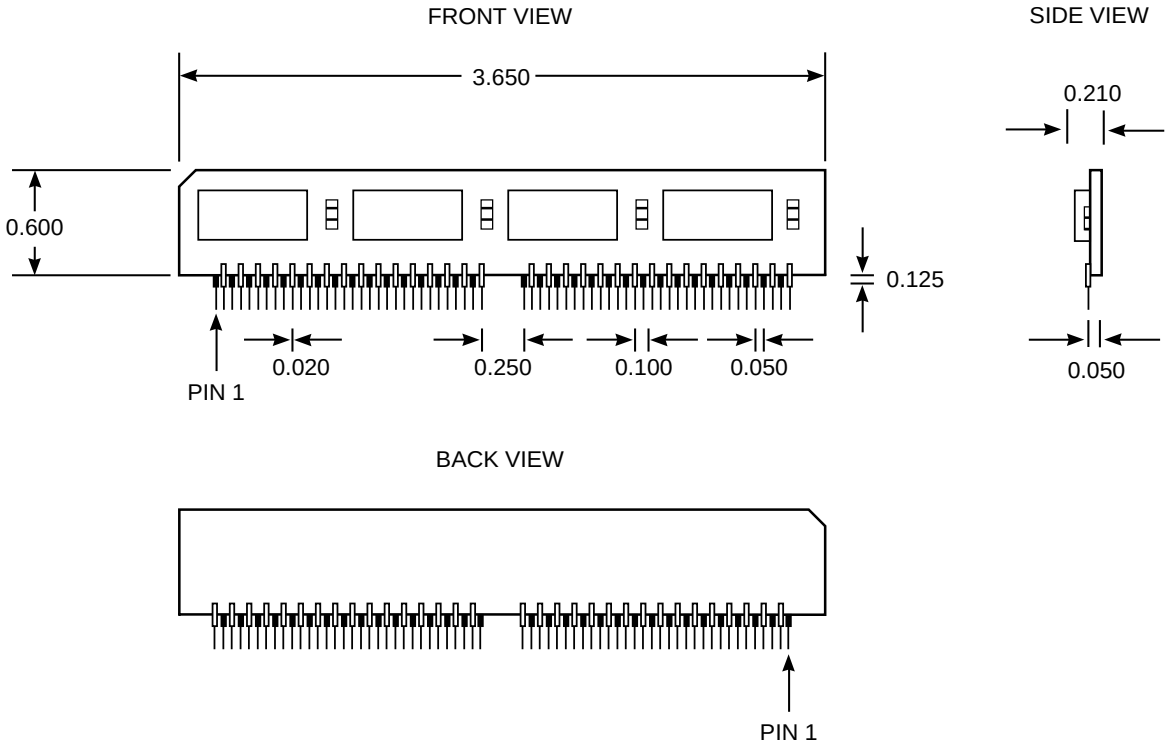
Timing Waveforms of Write Cycle No.2 ($\overline{CS}$ Controlled)(1,2,3,5)



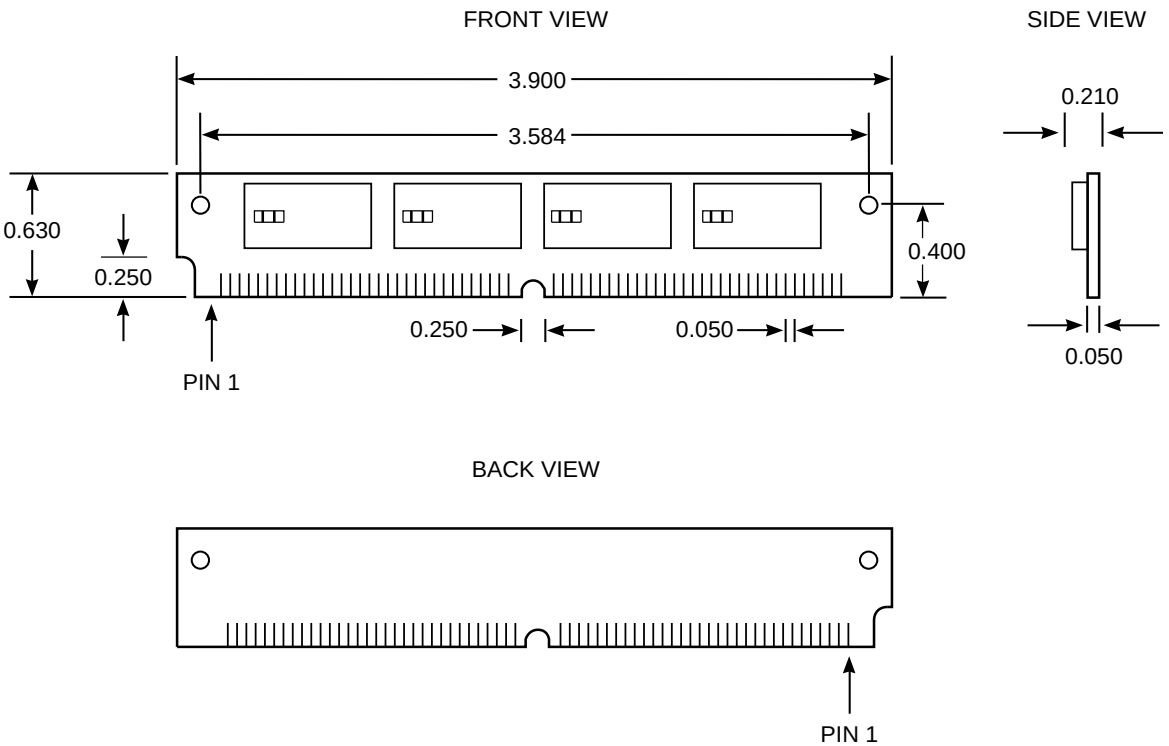
NOTES 1. $\overline{WE}$ or $\overline{CS}$ must be HIGH during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a LOW $\overline{CS}$ and a LOW $\overline{WE}$.
3. t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going HIGH to end the write cycle.
4. During this period, I/O pins are in the output state, and input signals must be applied.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with or after the $\overline{WE}$ LOW transition, the outputs remain in a high-impedance state.
6. Transition is measured ±200 mV for steady state with a 5 pF load (including scope and jig). This parameter is determined by device characteristics but is not production tested.
7. If $\overline{OE}$ is LOW during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WHZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is HIGH during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse width can be as short as the specified t_{WP}.

Package Dimensions

ZIP Version



SIMM Version



Ordering Information