Peregrine Semiconductor

Product Specification

PE926C31

Quad RS-422 Differential Line Driver Radiation Hardened

Features

- High-speed operation: < 10 nS typical
- Low power: < 150 uA typical (unloaded)
- 3.3 V operation
- Standard packaging: 16-lead flat pack
- SEL Immune UTSi CMOS-on-sapphire
- SEU <10-10 errors / bit-day
- 300 Krad Total Dose

Product Description

The PE926C31 is a high performance monolithic CMOS RS-422 line driver. Its operating supply range is 3.0 to 3.6 V, with an output signal overvoltage range of 0 – 6 V. The PE26C31 offers higher speed and lower power than other RS-422 driver types. It is packaged in a flat pack and is ideal for space applications.

The PE926C31 is manufactured in Peregrine's patented Ultra Thin Silicon (UTSi®) CMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Package Drawing

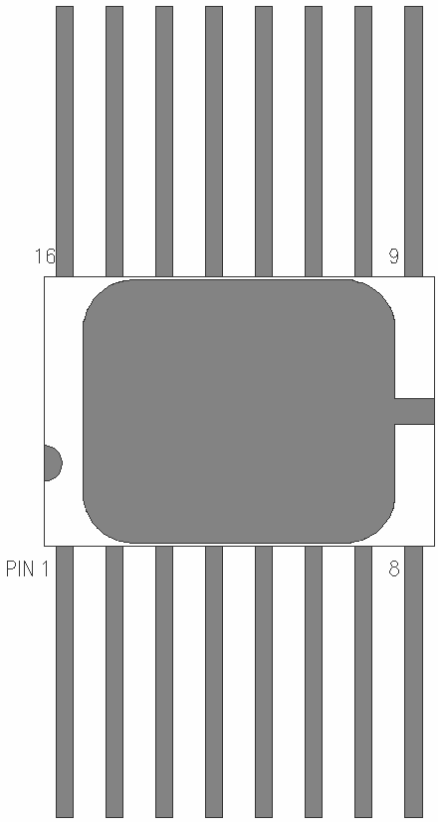

Figure 2. Pin Configuration (Top View)

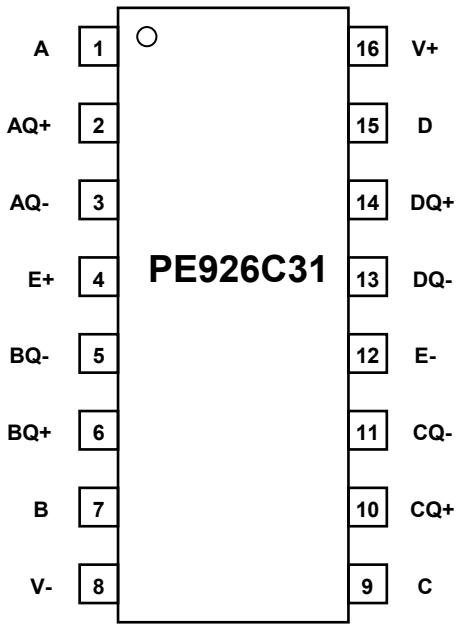

Table 1. Pin Descriptions

Pin No.	Pin Name	Description
1	A	Channel A Input
2	AQ+	Channel A Noninverting Ouput
3	AQ-	Channel A Inverting Output
4	E+	Enable, active high
5	BQ-	Channel B Inverting Output
6	BQ+	Channel B Noninverting Output
7	B	Channel B Input
8	V-	Ground Pin
9	C	Channel C Input
10	CQ+	Channel C Noninverting Output
11	CQ-	Channel C Inverting Ouput
12	E-	Enable, active low
13	DQ-	Channel D Inverting Output
14	DQ+	Channel D Noninverting Output
15	D	Channel D Input
16	V+	Supply Pin

Table 2. Recommended Operating Conditions

Symbol	Parameter/Conditions	Min	Max	Units
V+	Supply voltage	3.0	3.6	V
T_{OP}	Operating temperature range	-55	125	°C
VIN	Maximum input voltage	0	Vdd	V
VOUT	Maximum output voltage	0	Vdd	V
IOUT	Maximum output current	-50	50	mA

Electrostatic Discharge (ESD) Precautions

When handling this UTSi device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 2.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS™ devices are immune to latch-up.

Device Functional Considerations

The PE926C31 operates at high switching speeds. In order to obtain maximum performance, it is crucial that pin 16 be supplied with a bypass capacitor to ground (pin 8).

Table 3. Truth Table

E+	E-	Data	Q+	Q-
L	H	X	Z	Z
H	X	L	L	H
X	L			
H	X	H	H	L
X	L			

Table 4. Electrical Specifications

-55° C < Tcase < 125° C, 3.0 V < V+ < 3.6 V, PreRad, unless otherwise specified

Param	Description	Conditions	Pin(s)	Min	Typ	Max	Units
VD1	Output Differential Voltage	No load	AQ+, AQ-, BQ+, BQ-, CQ+, CQ-, DQ+, DQ-	(V+) -0.3	(V+)	(V+) +0.6	V
VD2	Output Differential Voltage	RL=100 Ω, Fig DC1		1.9	2.3		V
DVD2	Output Differential Voltage Change	IOUT 0 – 20mA, Fig DC1		-0.4	0	0.4	V
VCM	Common Mode Voltage	RL=100 Ω, Fig DC1			1.5	2.0	V
DVCM	Common Mode Voltage Change	RL=100 Ω, Fig DC1		-0.4	0	0.4	V
IOZH	Tristate Output Leakage (H)	VOUT = V+, disabled		-5	-0.1		uA
IOZL	Tristate Output Leakage (L)	VOUT = 0.0 V, disabled			0.1	5	uA
IOSC	Output Short Circuit Current	VOUT = 0.0 V, Enabled Q=H		-30	-70	-100	mA
IOFFH	Output Leakage Current (H)	VOUT=6.0V,V+ and all inputs = 0.0V			1	100	uA
IOFFL	Output Leakage Current (L)	VOUT=-0.25V,V+ and all inputs = 0.0V		-100	-1		uA
VOH	Output High Voltage	Iout=-20mA		2.0	2.4		V
VOL	Output Low Voltage	Iout=20mA			0.1	0.5	V
VIH	Input threshold H	Vdd=3.6V (VIHMIN=0.7*VDD)	A, B, C, D, E+, E-	2.5			V
VIL	Input Threshold L	Vdd=3.0V (VILMAX=0.3*VDD)	A, B, C, D, E+, E-			0.9	V
IIH	Input Lkg Current		A, B, C, D, E+, E-	-1		1	uA
IIL	Input Lkg Current		A, B, C, D, E+, E-	-1		1	uA
VIKL	Input Clamp Diode Voltage	IIN=-20 mA	A, B, C, D, E+, E-	-1.5			
VIKH	Input Clamp Diode Voltage	IIN=20 mA	A, B, C, D, E+, E-			(V+) + 1.5 V	µ
ICC	Supply Current	No load, Inputs = 0 V or V+	V+		120 uA	150 uA	

Notes: 1. “Line” pins refer to AQ-, AQ+, BQ-, BQ+, CQ-, CQ+, DQ-, DQ+, differential outputs
2. “Digital Input” or “Enable” pins refer to E+, E-
3. “Digital Input” pins refer to A, B, C, D

Table 5. Post-Irradiation DC Electrical Specifications

Tcase = 25° C, 3.0 V < V+ < 3.6 V, 300 KRad, unless otherwise specified

Param	Description	Conditions	Pin(s)	Min	Typ	Max	Units
VD1	Output Differential Voltage	No load	AQ+, AQ-, BQ+, BQ-, CQ+, CQ-, DQ+, DQ-	(V+) -0.3	(V+)	(V+) +0.6	V
VD2	Output Differential Voltage	RL=100 Ω, Fig DC1		1.9	2.3		V
DVD2	Output Differential Voltage Change	IOUT 0 – 20mA, Fig DC1		-0.4	0	0.4	V
VCM	Common Mode Voltage	RL=100 Ω, Fig DC1			1.5	2.0	V
DVCM	Common Mode Voltage Change	RL=100 Ω, Fig DC1		-0.4	0	0.4	V
IOZH	Tristate Output Leakage (H)	VOUT = V+, disabled		-5	-0.1		uA
IOZL	Tristate Output Leakage (L)	VOUT = 0.0 V, disabled			0.1	5	uA
IOSC	Output Short Circuit Current	VOUT = 0.0 V, Enabled Q=H		-30	-70	-100	mA
IOFFH	Output Leakage Current (H)	VOUT=6.0V,V+ and all inputs = 0.0V			1	100	uA
IOFFL	Output Leakage Current (L)	VOUT=-0.25V,V+ and all inputs = 0.0V		-100	-1		uA
VOH	Output High Voltage	Iout=-20mA		2.0	2.4		V
VOL	Output Low Voltage	Iout=20mA			0.1	0.5	V
VIH	Input threshold H	Vdd=3.6V (VIHMIN=0.7*VDD)	A, B, C, D, E+, E-	2.5			V
VIL	Input Threshold L	Vdd=3.0V (VILMAX=0.3*VDD)	A, B, C, D, E+, E-			0.9	V
IIH	Input Lkg Current		A, B, C, D, E+, E-	-1		1	uA
IIL	Input Lkg Current		A, B, C, D, E+, E-	-1		1	uA
VIKL	Input Clamp Diode Voltage	IIN=-20 mA	A, B, C, D, E+, E-	-1.5			
VIKH	Input Clamp Diode Voltage	IIN=20 mA	A, B, C, D, E+, E-			(V+) + 1.5 V	
ICC	Supply Current	No load, Inputs = 0 V or V+	V+		120 uA	150 uA	

Notes: 1. “Line” pins refer to AQ-, AQ+, BQ-, BQ+, CQ-, CQ+, DQ-, DQ+, differential outputs
2. “Digital Input” or “Enable” pins refer to E+, E-
3. “Digital Input” pins refer to A, B, C, D
4. Output Short Circuit not intended to imply continuous operation

Table 6. Pre-irradiation Electrical Specifications

-55° C < Tcase < 125° C, 3.0 V < V+ < 3.6 V, PreRad, unless otherwise specified

Param	Description	Conditions	Pin(s)	Min	Typ	Max	Units
TPHL	Prop Delay H-L	RL=100 CL=50 pF	AQ+, AQ-, BQ+, BQ-, CQ+, CQ-, DQ+, DQ-	3	9	15	nS
TPLH	Prop Delay H-L			3	9	15	nS
TSK1	Prop Delay Q+/Q-			-3	0	3	nS
TSK2*	Prop Delay Skew Ch/Ch			-3	0	3	nS
TRISE*	Rise Time 20%/80%				3	10	nS
TFALL*	Fall Time 20%/80%				3	10	nS
TPHZ	Prop Delay H-Z				12	20	nS
TPZH	Prop Delay Z-H				12	20	nS
TPLZ	Prop Delay L-Z				10	20	nS
TPZL	Prop Delay Z-L				10	20	nS

Table 7. Post-irradiation Electrical Specifications

25° C, 3.0 V < V+ < 3.6 V, 300 KRad, unless otherwise specified

Param	Description	Conditions	Pin(s)	Min	Typ	Max	Units
TPHL	Prop Delay H-L	RL=100 CL=50 pF	AQ+, AQ-, BQ+, BQ-, CQ+, CQ-, DQ+, DQ-	3	9	15	nS
TPLH	Prop Delay H-L			3	9	15	nS
TSK1	Prop Delay Q+/Q-			-3	0	3	nS
TSK2*	Prop Delay Skew Ch/Ch			-3	0	3	nS
TRISE*	Rise Time 20%/80%				3	10	nS
TFALL*	Fall Time 20%/80%				3	10	nS
TPHZ	Prop Delay H-Z				20	20	nS
TPZH	Prop Delay Z-H				20	20	nS
TPLZ	Prop Delay L-Z				10	20	nS
TPZL	Prop Delay Z-L				10	20	nS

*****Note**:** Guaranteed by design, not tested

Figure 3. TPLH, TPHL Test Circuit Block Diagram

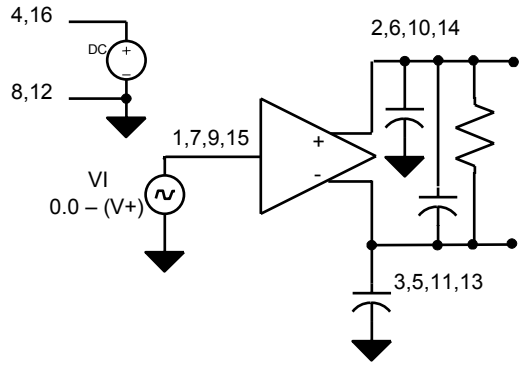

Figure 2 : TPLH, TPHL

TPLH, TPHL measured from input 50% to output 50% thresholds. TRISE, TFALL measured from output 20% to output 80% thresholds.

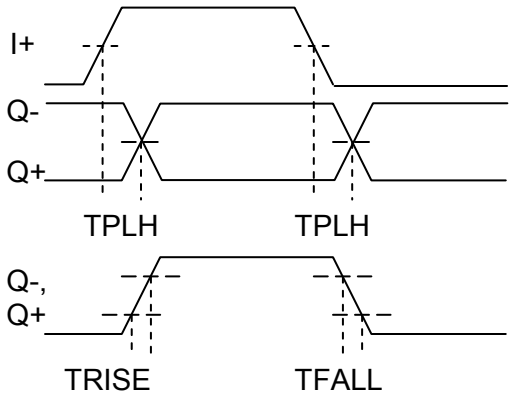

Figure 4. TPLZ, TPZL, TPHZ, TPZH Test Circuit Block Diagram

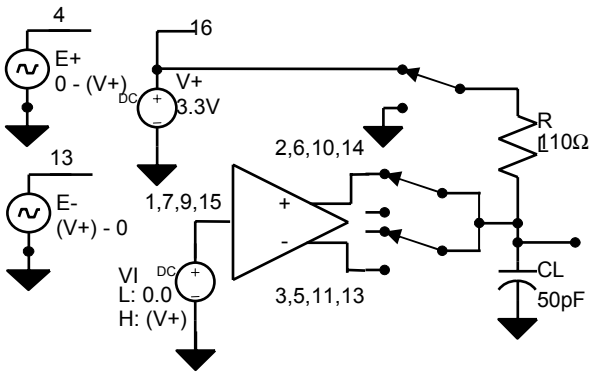

Figure 3: TPHZ, TPZH, TPLZ, TPZL

TPZH, TPZL measured from input 50% to output 50% thresholds. TPHZ, TPLZ measured from input 50% to output 10% thresholds.

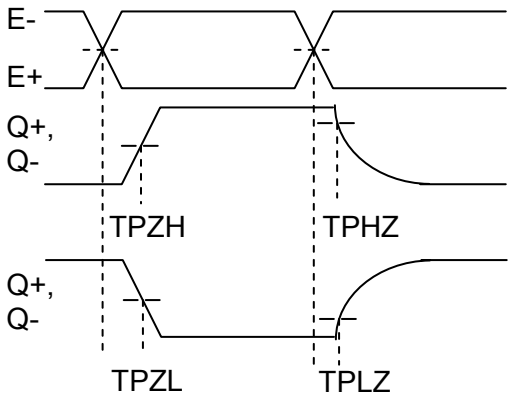

Table 8. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
926C31-01	PE926C31-01	Engineering Sample	16-lead FLAT PACK	1/Box
926C31-21	PE926C31-21	Flight Product, FP	16-lead FLAT PACK	25/Tray
926C31-00	PE926C31-EK	Evaluation Kit	Evaluation Board	1/Box

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For a list of representatives in your area, please refer to our Web site at: ***www.psemi.com***

Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

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