SIEMENS

ICs for Communications

Four Channel Codec Filter with PCM- and µ-Controller Interface SICOFI®4-µC

PEB 2466 Version 1.2

Data Sheet 02.97

DS 2

Edition 02.97

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PEB 2466 **Revision History:**	**Current Version: 02.97**
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Page (in last revision)	**Subjects (major changes regarding Preliminary Data Sheet 03.96)**
1	Featurelist updated
2-4	Chapter “Major Applications” added
5-8	Errors in pin configuration fixed Values of filter and coupling capacitors fixed Several minor clarifications
12-15	PCM interface clarified
17	Byte by byte transfer with the µC-interface added
18	Types of Commands and Databytes clarified
19-23	Several errors in programming examples fixed
25	IM-Filter changed to IM/R1-filter
32	CRAM architecture described
38	Error in definition of XR4-register fixed
39	Error in definition of XR5-register fixed
39	Definition of “crash” added
41	Figure for “setting slopes in XR6” added
45-46	Chapter about programmable filters updated
46-47	Chapter about “QSICOS” added
48	Clear separation of A-law and µ-law
49	ICN-spec updated
58	Values for power dissipation and current-consumption updated
59	Values for analog input and output resistance updated
60	Figure for selection of optimum coupling cap. added
61-64	Timing spec. figures for digital interfaces added, times updated
65	Description of Level Metering function added
68	Guidelines for Boarddesign added

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Last Revision	Data Sheet 06.96

Page (in current version)	Subjects (major changes since last revision)
4	Footnote added to the pins VDDA12 and VDDA34, reference added to footnote for filter-capacitors clarification, INT12, INT34 are active high
26	AX1 and AX2 exchanged, in figure “CUT OFFs” and Loops
27	Footnote added regarding attenuation of HPR and HPX
39	Figure “Setting of Slopes in Register XR6” updated
42	Errors in description “Standby- and Operating mode” fixed (PU bit, CR1)
44	Figure in chapter “QSICOS” clarified
45	Hint for tool “QSUCCONV.EXE” added
46	Test conditions completed
57	“Analog output load”-spec added
58	Change for clarification, R_{out} -> R_{load}
63	Figure updated (AX1 and AX2 exchanged)
64	Command description updated
65	Figure “Proposed Test Circuit” updated
66	Layout-figure updated
5, 6, 58	Coupling capacitors in transmit direction updated to 39 nF

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1 General Description

The four channel Signal Processing Codec Filter PEB 2466 SICOFI-4-µC is the logical continuation of a well established family of SIEMENS programmable codec-filter-ICs.

Its major difference to the PEB 2465 (SICOFI-4) is the PCM and µC interface, which replaces the IOM-2 interface.

The SICOFI-4-µC is a fully integrated PCM CODEC and FILTER fabricated in low power 1µ CMOS technology for applications in digital communication systems. Based on an advanced digital filter concept, the PEB 2466-H provides excellent transmission performance and high flexibility. The new filter concept (second generation) leads to a maximum of independence between the different filter blocks. Each filter block can be seen like a one to one representative of the corresponding network element.

To complete the functionality of the PEB 2466 only two external capacitors per channel are needed. The internal level accuracy is based on a very accurate bandgap reference. The frequency behaviour is mainly determined by digital filters, which do not have any fluctuations. As a result of the new ADC - and DAC - concepts linearity is only limited by second order parasitic effects. Although the device works with only one single 5 V supply there is a very good dynamic range available.

SIEMENS

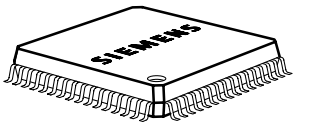
Four Channel Codec Filter with PCM- and µ-Controller Interface SICOFI®4-µC

PEB 2466

Version 1.2

CMOS

1.1 Features



P-MQFP-64

- Single chip programmable CODEC and FILTER to handle four
  - Central Office
  - or PABX-channels
- Specification according to relevant CCITT, EIA and LSSGR recommendations
- Digital signal processing technique
- Serial µ-Controller interface
- 2 programmable PCM-interfaces (up to 8 Mbit/s)
- Programmable interface to electronic SLICs and transformer solutions for signaling information
- High analog driving capability (300 Ω) for direct driving of transformers
- Programmable digital filters to adapt the transmission behaviour especially for
  - AC impedance matching
  - transhybrid balancing
  - frequency response
  - gain
  - A/µ-law conversion
- Single 5 V power supply
- Advanced low power 0.9 µm analog CMOS technology
- Low power consumption (< 35 mW per channel)
- High performance A/D conversion
- High performance D/A conversion
- Advanced test capabilities
  - five digital loops
  - four analog loops
  - two programmable tone generators (DTMF possible)
  - built in self-test
  - level metering function for system tests
- Standard P-MQFP-64 package
- Comprehensive development platform available
  - software for automatic filter coefficient calculation - QSICOS
  - Hardware development board - STSI 2466

Type	Ordering Code	Package
PEB 2466-H V1.2	on request	P-MQFP-64

1.2 Pin Configuration

(top view)

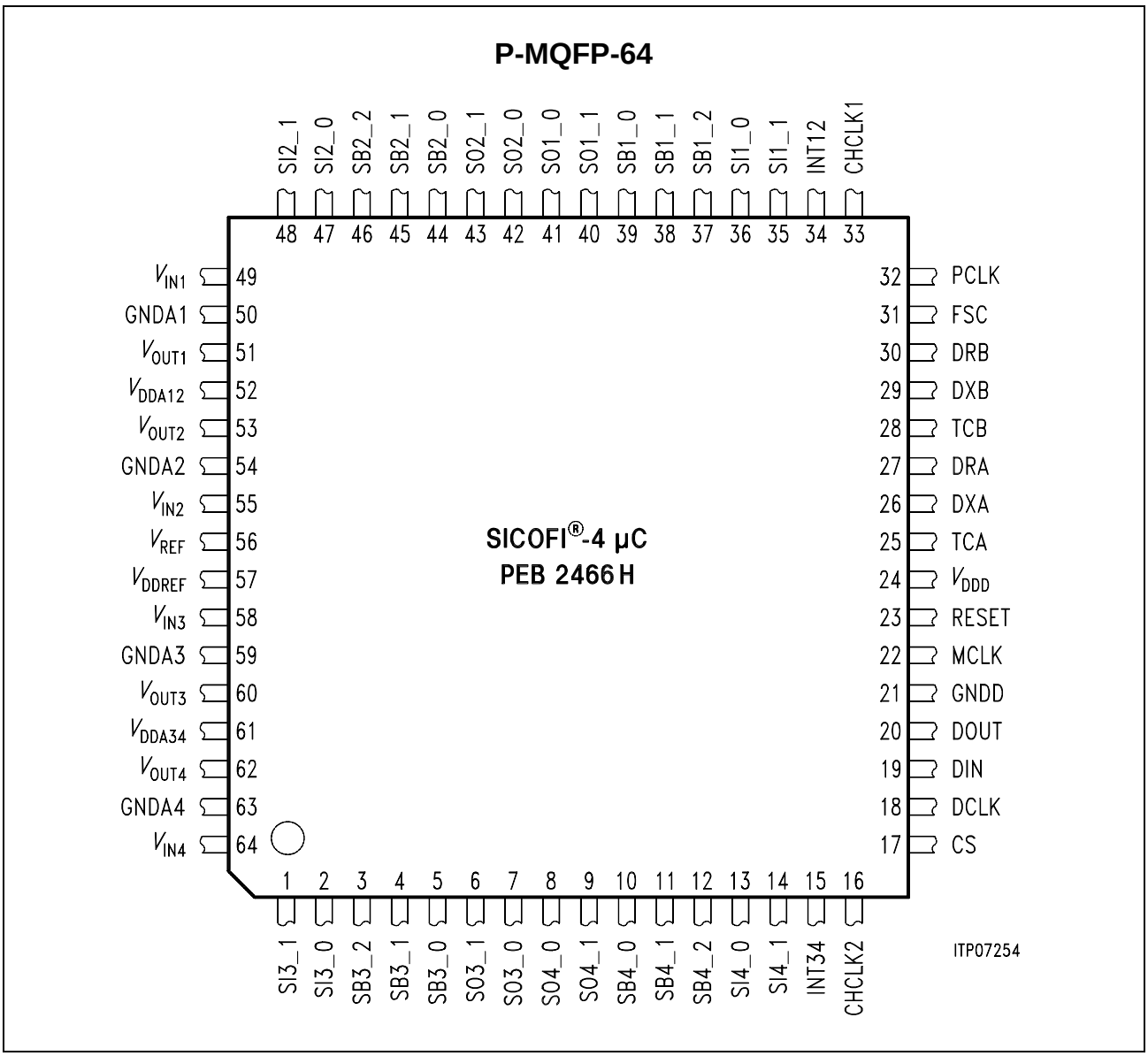


Figure 1

1.3 Pin Definition and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
Common Pins for all Channels			
24	V_{DDD}	I	+ 5 V supply for the digital circuitry [1)]
21	GNDD	I	Ground Digital, not internally connected to GNDA1,2,3,4 All digital signals are referred to this pin
52	V_{DDA12}	I	+ 5 V Analog supply voltage for channel 1 and 2 [1)]
61	V_{DDA34}	I	+ 5 V Analog supply voltage for channel 3 and 4 [1)]
56	V_{REF}	I/O	Reference voltage, has to be connected to a 220 nF cap. to ground, can also be used as virtual ground for analog inputs and outputs (high-ohmic buffer needed !!!)
57	V_{DDREF}	I	+ 5 V Analog supply voltage (100 nF cap. required)
31	FSC	I	Frame synchronization clock, 8 kHz, identifies the beginning of the frame, individual time slots are referenced to this pin, FSC must be synchronous to PCLK
32	PCLK	I	Data clock 128 to 8192 kHz, determines the rate at which PCM data is shifted into or out of the PCM-ports
30	DRB	I	PCM-interface: Receive PCM data from PCM-highway B, data for each channel is received in 8 bit bursts every 125 µs
29	DXB	O	PCM-interface: Transmit PCM data to PCM-highway B, data for each channel is transmitted in 8 bit burst every 125 µs
28	TCB	O	PCM-interface: Transmit control output B, is active if data is transmitted via DXB, active low, open drain
27	DRA	I	PCM-interface: Receive PCM data from PCM-highway A, data for each channel is received in 8 bit bursts every 125 µs
26	DXA	O	PCM-interface: Transmit PCM data to PCM-highway A, data for each channel is transmitted in 8 bit burst every 125 µs

1.3 Pin Definition and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
25	TCA	O	PCM-interface: Transmit control output A, is active if data is transmitted via DXA, active low, open drain
23	RESET	I	Reset input - forces the device to default mode, active low
22	MCLK	I	Master clock input, 1536, 2048, 4096 or 8192 kHz, synchronous to FSC, must be available if the SICOFI-4-µC is used
17	CS	I	µ-Controller interface: chip select enable to read or write data, active low
18	DCLK	I	µ-Controller interface: data clock, shifts data from or to device, the maximum clock rate is 8192 kHz
19	DIN	I	µ-Controller interface: control data input pin, DCLK determines the data rate
20	DOUT	O	µ-Controller interface: control data output pin, DCLK determines the data rate, DOUT is high 'Z' if no data is transmitted from the SICOFI-4-µC
33	CHCLK1	O	Chopper Clock output, provides a programmable (2 … 28 ms) output signal (synchronous to MCLK)
16	CHCLK2	O	Chopper Clock output, provides a 256, or 512 or 16384 kHz signal, is synchronous to MCLK
34	INT12	O	Interrupt output pin for channel 1 and 2, active high
15	INT34	O	Interrupt output pin for channel 3 and 4, active high

1.3 Pin Definition and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
Specific Pins for Channel 1			
50	GNDA1	I	Ground Analog for channel 1, not internally connected to GNDD or GNDA2,3,4
49	V_{IN1}	I	Analog voice (voltage) input for channel 1, has to be connected to the SLIC by a 39 nF cap.
51	V_{OUT1}	O	Analog voice (voltage) output for channel 1, has to be connected to the SLIC via a cap. [2)]
36	SI1_0	I	Signaling input pin 0 for channel 1
35	SI1_1	I	Signaling input pin 1 for channel 1
41	SO1_0	O	Signaling output pin 0 for channel 1
40	SO1_1	O	Signaling output pin 1 for channel 1
39	SB1_0	I/O	Bi-directional signaling pin 0 for channel 1
38	SB1_1	I/O	Bi-directional signaling pin 1 for channel 1
37	SB1_2	I/O	Bi-directional signaling pin 2 for channel 1
Specific Pins for Channel 2			
54	GNDA2	I	Ground Analog for channel 2, not internally connected to GNDD or GNDA 1,3,4
55	V_{IN2}	I	Analog voice (voltage) input for channel 2, has to be connected to the SLIC by a 39 nF cap.
53	V_{OUT2}	O	Analog voice (voltage) output for channel 2, has to be connected to the SLIC via a cap. [2)]
47	SI2_0	I	Signaling input pin 0 for channel 2
48	SI2_1	I	Signaling input pin 1 for channel 2
42	SO2_0	O	Signaling output pin 0 for channel 2
43	SO2_1	O	Signaling output pin 1 for channel 2
44	SB2_0	I/O	Bi-directional signaling pin 0 for channel 2
45	SB2_1	I/O	Bi-directional signaling pin 1 for channel 2
46	SB2_2	I/O	Bi-directional signaling pin 2 for channel 2

1.3 Pin Definition and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
Specific Pins for Channel 3			
59	GNDA3	I	Ground Analog for channel 3, not internally connected to GNDD or GNDA1,2,4
58	V_{IN3}	I	Analog voice (voltage) input for channel 3, has to be connected to the SLIC by a 39 nF cap.
60	V_{OUT3}	O	Analog voice (voltage) output for channel 3, has to be connected to the SLIC via a cap. [2)]
2	SI3_0	I	Signaling input pin 0 for channel 3
1	SI3_1	I	Signaling input pin 1 for channel 3
7	SO3_0	O	Signaling output pin 0 for channel 3
6	SO3_1	O	Signaling output pin 1 for channel 3
5	SB3_0	I/O	Bi-directional signaling pin 0 for channel 3
4	SB3_1	I/O	Bi-directional signaling pin 1 for channel 3
3	SB3_2	I/O	Bi-directional signaling pin 2 for channel 3

1.3 Pin Definition and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
Specific Pins for Channel 4			
63	GNDA4	I	Ground Analog for channel 4, not internally connected to GNDD or GNDA1,2,3
64	V_{IN4}	I	Analog voice (voltage) input for channel 4, has to be connected to the SLIC by a 39 nF cap.
62	V_{OUT4}	O	Analog voice (voltage) output for channel 4, has to be connected to the SLIC via a cap. [2]
13	SI4_0	I	Signaling input pin 0 for channel 4
14	SI4_1	I	Signaling input pin 1 for channel 4
8	SO4_0	O	Signaling output pin 0 for channel 4
9	SO4_1	O	Signaling output pin 1 for channel 4
10	SB4_0	I/O	Bi-directional signaling pin 0 for channel 4
11	SB4_1	I/O	Bi-directional signaling pin 1 for channel 4
12	SB4_2	I/O	Bi-directional signaling pin 2 for channel 4

[1] A 100 nF cap. should be used for blocking these pins, see also on page 82

[2] The value for the capacitor needed, depends on the input impedance of the 'SLIC'-circuitry. For choosing the appropriate values see figure on page 71.

2 Functional Description

2.1 SICOFI®-4-µC Principles

The change from 2 µm to 1 µm CMOS process requires new concepts in the realization of the analog functions. High performance (in the terms of gain, speed, stability …) 1 µm CMOS devices cannot withstand more than 5.5 V of supply-voltage. On that account the negative supply voltage VSS of the previous SICOFIs is omitted. This is a benefit for the user but it makes a very high demand on the analog circuitry.

ADC and DAC are changed to Sigma-Delta-concepts to fulfill the stringent requirements on the dynamic parameters.

Using 1 µm CMOS does not only lead to problems - it is the only acceptable solution in terms of area and power consumption for the integration of more than two SICOFI channels on a single chip.

It is rather pointless to implement 4 codec-filter-channels on one chip with pure analog circuitry. The use of a DSP-concept (the SICOFI and the SICOFI-2-approach) for this function is a must for an adequate four channel architecture.

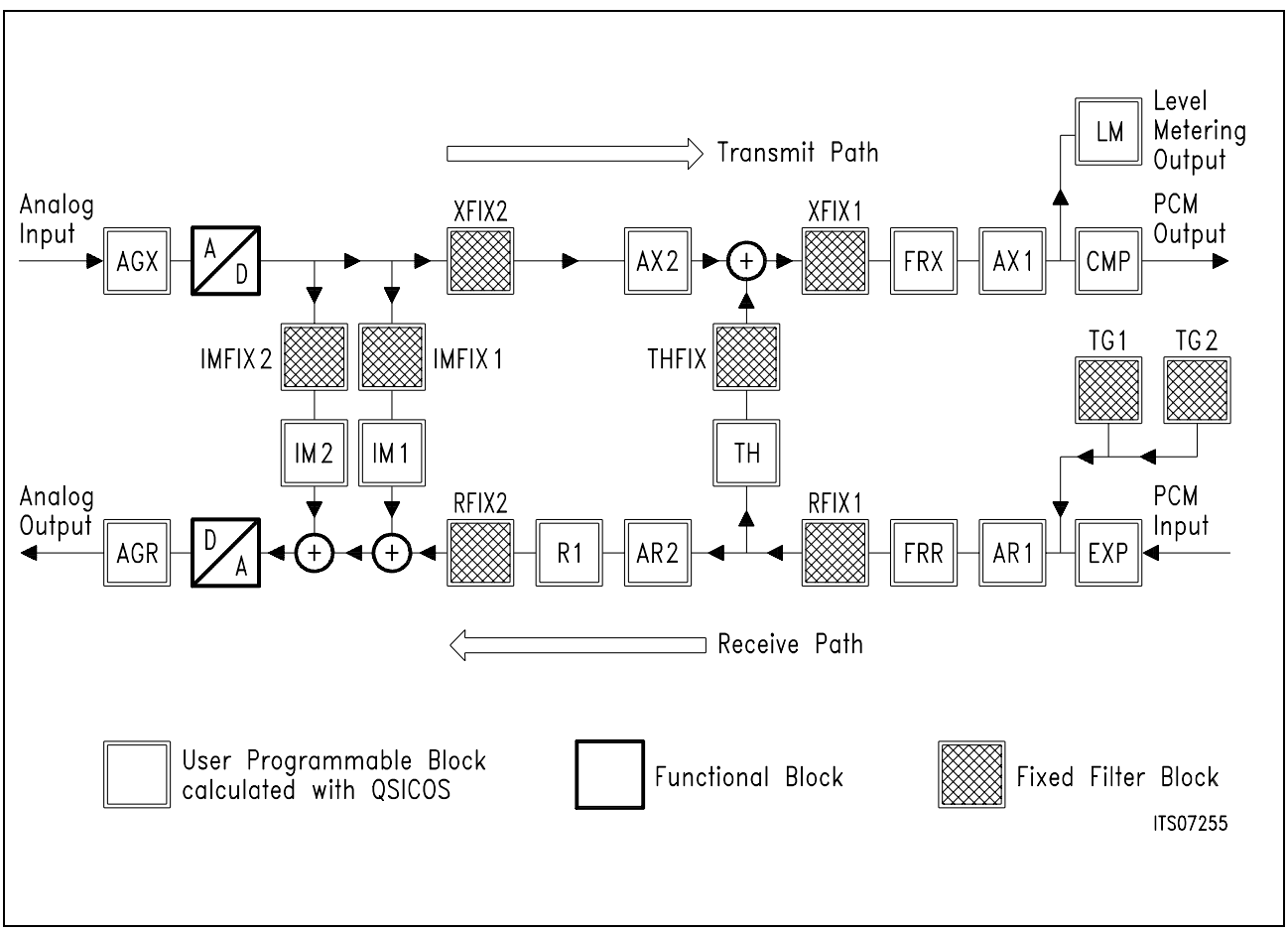


Figure 2
SICOFI®-4 µC Signal Flow Graph (for any channel)

Transmit Path

The analog input signal has to be DC-free connected by an external capacitor because there is an internal virtual reference ground potential. After passing a simple antialiasing prefilter (PREFI) the voice signal is converted to a 1-bit digital data stream in the Sigma-Delta-converter. The first downsampling steps are done in fast running digital hardware filters. The following steps are implemented in the micro-code which has to be executed by the central Digital Signal Processor. This DSP-machine is able to handle the workload for all four channels. At the end the fully processed signal (flexibly programmed in many parameters) is transferred to the PCM- interface in a PCM-compressed signal representation.

Receive Path

The digital input signal is received via the PCM interface. Expansion, PCM-Law-pass-filtering, gain correction and frequency response correction are the next steps which are done by the DSP-machine. The upsampling interpolation steps are again processed by fast hardware structures to reduce the DSP-workload. The upsampled 1-bit data stream is then converted to an analog equivalent which is smoothed by a POST-Filter (POFI). As the signal V_{OUT} is also referenced to an internal virtual ground potential, an external capacitor is required for DC-decoupling.

Loops

There are two loops implemented. The first is to generate the AC-input impedance (IM) and the second is to perform a proper hybrid balancing (TH). A simple extra path IM2 (from the transmit to the receive path) supports the impedance matching function.

Test Features

There are four analog and five digital test loops implemented in the SICOFI-4. For special tests it is possible to Cut Off the receive and the transmit path at two different points.

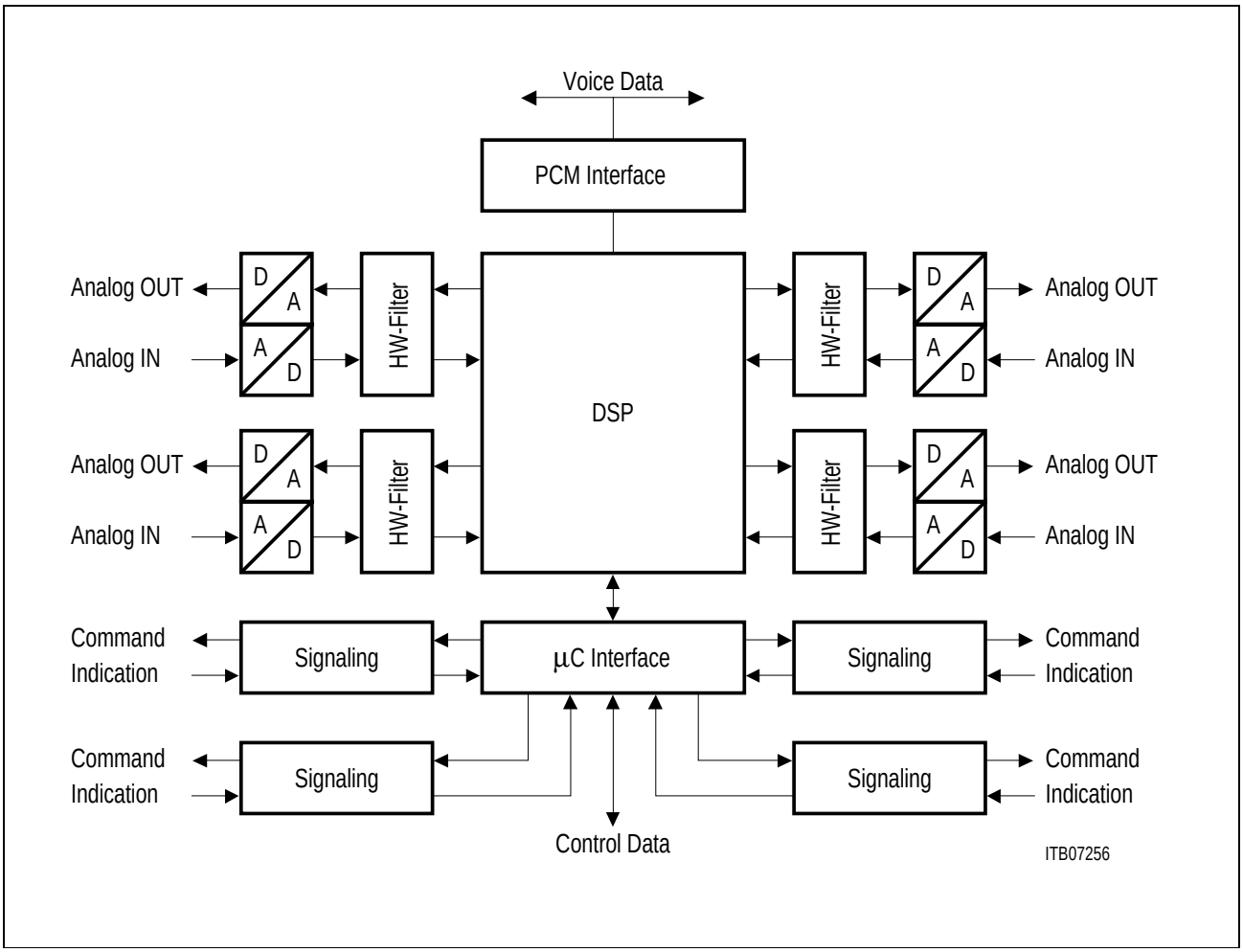


Figure 3
SICOFI®-4-µC Block Diagram

The SICOFI-4-µC bridges the gap between analog and digital voice signal transmission in modern telecommunication systems. High performance oversampling Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC) provide the conversion accuracy required. Analog antialiasing prefilters (PREFI) and smoothing postfilters (POFI) are included. The connection between the ADC and the DAC (with high sampling rate) and the DSP, is done by specific Hardware Filters, for filtering like interpolation and decimation. The dedicated Digital Signal Processor (DSP) handles all the algorithms necessary e.g. for PCM bandpass filtering, sample rate conversion and PCM companding. The PCM-interface handles digital voice transmission, a serial µC-interface handles SICOFI-4-µC feature control and transparent access to the SICOFI-4-µC command and indication pins. To program the filters, precalculated sets of coefficients are downloaded from the system to the on-chip Coefficient-RAM (CRAM).

2.2 The PCM-interface

Two serial PCM-interfaces are used for the transfer of A- or µ-law compressed voice data. The PCM-interface consist of 8 pins:

PCLK: PCM-Clock, 128 kHz to 8192 kHz

FSC: Frame Synchronization Clock, 8 kHz

DRA: Receive Data input for PCM-highway A

DRB: Receive Data input for PCM-highway B

DXA: Transmit Data output for PCM-highway A

DXB: Transmit Data output for PCM-highway B

TCA: Transmit Control Output for PCM-highway A, active low during transmission

TCB: Transmit Control Output for PCM-highway B, active low during transmission

The Frame Sync FSC pulse identifies the beginning of a receive and transmit frame for all of the four channels. The PCLK clock is the signal to synchronize the data transfer on both lines DXA (DXB) and DRA (DRB). Bytes in all channels are serialized to 8 bit width and MSB first. As a default setting, the rising edge indicates the start of the bit, while the falling edge is used to latch the contents of the received data on DRA (DRB). If the double clock rate is chosen (twice the transmission rate) the first rising edge indicates the start of a bit, while the second falling edge is used for latching the contents of the data line DRA (DRB) by default.

The data rate of the interface can vary from 2×128 kbit/s to 2×8192 kbit/s (2 highways) A frame may consist of up to 128 time slots of 8 bits each. In the Time Slot Configuration Registers CR5 and CR6 the user can select an individual time slot, and an individual PCM-highway, for any of the four voice channels. Receive and transmit time slots can also be programmed individually. An extra delay of up to 7 clocks, valid for all channels, as well as the sampling slope may be programmed (see XR6).

When the SICOFI-4-µC is transmitting data on DXA (DXB), pin TCA (TCB) is activated to control an extra external driving device.

The following table shows possible examples for the PCM-interface, other frequencies like 768 kHz or 1536 kHz are also possible.

Table 1

	Frequency [kHz]	**Single/Double** [1/2]	**Time Slots** [per highway]	**Datarate** [kbit/s per highway]
	128	1	2	128
	256	2	2	128
	256	1	4	256
	512	2	4	256
	512	1	8	512
	1024	2	8	512
	1024	1	16	1024
	2048	2	16	1024
	2048	1	32	2048
	4096	2	32	2048
	4096	1	64	4096
	8192	2	64	4096
	8192	1	128	8192
Formula	**f**	**1**	**f/64**	**f**
Formula	**f**	**2**	**f/128**	**f/2**

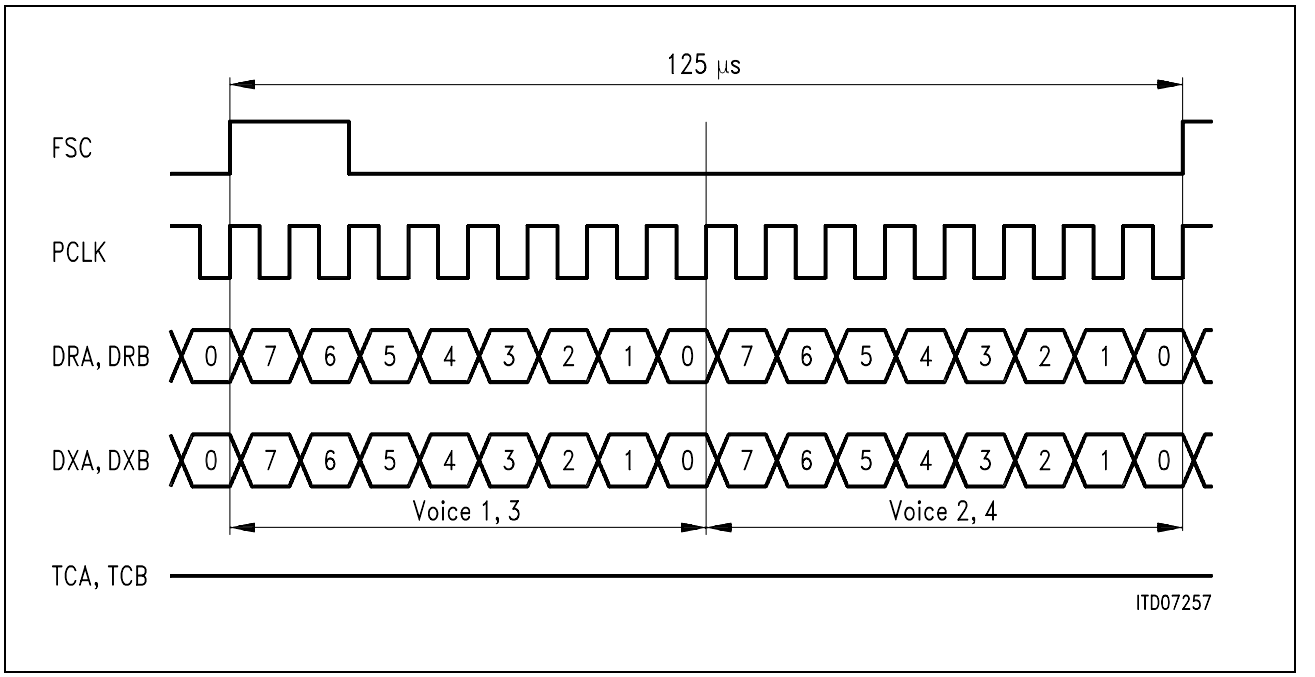


Figure 4
Example for Single Clock Rate, 128 kbit/s

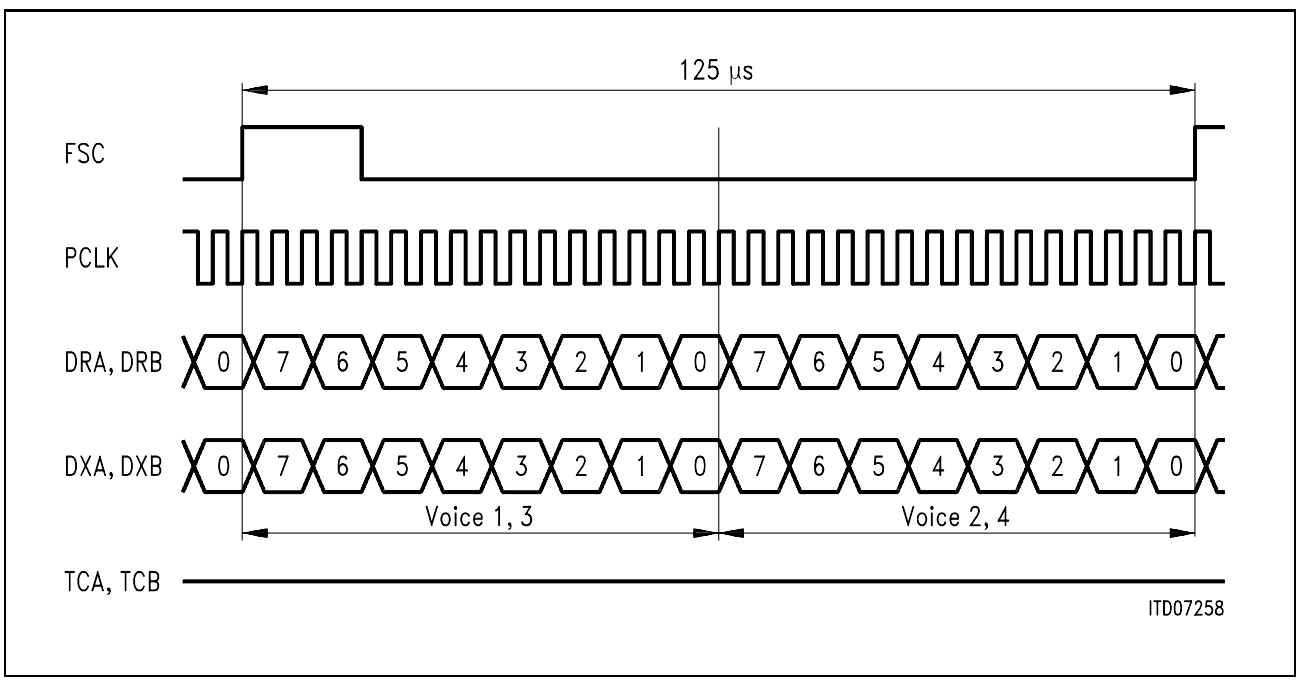


Figure 5
Example for Double Clock Rate, 128 kbit/s

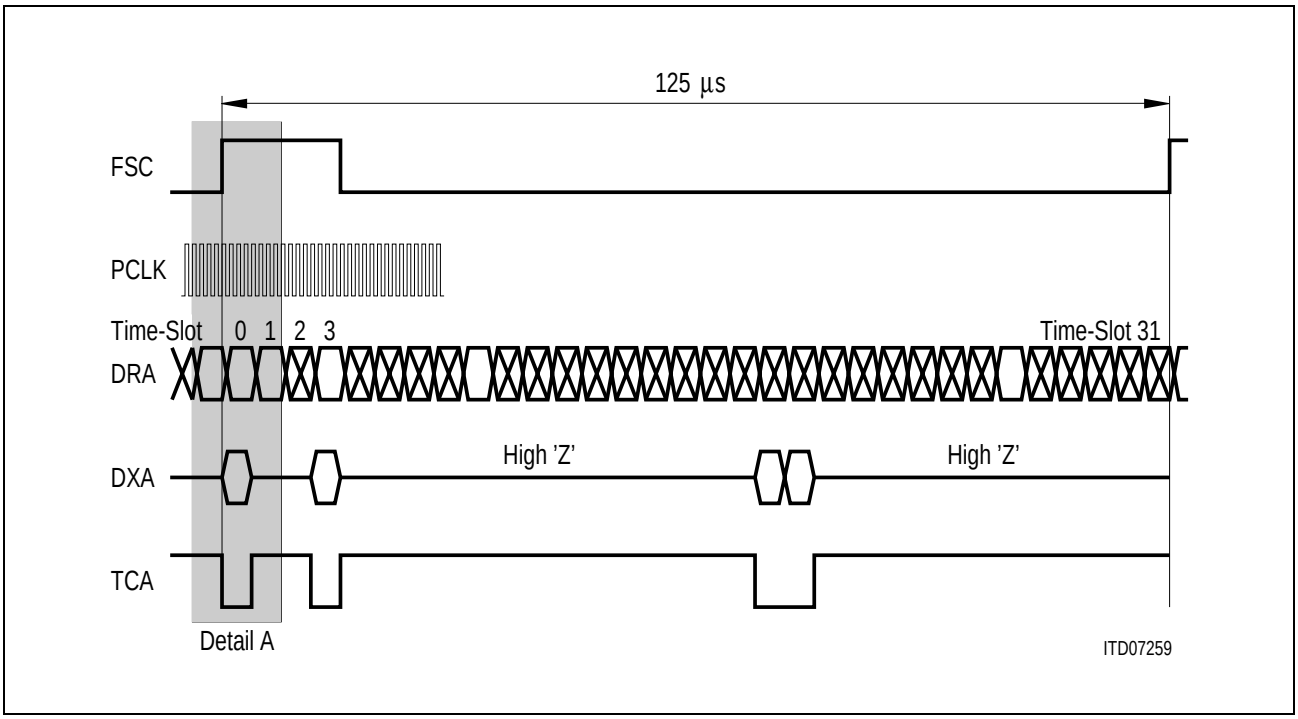


Figure 6
Example for 2048 kbit/s, Single Clock Operation, only Highway A used

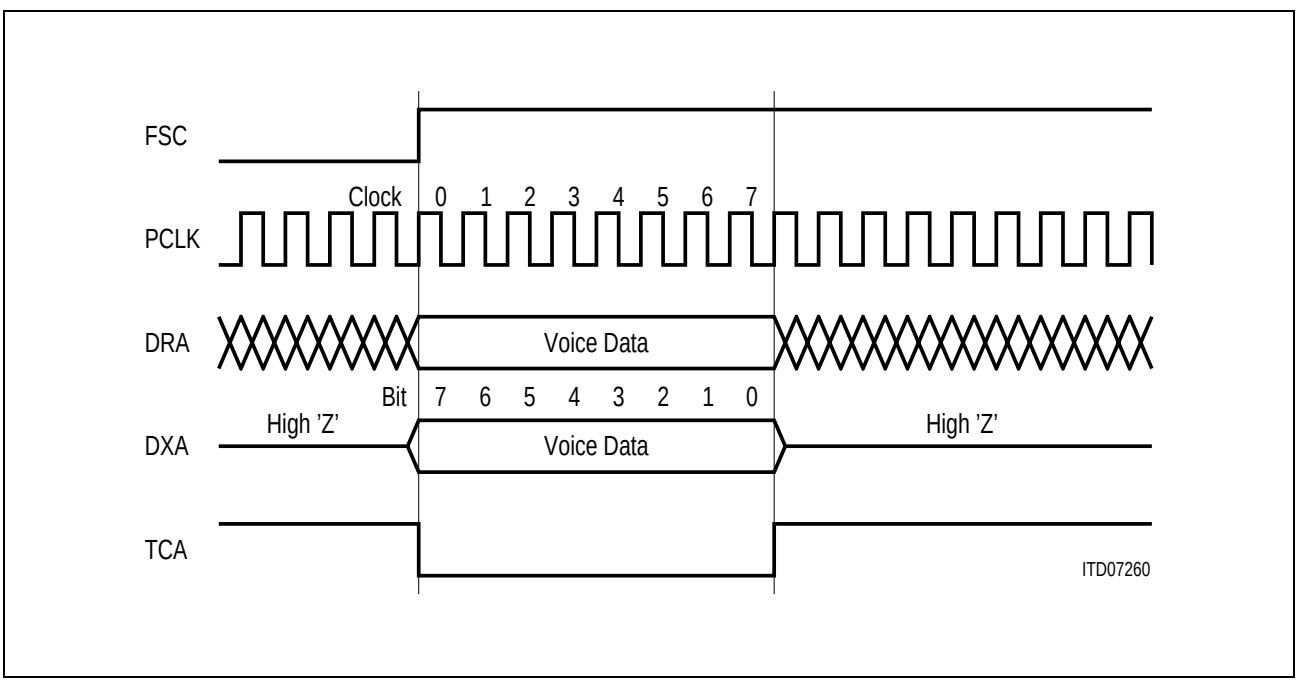


Figure 7
Detail A

For special purposes the DRA/B and DXA/B pins may be strapped together, and form bi-directional data-'pin' (like SIP with the SLD-bus).

2.3 The µ-Controller Interface

The internal configuration registers, the signaling interface, and the Coefficient-RAM (CRAM) of the SICOFI-4-µC are programmable via a serial µ-Controller interface.

The µ-Controller interface consists of four lines: CS, DCLK, DIN and DOUT:

CS is used to start a serial access to the SICOFI-4-µC registers and Coefficient-RAM. Following a falling edge of CS, the first eight bits received on DIN specify the command. Subsequent data bytes (number depends on command) are stored in the selected configuration registers or the selected part of the Coefficient-RAM.

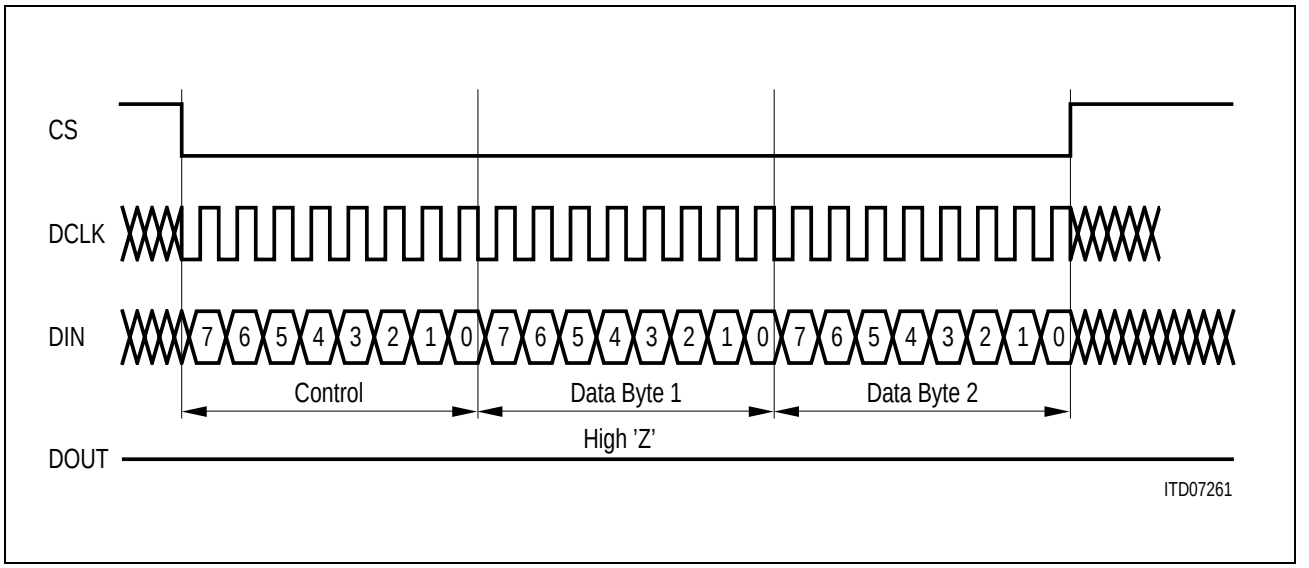


Figure 8
Example for a Write Access, with Two Data Bytes Transferred

If the first eight bits received via DIN specify a read-command, the SICOFI-4 will start a response via DOUT with its specific address byte (81_H). After transmitting this identification, the specified n data bytes (contents of configuration registers, or contents of the CRAM) will follow on DOUT.

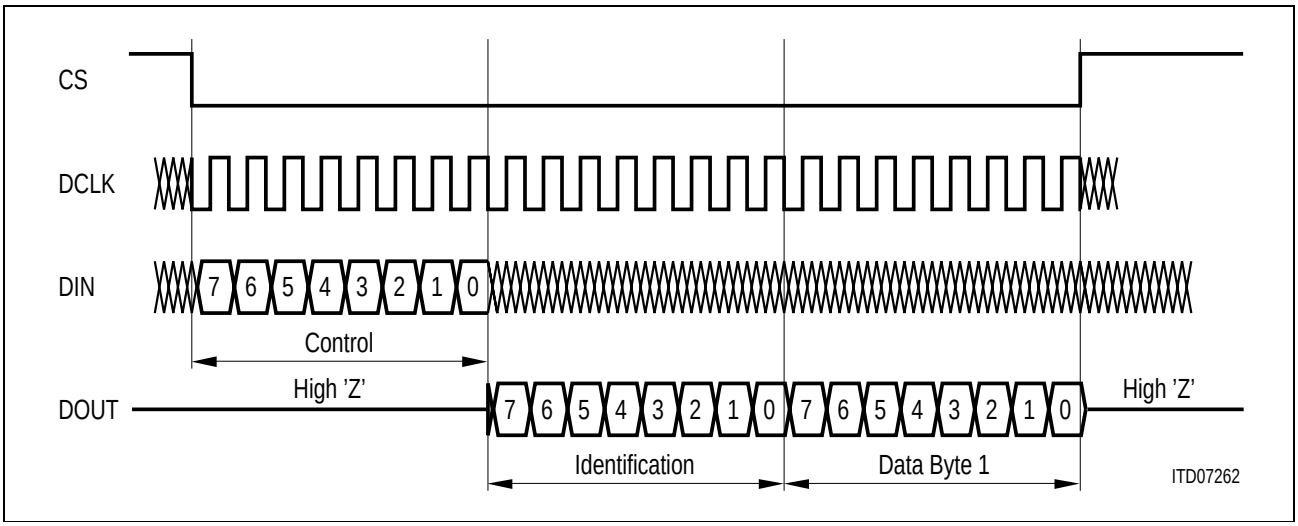


Figure 9
Example for a Read Access, with One Data Byte Transferred via DOUT

The data transfer is synchronized by the DCLK input. The contents of DIN is latched at the rising edge of DCLK, while DOUT changes with the falling edge of DCLK. During execution of commands that are followed by output data (read commands), the device will not accept any new command via DIN. The data transfer sequence can be broken by setting CS to high.

To reduce the number of connections to the µP DIN and DOUT may be strapped together, and form a bi-directional data-'pin'.

For special applications a byte by byte transfer is needed. This can be done by prolonging the high time of DCLK for a user defined 'waiting time' after transferring any byte.

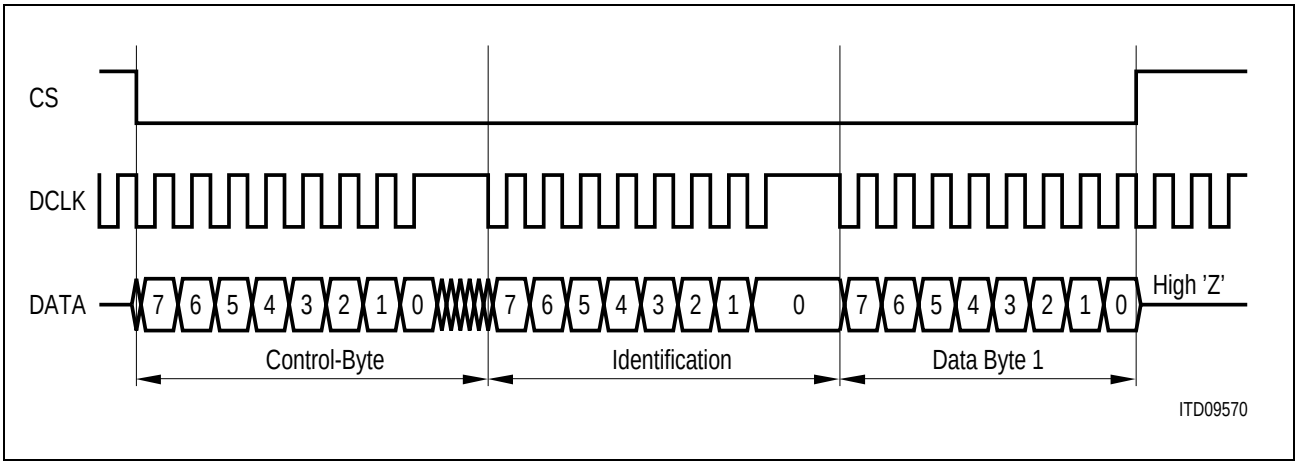


Figure 10
Example for a Write/Read Access, with a Byte by Byte Transfer, and DIN and DOUT Strapped Together

The Identification Byte is "81_H" for the PEB 2466.

3 Programming the SICOFI®-4-µC

With the appropriate commands, the SICOFI-4-µC can be programmed and verified very flexibly via the µ-Controller interface.

With the first byte received via DIN, one of 3 different types of commands (SOP, XOP and COP) is selected. Each of those can be used as a write or read command. Due to the extended SICOFI-4-µC feature control facilities, SOP, COP and XOP commands contain additional information (e.g. number of subsequent bytes) for programming (write) and verifying (read) the SICOFI-4-µC status.

A write command is followed by up to 8 bytes of data. The SICOFI-4-µC responds to a read command with its specific identification and the requested information, that is up to 8 bytes of data.

3.1 Types of Command and Data Bytes

The 8-bit bytes have to be interpreted as either commands or status information stored in Configuration Registers or the Coefficient-RAM. There are three different types of SICOFI -4-µC commands which are selected by bit 3 and 4 as shown below.

SOP **STATUS OPERATION:** SICOFI-4-µC status setting/monitoring

Bit	7							0
	AD2	AD1		1	0			

XOP **EXTENDED OPERATION:** C/I[1)] channel configuration/evaluation

Bit	7							0
		0		1	1			

COP **COEFFICIENT OPERATION:** filter coefficient setting/monitoring

Bit	7							0
	AD2	AD1		0				

Note: [1)] Command/Indication (signaling) channel.

Storage of Programming Information

6 configuration registers per channel:	CR0, CR1, CR2, CR3, CR4 and CR5 accessed by SOP commands
8 common configuration registers:	XR0 .. XR7 accessed by XOP commands, valid for all 4 channels
1 Coefficient-RAM per channel:	CRAM accessed by COP commands

3.2 Examples for SICOFI®-4 Commands

SOP - Write Commands

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
SOP-Write 1 Byte			0	1	0	0	0	0		Idle								
CR0	Data									Idle								

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
SOP-Write 2 Bytes			0	1	0	0	0	1		Idle								
CR1	Data									Idle								
CR0	Data									Idle								

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
SOP-Write 3 Bytes			0	1	0	0	1	0		Idle								
CR2	Data									Idle								
CR1	Data									Idle								
CR0	Data									Idle								

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
SOP-Write 4 Bytes			0	1	0	0	1	1		Idle								
CR3	Data									Idle								
CR2	Data									Idle								
CR1	Data									Idle								
CR0	Data									Idle								

XOP - Write Commands

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
XOP-Write 2 Bytes			0	1	1	0	0	1		Idle								
XR1	Data									Idle								
XR0	Data									Idle								

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
XOP-Write 3 Bytes			0	1	1	0	1	0		Idle								
XR2	Data									Idle								
XR1	Data									Idle								
XR0	Data									Idle								

COP - Write Commands

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
COP-Write 4 Bytes			0	0						Idle								
Coeff. 3	Data									Idle								
Coeff. 2	Data									Idle								
Coeff. 1	Data									Idle								
Coeff. 0	Data									Idle								

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
COP-Write 8 Bytes			0	0						Idle								
Coeff. 7	Data									Idle								
Coeff. 6	Data									Idle								
Coeff. 5	Data									Idle								
Coeff. 4	Data									Idle								
Coeff. 3	Data									Idle								
Coeff. 2	Data									Idle								
Coeff. 1	Data									Idle								
Coeff. 0	Data									Idle								

SOP - Read Commands

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
SOP-Read 1 Byte			1	1	0	0	0	0		Idle								
	Idle									1	0	0	0	0	0	0	1	Identification
	Idle									Data								CR0

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
SOP-Read 2 Bytes			1	1	0	0	0	1		Idle								
	Idle									1	0	0	0	0	0	0	1	Identification
	Idle									Data								CR1
	Idle									Data								CR0

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
SOP-Read 3 Bytes			1	1	0	0	1	0		Idle								
	Idle									1	0	0	0	0	0	0	1	Identification
	Idle									Data								CR2
	Idle									Data								CR1
	Idle									Data								CR0

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
SOP-Read 4 Bytes			1	1	0	0	1	1		Idle								
	Idle									1	0	0	0	0	0	0	1	Identification
	Idle									Data								CR3
	Idle									Data								CR2
	Idle									Data								CR1
	Idle									Data								CR0

XOP-Read Commands

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
XOP-Read 1 Byte			1	1	1	0	0	0		Idle								
	Idle									1	0	0	0	0	0	0	1	Identification
	Idle									Data								XR0

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
XOP-Read 2 Bytes			1	1	1	0	0	1		Idle								
	Idle									1	0	0	0	0	0	0	1	Identification
	Idle									Data								XR1
	Idle									Data								XR0

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
XOP-Read 3 Bytes			1	1	1	0	1	0		Idle								
	Idle									1	0	0	0	0	0	0	1	Identification
	Idle									Data								XR2
	Idle									Data								XR1
	Idle									Data								XR0

COP-Read Commands

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
COP-Read 4 Bytes			1	0	1					Idle								
	Idle									1	0	0	0	0	0	0	1	Identification
	Idle									Data								Coeff. 3
	Idle									Data								Coeff. 2
	Idle									Data								Coeff. 1
	Idle									Data								Coeff. 0

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
COP-Read 8 Bytes			1	0	0					Idle								
	Idle									1	0	0	0	0	0	0	1	Identification
	Idle									Data								Coeff. 8
	Idle									Data								Coeff. 7
	Idle									Data								Coeff. 6
	Idle									Data								Coeff. 5
	Idle									Data								Coeff. 4
	Idle									Data								Coeff. 3
	Idle									Data								Coeff. 2
	Idle									Data								Coeff. 1

Example of a Mixed Command

DIN	7	6	5	4	3	2	1	0	Bit	7	6	5	4	3	2	1	0	DOUT
SOP-Write 4 Bytes			0	1	0	0	1	1		Idle								
CR3	Data									Idle								
CR2	Data									Idle								
CR1	Data									Idle								
CR0	Data									Idle								
XOP-Write 2 Bytes			0	1	1	0	0	1		Idle								
XR1	Data									Idle								
XR0	Data									Idle								
COP-Write 4 Bytes			0	0	1					Idle								
Coeff. 3	Data									Idle								
Coeff. 2	Data									Idle								
Coeff. 1	Data									Idle								
Coeff. 0	Data									Idle								
SOP-Read 3 Bytes			1	1	0	0	1	0		Idle								
	Idle									1	0	0	0	0	0	0	1	Identification
	Idle									Data								CR2
	Idle									Data								CR1
	Idle									Data								CR0
COP-Read 4 Bytes			1	0	1					Idle								
	Idle									1	0	0	0	0	0	0	1	Identification
	Idle									Data								Coeff. 3
	Idle									Data								Coeff. 2
	Idle									Data								Coeff. 1
	Idle									Data								Coeff. 0
XOP-Read 1 Byte			1	1	1	0	0	0		Idle								
	Idle									1	0	0	0	0	0	0	1	Identification
	Idle									Data								XR0

3.3 SOP Command

To modify or evaluate the SICOFI-4-µC status, the contents of up to 6 configuration registers CR0 .. CR7 may be transferred to or from the SICOFI-4-µC. This is started by a SOP-Command (status operation command).

Bit 7 0

AD2	AD1	RW	1	0	LSEL2	LSEL1	LSEL0

AD Address Information

AD = 00 SICOFI-4-µC - channel 1 is addressed with this command

AD = 01 SICOFI-4-µC - channel 2 is addressed with this command

AD = 10 SICOFI-4-µC - channel 3 is addressed with this command

AD = 11 SICOFI-4-µC - channel 4 is addressed with this command

RW Read/Write Information: Enables reading from the SICOFI-4-µC or writing information to the SICOFI-4-µC

RW = 0 Write to SICOFI-4 µC

RW = 1 Read from SICOFI-4 µC

LSEL Length select information (see also programming procedure)
This field identifies the number of subsequent data bytes

LSEL = 000 1 byte of data is following (CR0)

LSEL = 001 2 bytes of data are following (CR1, CR2)

LSEL = 010 3 bytes of data are following (CR2, CR1, CR0)

LSEL = 011 4 bytes of data are following (CR3, CR2, CR1, CR0)

LSEL = 100 5 bytes of data are following (CR4, CR3, CR2, CR1, CR0)

LSEL = 101 6 bytes of data are following (CR5, CR4, CR3, CR2, CR1, CR0)

All other codes are reserved for future use !

Note: If only one configuration register requires modification, for example CR5, this can be accomplished by setting LSEL = 101 and releasing pin CS after CR5 is written.

3.3.1 CR0 Configuration Register 0

Configuration register CR0 defines the basic SICOFI-4-µC settings, which are: enabling/ disabling the programmable digital filters.

Bit	7						0
	TH	IM/R1	FRX	FRR	AX	AR	TH-SEL

TH Enable TH- (Trans Hybrid Balancing) Filter

TH = 0: TH-filter disabled

TH = 1: TH-filter enabled

IM/R1 Enable IM-(Impedance Matching) Filter and R1-Filter

IM/R1 = 0: IM-filter and R1-filter disabled

IM/R1 = 1: IM-filter and R1-filter enabled

FRX Enable FRX (Frequency Response Transmit)-Filter

FRX = 0: FRX-filter disabled

FRX = 1: FRX-filter enabled

FRR Enable FRR (Frequency Response Receive)-Filter

FRR = 0: FRR-filter disabled

FRR = 1: FRR-filter enabled

AX Enable AX-(Amplification/Attenuation Transmit) Filter

AX = 0: AX-filter disabled

AX = 1: AX-filter enabled

AR Enable AR-(Amplification/Attenuation Receive) Filter

AR = 0: AX-filter disabled

AR = 1: AX-filter enabled

TH-SEL 2 bit field to select one of four programmed TH-filter coefficient sets

TH-Sel = 0 0: TH-filter coefficient set 1 is selected

TH-Sel = 0 1: TH-filter coefficient set 2 is selected

TH-Sel = 1 0: TH-filter coefficient set 3 is selected

TH-Sel = 1 1: TH-filter coefficient set 4 is selected

3.3.2 CR1 Configuration Register 1

Configuration register CR1 selects tone generator modes and other operation modes.

Bit	7							0
	ETG2	ETG1	PTG2	PTG1	LAW	0	0	PU

ETG2 Enable programmable tone generator 2 [1)]

ETG2 = 0: Programmable tone generator 2 is disabled

ETG2 = 1: Programmable tone generator 2 is enabled

ETG1 Enable programmable tone generator 1

ETG1 = 0: Programmable tone generator 1 is disabled

ETG1 = 1: Programmable tone generator 1 is enabled

PTG2 User programmed frequency or fixed frequency is selected

PTG2 = 0: Fixed frequency for tone generator 2 is selected (1 kHz)

PTG2 = 1: Programmed frequency for tone generator 2 is selected

PTG1 User programmed frequency or fixed frequency is selected

PTG1 = 0: Fixed frequency for tone generator 1 is selected (1 kHz)

PTG1 = 1: Programmed frequency for tone generator 1 is selected

LAW PCM - law selection

LAW = 0: A-Law is selected

LAW = 1: µ-Law (µ255 PCM) is selected

PU Power UP, sets the addressed channel to Power Up / Down

PU = 0: The addressed channel is set to Power Down (standby)

PU = 1: The addressed channel is set to Power Up (operating)

[1)] Tone generator 2 is not available if Level Metering Function is enabled!

3.3.3 CR2 Configuration Register 2

Bit 7 0

COT/R	0	IDR	LM	LMR	V+T

COT/R Selection of Cut off Transmit/Receive Paths

0 0 0:	Normal Operation	
0 0 1:	COT16	Cut Off Transmit Path at 16 kHz (input of TH-Filter)
0 1 0:	COT8	Cut Off Transmit Path at 8 kHz (input of compression, output is zero for µ-law, 1 LSB for A-law)
1 0 1:	COR4M	Cut Off Receive Path at 4 MHz (POFI-output)
1 1 0:	COR64	Cut Off Receive Path at 64 kHz (IM-filter input)

IDR Initialize Data RAM

IDR = 0: Normal operation is selected

IDR = 1: Contents of Data RAM is set to 0 (used for production test purposes)

LM Level Metering function [1)]

LM = 0: Level metering function is disabled

LM = 1: Level metering function is enabled

LMR Result of Level Metering function (this bit can not be written)

LMR = 0: Level detected was lower than the reference

LMR = 1: Level detected was higher than the reference

V+T Add Voice signal and Tone Generator signal

V+T = 0: Voice or Tone Generator is fed to the DAC

V+T = 1: Voice and Tone Generator Signals are added, and fed to the Digital to Analog Converter

1) Explanation of the level metering function:
A signal fed to A/µ-Law compression via AX- and HPX-filters (from a digital loop, or externally via VIN), is rectified, and the power is measured. If the power exceeds a certain value, loaded to XR7, bit LMR is set to '1'. The power of the incoming signal can be adjusted by AX-filters.

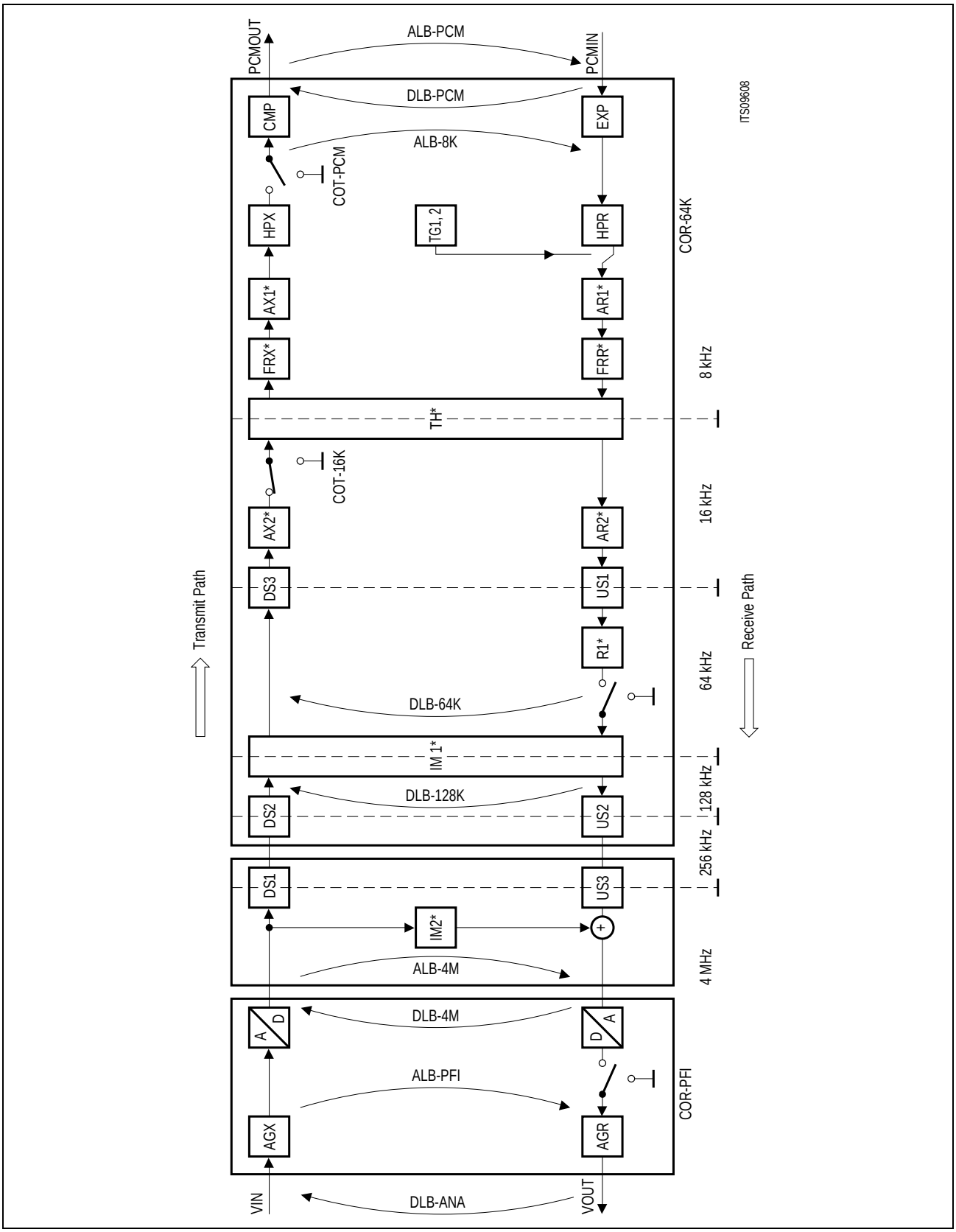


Figure 11
'CUT OFF's' and Loops

3.3.4 CR3 Configuration Register 3

Bit 7 0

Test-Loops	AGX	AGR	D-HPX	D-HPR

Test-Loops 4 bit field for selection of Analog and Digital Loop Backs

0 0 0 0:		No loop back is selected (normal operation)
0 0 0 1:	ALB-PFI	Analog loop back via PREFI-POFI is selected
0 0 1 1:	ALB-4M	Analog loop back via 4 MHz is selected
0 1 0 0:	ALB-PCM	Analog loop back via 8 kHz (PCM) is selected (attention: special settings necessary)
0 1 0 1:	ALB-8K	Analog loop back via 8 kHz (linear) is selected
1 0 0 0:	DLB-ANA	Digital loop back via analog port is selected
1 0 0 1:	DLB-4M	Digital loop back via 4 MHz is selected
1 1 0 0:	DLB-128K	Digital loop back via 128 kHz is selected
1 1 0 1:	DLB-64K	Digital loop back via 64 kHz is selected
1 1 1 1:	DLB-PCM	Digital loop back via PCM-registers is selected

AGX Analog gain in transmit direction

AGX = 0: Analog gain is disabled

AGX = 1: Analog gain is enabled (6.02 dB amplification)

AGR Analog gain in receive direction

AGR = 0: Analog gain is disabled

AGR = 1: Analog gain is enabled (6.02 dB attenuation)

D-HPX Disable highpass in transmit direction

D-HPX = 0: Transmit high pass is enabled

D-HPX = 1: Transmit high pass is disabled[1)]

D-HPR Disable highpass in receive direction

D-HPR = 0: Receive high pass is enabled

D-HPR = 1: Receive high pass is disabled[2)]

1) In this case the transmit-path signal is attenuated 0.06 dB

2) In this case the receive-path signal is attenuated 0.12 dB

3.3.5 CR4 Configuration Register 4

Configuration register CR4, sets the receiving time slot and the receiving PCM-highway.

Bit 7							0
R-WAY	**RS6**	**RS5**	**RS4**	**RS3**	**RS2**	**RS1**	**RS0**

R-WAY Selects the PCM-Highway for the receiving of PCM-data

R-WAY = 0: PCM-Highway A is selected

R-WAY = 1: PCM-Highway B is selected

RS[6:0] Selects the time slot (0 to 127) used for receiving the PCM-data

The time slot-number is binary coded.

0 0 0 0 0 0 0: Time slot 0 is selected

0 0 0 0 0 0 1: Time slot 1 is selected

....

1 1 1 1 1 1 0: Time slot 126 is selected

1 1 1 1 1 1 1: Time slot 127 is selected

3.3.6 CR5 Configuration Register 5

Configuration register CR5, sets the transmit time slot and the transmit PCM-highway.

Bit 7							0
X-WAY	**XS6**	**XS5**	**XS4**	**XS3**	**XS2**	**XS1**	**XS0**

X-WAY Selects the PCM-Highway for transmitting PCM-data

X-WAY = 0: PCM-Highway A is selected

X-WAY = 1: PCM-Highway B is selected

XS[6:0] Selects the time slot (0 to 127) used for transmitting the PCM-data

The time slot-number is binary coded.

0 0 0 0 0 0 0: Time slot 0 is selected

0 0 0 0 0 0 1: Time slot 1 is selected

....

1 1 1 1 1 1 0: Time slot 126 is selected

1 1 1 1 1 1 1: Time slot 127 is selected

3.4 COP Command

With a COP command coefficients for the programmable filters can be written to the SICOFI-4-µC coefficient-RAM or read from the Coefficient-RAM via the µ-Controller interface for verification

Bit 7 … 0

AD2	AD1	RW	0	CODE3	CODE2	CODE1	CODE0

AD Address

AD = 0 0 SICOFI-4-µC- channel 1 is addressed

AD = 0 1 SICOFI-4-µC- channel 2 is addressed

AD = 1 0 SICOFI-4-µC- channel 3 is addressed

AD = 1 1 SICOFI-4-µC- channel 4 is addressed

RW Read/Write

RW = 0 Subsequent data is written to the SICOFI-4-µC

RW = 1 Read data from SICOFI-4-µC

CODE Includes number of following bytes and filter-address

0	0	0	0	TH-Filter coefficients (part 1)	(followed by 8 bytes of data)
0	0	0	1	TH-Filter coefficients (part 2)	(followed by 8 bytes of data)
0	0	1	0	TH-Filter coefficients (part 3)	(followed by 8 bytes of data)
0	1	0	0	IM/R1-Filter coefficients (part 1)	(followed by 8 bytes of data)
0	1	0	1	IM/R1-Filter coefficients (part 2)	(followed by 8 bytes of data)
0	1	1	0	FRX-Filter coefficients	(followed by 8 bytes of data)
0	1	1	1	FRR-Filter coefficients	(followed by 8 bytes of data)
1	0	0	0	AX-Filter coefficients	(followed by 4 bytes of data)
1	0	0	1	AR-Filter coefficients	(followed by 4 bytes of data)
1	1	0	0	TG 1- coefficients	(followed by 4 bytes of data)
1	1	0	1	TG 2- coefficients	(followed by 4 bytes of data)

How to Program the Filter Coefficients

TH-Filter: Four sets of TH-filter coefficients can be loaded to the SICOFI-4-µC. Each of the four sets can be selected for any of the four SICOFI-4-µC channels, by setting the value of TH-Sel in configuration register CR2. Coefficient set 1 is loaded to the SICOFI-4-µC via channel 1, set 2 is loaded via channel 2 and so on.

AX, AR, IM/R1, FRX, FRR-Filter, Tone-Generators:

An individual coefficient set is available for each of the four channels.

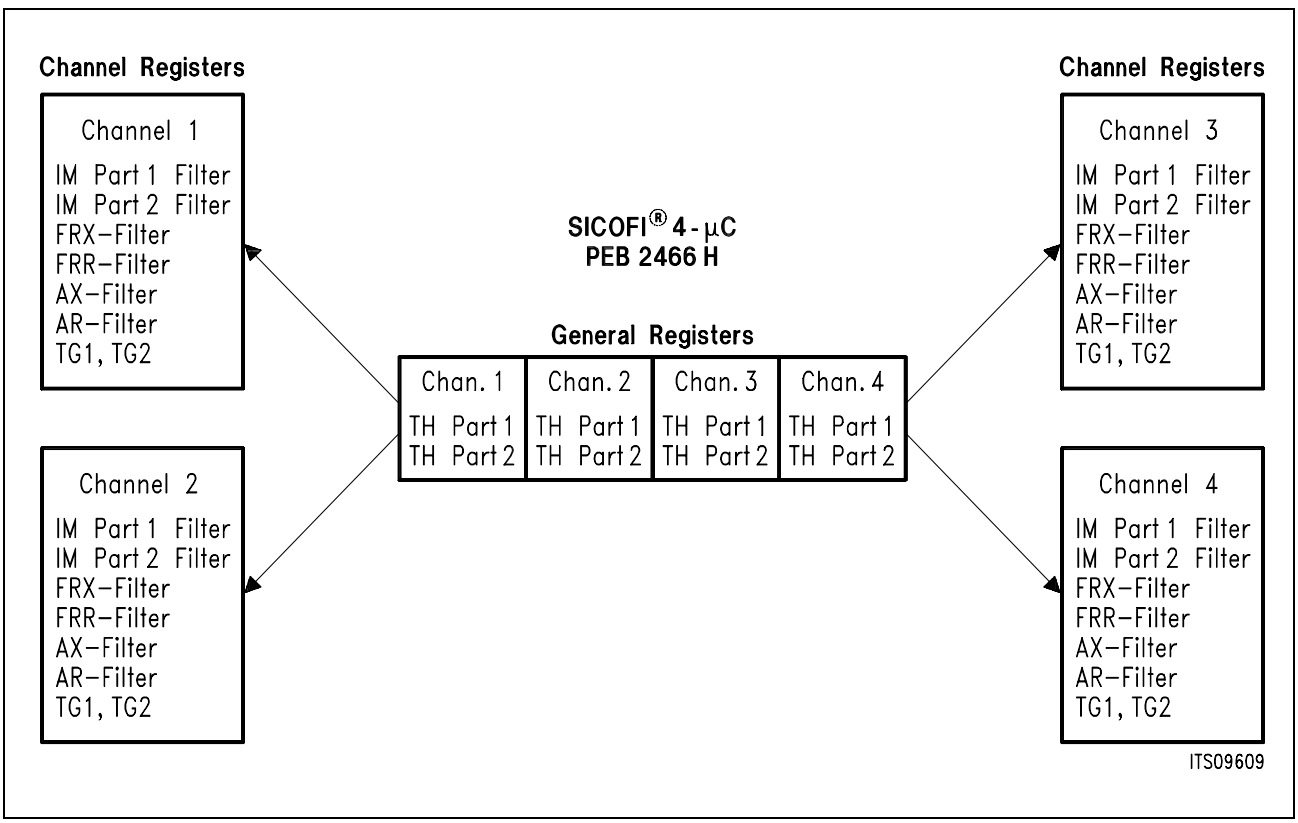


Figure 12

3.5 XOP Command

With the XOP command the SICOFI-4-µC digital command/indication interface to a SLIC is configured and evaluated. Also other common functions are assigned with this command.

Bit 7 … 0

RST	0	RW	1	1	LSEL2	LSEL1	LSEL0

RST Software Reset

(same as RESET-pin, valid for all 4 channels)

RST = 1: Reset

RST = 0: No operation

RW Read / Write Information: Enables reading from the SICOFI-4-µC or writing information to the SICOFI-4-µC

RW = 0: Write to SICOFI-4-µC

RW = 1: Read from SICOFI-4-µC

LSEL Length select information, for setting the number of subsequent data bytes

LSEL = 000: 1 byte of data is following (XR0)

LSEL = 001: 2 bytes of data are following (XR1, XR0)

:

LSEL = 111: 8 bytes of data are following (XR7, XR6, XR5, XR4, XR3, XR2, XR1, XR0)

Note: All other codes are reserved for future use!
If only one configuration register requires modification, for example XR5, this can be accomplished by setting LSEL =101 and releasing pin CS after XR5 is written.

3.5.1 XR0 Extended Register 0

The signaling connection between SICOFI-4-µC and a SLIC is performed by master device the SICOFI-4-µC signaling input and output pins and Configuration Register XR0... XR4. Data received from the upstream master device are transferred to signaling output pins (SO, SB). Data at the signaling input pins are transferred to the upstream controller.

In Connection with XOP-Read Commands

Bit 7							0
SI4_1	**SI4_0**	**SI3_1**	**SI3_0**	**SI2_1**	**SI2_0**	**SI1_1**	**SI1_0**

SI4_1 Status of pin SI4_1 is transferred to the upstream master device

SI4_0 Status of pin SI4_0 is transferred to the upstream master device

SI3_1 Status of pin SI3_1 is transferred to the upstream master device

SI3_0 Status of pin SI3_0 is transferred to the upstream master device

SI2_1 Status of pin SI2_1 is transferred to the upstream master device

SI2_0 Status of pin SI2_0 is transferred to the upstream master device

SI1_1 Status of pin SI1_1 is transferred to the upstream master device

SI1_0 Status of pin SI1_0 is transferred to the upstream master device

In Connection with XOP-Write Commands

Bit 7							0
SO4_1	**SO4_0**	**SO3_1**	**SO3_0**	**SO2_1**	**SO2_0**	**SO1_1**	**SO1_0**

SO4_1 Pin SO4_1 is set to the assigned value

SO4_0 Pin SO4_0 is set to the assigned value

SO3_1 Pin SO3_1 is set to the assigned value

SO3_0 Pin SO3_0 is set to the assigned value

SO2_1 Pin SO2_1 is set to the assigned value

SO2_0 Pin SO2_0 is set to the assigned value

SO1_1 Pin SO1_1 is set to the assigned value

SO1_0 Pin SO1_0 is set to the assigned value

3.5.2 XR1 Extended Register 1

This register transfers information to or from the programmable signaling pins.

Bit 7							0
SB4_1	**SB4_0**	**SB3_1**	**SB3_0**	**SB2_1**	**SB2_0**	**SB1_1**	**SB1_0**

In Connection with a XOP-Read Command

SB4_1 If input: status of pin SB4_1 is transferred upstream
SB4_0 If input: status of pin SB4_0 is transferred upstream
SB3_1 If input: status of pin SB3_1 is transferred upstream
SB3_0 If input: status of pin SB3_0 is transferred upstream
SB2_1 If input: status of pin SB2_1 is transferred upstream
SB2_0 If input: status of pin SB2_0 is transferred upstream
SB1_1 If input: status of pin SB1_1 is transferred upstream
SB1_0 If input: status of pin SB1_0 is transferred upstream

In Connection with a XOP-Write Command

SB4_1 If output: pin SB4_1 is set to the assigned value
SB4_0 If output: pin SB4_0 is set to the assigned value
SB3_1 If output: pin SB3_1 is set to the assigned value
SB3_0 If output: pin SB3_0 is set to the assigned value
SB2_1 If output: pin SB2_1 is set to the assigned value
SB2_0 If output: pin SB2_0 is set to the assigned value
SB1_1 If output: pin SB1_1 is set to the assigned value
SB1_0 If output: pin SB1_0 is set to the assigned value

Note: After a 'Reset' of the device, all programmable pins are input pins!

3.5.3 XR2 Extended Register 2

This register controls the direction of the programmable signaling pins.

Bit 7 0

PSB4_1	PSB4_0	PSB3_1	PSB3_0	PSB2_1	PSB2_0	PSB1_1	PSB1_0

PSB4_1 Programmable bi-directional signaling pin SB4_1 is programmed
PSB4_1 = 0: Pin SB4_1 is indication input
PSB4_1 = 1: Pin SB4_1 is command output

PSB4_0 Programmable bi-directional signaling pin SB4_0 is programmed
PSB4_0 = 0: pin SB4_0 is indication input
PSB4_0 = 1: Pin SB4_0 is command output

PSB3_1 Programmable bi-directional signaling pin SB3_1 is programmed
PSB3_1 = 0: Pin SB3_1 is indication input
PSB3_1 = 1: Pin SB3_1 is command output

PSB3_0 Programmable bi-directional signaling pin SB3_0 is programmed
PSB3_0 = 0: Pin SB3_0 is indication input
PSB3_0 = 1: Pin SB3_0 is command output

PSB2_1 Programmable bi-directional signaling pin SB2_1 is programmed
PSB2_1 = 0: Pin SB2_1 is indication input
PSB2_1 = 1: Pin SB2_1 is command output

PSB2_0 Programmable bi-directional signaling pin SB2_0 is programmed
PSB2_0 = 0: Pin SB2_0 is indication input
PSB2_0 = 1: Pin SB2_0 is command output

PSB1_1 Programmable bi-directional signaling pin SB1_1 is programmed
PSB1_1 = 0: Pin SB1_1 is indication input
PSB1_1 = 1: Pin SB1_1 is command output

PSB1_0 Programmable bi-directional signaling pin SB1_0 is programmed
PSB1_0 = 0: Pin SB1_0 is indication input
PSB1_0 = 1: Pin SB1_0 is command output

Note: After a 'Reset' of the device, all programmable pins are input pins!

3.5.4 XR3 Extended Register 3

This register transfers information to or from the programmable signaling pins and configures these pins.

Bit 7 0

SB4_2	SB3_2	SB2_2	SB1_2	PSB4_2	PSB3_2	PSB2_2	PSB1_2

In Connection with a XOP-Read Command

SB4_2 If input: status of pin SB4_2 is transferred upstream

SB3_2 If input: status of pin SB3_2 is transferred upstream

SB2_2 If input: status of pin SB2_2 is transferred upstream

SB1_2 If input: status of pin SB1_2 is transferred upstream

In Connection with a XOP-Write Command

SB4_2 If output: pin SB4_2 is set to the assigned value

SB3_2 If output: pin SB3_2 is set to the assigned value

SB2_2 If output: pin SB2_2 is set to the assigned value

SB1_2 If output: pin SB1_2 is set to the assigned value

PSB4_2 Programmable bi-directional signaling pin SB4_2 is programmed

PSB4_2 = 0: Pin SB4_2 is indication input

PSB4_2 = 1: Pin SB4_2 is command output

PSB3_2 Programmable bi-directional signaling pin SB3_2 is programmed

PSB3_2 = 0: Pin SB3_2 is indication input

PSB3_2 = 1: Pin SB3_2 is command output

PSB2_2 Programmable bi-directional signaling pin SB2_2 is programmed

PSB2_2 = 0: Pin SB2_2 is indication input

PSB2_2 = 1: Pin SB2_2 is command output

PSB1_2 Programmable bi-directional signaling pin SB1_2 is programmed

PSB1_2 = 0: Pin SB1_2 is indication input

PSB1_2 = 1: Pin SB1_2 is command output

Note: After a 'Reset' of the device, all programmable pins are input pins!

3.5.5 XR4 Extended Register 4

Register XR4 provides two optional functions: debouncing of signaling input changes, and the configuration of the programmable output pin CHCLK1.

Bit 7							0
N				**T**			

Signaling Debounce Interval N

To restrict the rate of changes on signaling input pins transferred, deglitching of the status information from the SLIC may be applied. New status information will be read into registers XR0, XR1, XR2 and XR3, and an interrupt on pin INT12 (INT34) will be generated, after it has been stable for N milliseconds. N is programmable in the range of 2 to 30 ms in steps of 2 ms, with N = 0 the debouncing is disabled.

Field N				**Debounce Interval Time**
0	0	0	0	Debounce and interrupt generation is disabled
0	0	0	1	Debounce period 2 ms
0	0	1	0	Debounce period 4 ms
.	.	.	.	.
.	.	.	.	.
1	1	1	0	Debounce period 28 ms
1	1	1	1	Debounce period 30 ms

Configuration of CHCLK1

Field T				**Frequency applied to Pin CHCLK1**
0	0	0	0	CHCLK1 is set to 1 permanently
0	0	0	1	T is 2ms
0	0	1	0	T is 4ms
.	.	.	.	.
.	.	.	.	.
1	1	1	0	T is 28 ms
1	1	1	1	CHCLK1 is set to 0 permanently

3.5.6 XR5 Extended Register 5

This register contains additional configuration items valid for all 4 channels

Bit 7				0
MCLK-SEL	**CRSH_A**	**CRSH_B**	**CHCLK2**	**Version**

MCLK-SEL Selects Master Clock frequency, that has to be applied to pin MCLK

The MCLK signal has to synchronous to the 8 kHz FSC-signal.

0 0: 1536 kHz selected

0 1: 2048 kHz selected

1 0: 4096 kHz selected

1 1: 8192 kHz selected

CRSH_A Crash[1] on PCM-highway A (line DXA)

0: No crash detected

1: Crash detected (bad programming in CR5-registers)

CRSH_B Crash on PCM-highway B (line DXB)

0: No crash detected

1: Crash detected (bad programming in CR5-registers)

CHCLK2 Enables Chopper Clock Output to pin CHCLK2

0 0: pin CHCLK2 is set to 1

0 1: A 512 kHz signal is fed to pin CHCLK2

1 0: A 256 kHz signal is fed to pin CHCLK2

1 1: A 16384 kHz signal (internal masterclock) is fed to pin CHCLK2

(at least one of the four channels has to be set to 'POWER UP')

VERSION This two bit field identifies the actual chip version,

is '00' for Version 1.1, and '01' for Version 1.2

[1] A crash occurs, if 2 or more channels are programed to transmit (talk) in the same time slot on the same highway. In this case the crash-bit will be set, and transmission will be disabled for all affected channels.

3.5.7 XR6 Extended Register 6

This register configures the operation of the PCM-interface

Bit 7 0

C-MODE	X-S	R-S	DRV_0	Shift	PCM-OFFSET

C-MODE Defines the CLK-Mode for the PCM-interface

C-Mode = 0: Single clocking is used

C-Mode = 1: Double clocking is used

X-S Transmit Slope

X-S = 0: Transmission starts with rising edge

X-S = 1: Transmission starts with falling edge

R-S Receive Slope

R-S= 0: Data is sampled with falling edge of PCLK

R-S= 1: Data is sampled with rising edge of PCLK

DRV_0 Driving Mode for Bit 0 (only available with single clocking mode)

DRV_0 = 0: Bit 0 is driven the whole PCLK-period

DRV_0 = 1: Bit 0 is driven during the first half of the PCLK-period only

Shift Shifts the access to DXA/B and DRA/B for one PCLK-period (only available with double clocking mode)

Shift = 0: No shift takes place

Shift = 1: Access to DXA/B and DRA/B is shifted for one PCLK-per.

PCM-OFFSET Offset in number of data-clock periods added to Time slot

0 0 0: No offset is added

0 0 1: One data clock period is added

...

1 1 1 Seven data clock periods are added

3.5.8 XR7 Extended Register 7

This register contains the 8-bit offset value for the level metering function

Bit 7 0

OF7	OF6	OF5	OF4	OF3	OF2	OF1	OF0

3.5.9 Setting of Slopes in Register XR6

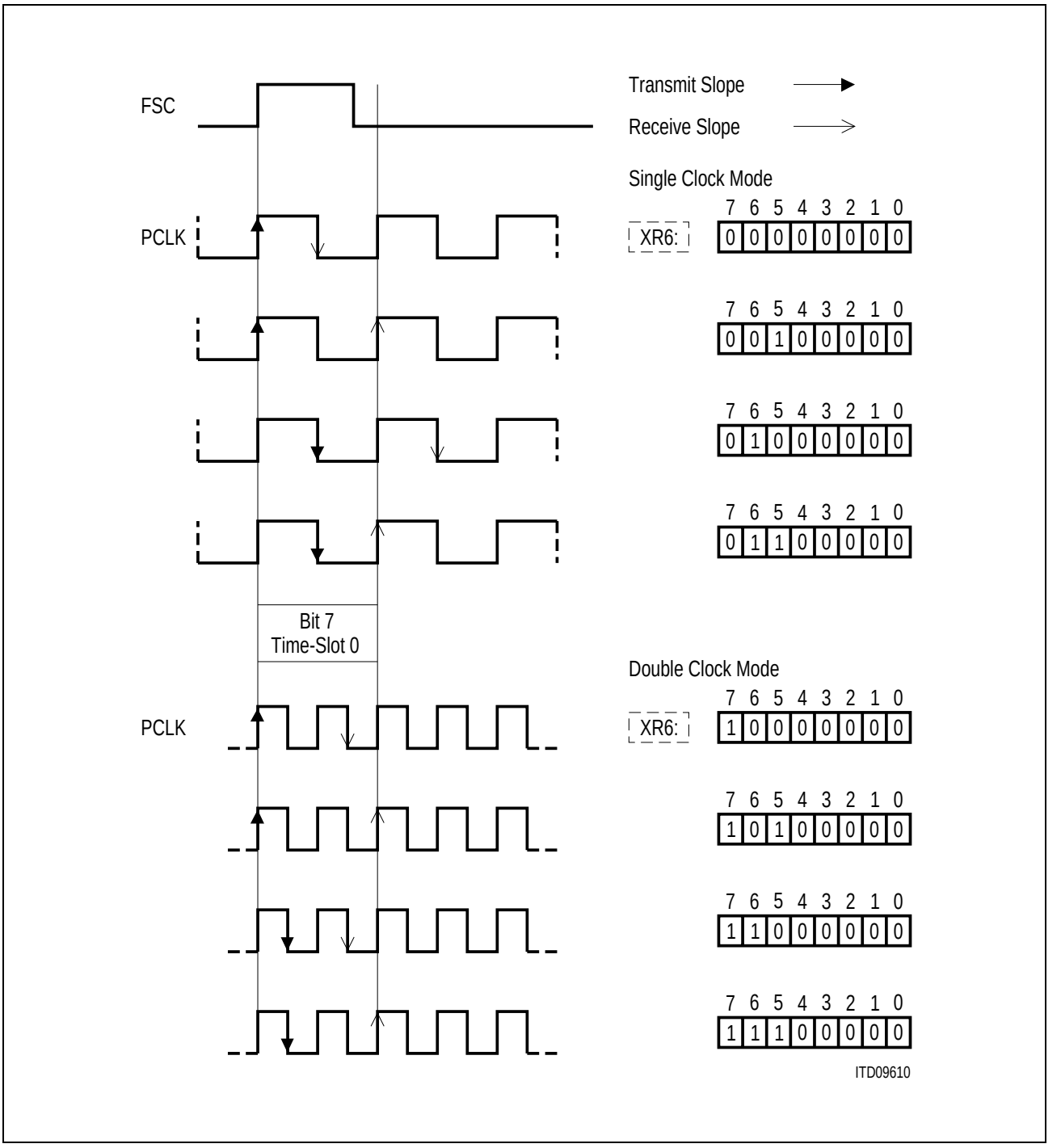


Figure 13

3.6 The Signaling Interface

The µC-SICOFI-4 signaling interface is made up of 2 input pins (SIx_0, SIx_1), two output pins (SOx_0, SOx_1) and three bi-directional programmable pins (SBx_0, SBx_1, SBx_2) per channel.

Additional two interrupt pins (INT12, INT34) are provided. If one of the input pins for channel 1 or 2, or one of the bi-directional pins for channel 1 and 2 (if programmed as inputs) changes, and being stable for the debounce time specified in Register XR4, INT12 will go from '0' to '1'. This interrupt is cleared if the appropriate registers (XR0, XR1 and XR3) are read via the serial µC-interface. Pin INT34 provides the same functionality for channel 3 and 4.

For special purposes two additional output signals are provided by the PEB 2466.

CHCLK1 (see also register XR4) will provide a programmable time period of 2 to 28 ms. CHCLK2 will provide 3 different frequencies (256 kHz, 512 kHz or 16384 kHz). Both signals are only available if a valid signal is applied to the MCLK-pin.

3.6.1 Operating Modes

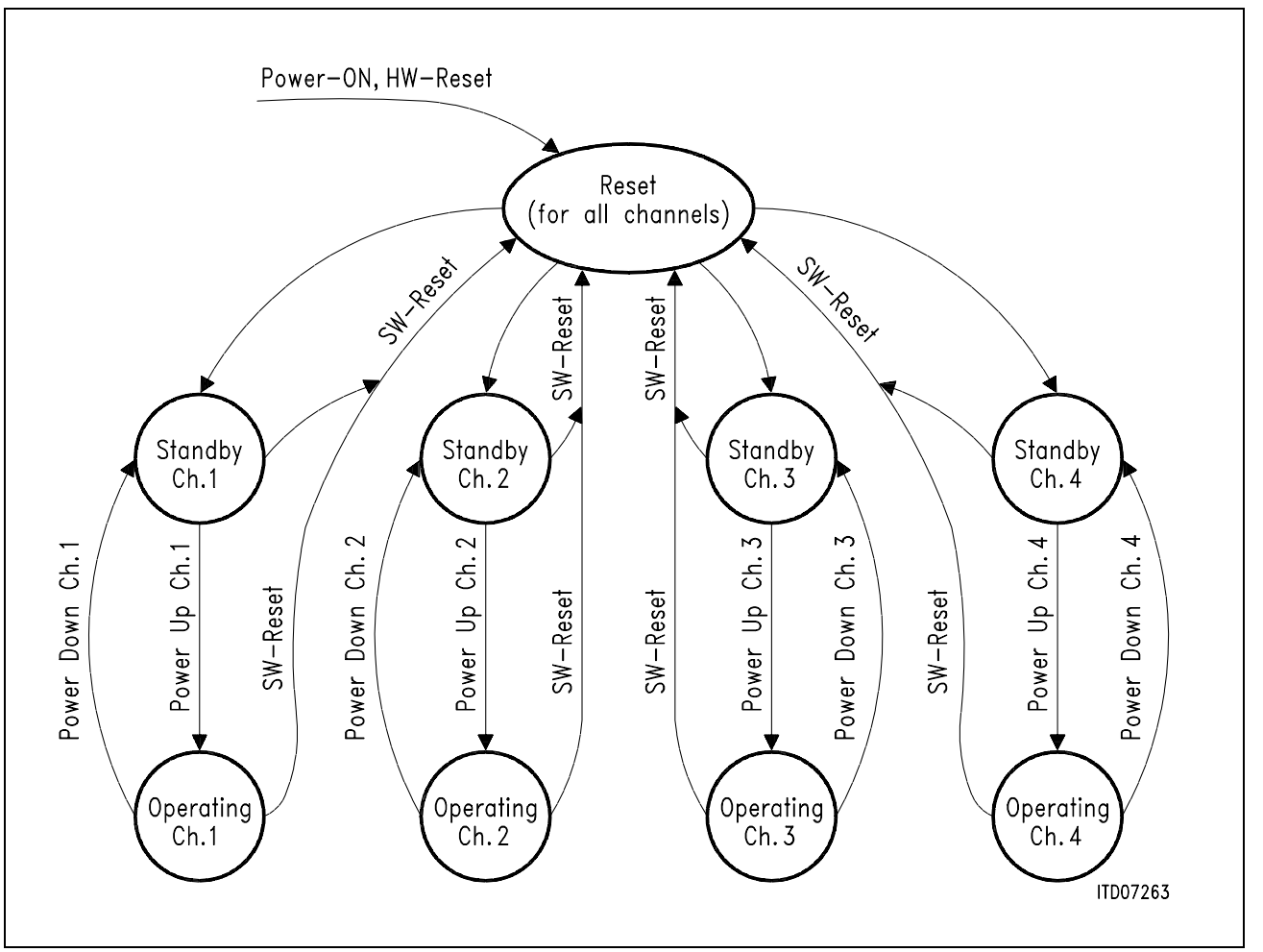


Figure 14

RESET (Basic Setting Mode)

Upon initial application of V_{DD} or resetting pin RESET to '0' during operation, or by software-reset (see XOP command), the SICOFI-4-µC enters a basic setting mode. Basic setting means, that the SICOFI-4-µC configuration registers CR0... CR6 and XR0... XR7 are initialized to '0' for all channels.

All programmable filters are disabled, all programmable command/indication pins are inputs. The two tone generators as well as any testmodes are disabled. There is no persistence checking. Receive signaling registers are cleared. DOUT-pin is in high impedance state, the analog outputs and the signaling outputs are forced to ground.

CR0.. CR6	00_H
XR0.. XR7	00_H
Coefficient-RAM	Old value
Command Stack	Cleared
DIN-input	Ignored
DOUT-output	High impedance
VOUT1,2,3,4	GNDA1,2,3,4
SBx_y	Input
SOx_y	GNDD

If any voltage is applied to any input-pin before initial application of V_{DD}, the SICOFI-4-µC may not enter the basic setting mode. In this case it is necessary to reset the SICOFI-4-µC or to initialize the SICOFI-4-µC configuration registers to '0'.

The SICOFI-4-µC leaves this mode automatically after the RESET-pin is released.

Standby Mode

After releasing the RESET-pin, (RESET-state), the SICOFI-4-µC will enter the Standby mode. The SICOFI-4-µC is forced to standby mode with the PU-bit set to '0' in the CR1-register (POWERDOWN). All 4 channels must be programmed separately. During standby mode the serial SICOFI-4-µC µ-Controller interface is ready to receive and transmit commands and data. Received voice data on DRA, DRB-pin will be ignored. SICOFI-4-µC configuration registers and Coefficient-RAM can be loaded and read back in this mode. Data on signaling input pins can be read via the µ-Controller interface.

DXA, DXB	High 'Z'
VOUT1, 2, 3, 4	GNDA1, 2, 3, 4

Operating Mode

The operating mode for any of the four channels is entered upon recognition of a PU-bit set to ‘1’ in a CR1-register for the specific channel.

3.6.2 Programmable Filters

Based on an advanced digital filter concept, the PEB 2466 provides excellent transmission performance and high flexibility. The new filter concept leads to a maximum independence between the different filter blocks.

Impedance Matching Filter

- Realization by 3 different loops
  - 4 MHz: Multiplication by a constant (12 bit)
  - 128 kHz: Wave Digital Filter (IIR) (60 bit)
    Improves low frequency response
  - 64 kHz: FIR-Filter (48 bit)
    For fine-tuning
- Improved stability behavior of feedback loops
- Real part of termination impedance positive under all conditions
- Improved overflow performance for transients
- Return loss better 30 dB

Transhybrid Balancing (TH) Filter

- New concept: 2 loops at 16 kHz
- Flexible realization allows optimization of wide impedance range
- Consists of a fixed and a programmable part
  - 2nd order Wave Digital Filter (IIR) (106 bit)
    Improves low frequency response
  - 7-TAP FIR-Filter (84 bit)
    For fine-tuning
- Trans-Hybrid-Loss better 30 dB (typically better 40 dB, device only)
- Adaptation to different lines by:
  - Easy selection between four different downloaded coefficient sets

Filters for Frequency Response Correction

- For line equalization and compensation of attenuation distortion
- Improvement of Group-Delay-Distortion by using minimum phase filters (instead of linear phase filters)
- FRR filter for correction of receive path distortion
  - 5 TAP programmable FIR filter operating at 8 kHz (60 bit)
- FRX filter for correction of transmit path distortion
  - 5 TAP programmable FIR filter operating at 8 kHz (60 bit)
- Frequency response better 0.1 dB

Amplification/Attenuation -Filters AX1, AX2, AR1, AR2

- Improved level adjustment for transmit and receive
- Two separate filters at each direction for
  - Improved trans-hybrid balancing
  - Optimal adjustment of digital dynamic range
  - Gain adjustments independent of TH-filter

Amplification/Attenuation Receive (AR1, AR2)-Filter

Step size for AR-Filter	range 3 .. – 14 dB:	step size 0.02 .. 0.05 dB
	range – 14 .. – 24	step size 0.5 dB

Amplification/Attenuation Transmit (AX1, AX2)-Filter

Step size for AX-Filter	range – 3 .. 14 dB:	step size 0.02 .. 0.05 dB
	range 14 .. 24 dB:	step size 0.5 dB

3.6.3 QSICOS Software

The QSICOS-software has been developed to help to obtain an optimized set of coefficients both quickly and easily. The QSICOS program runs on any PC with at least 575 Kbytes of memory. This also requires MS-DOS Version 5.0 or higher, as well as extended memory.

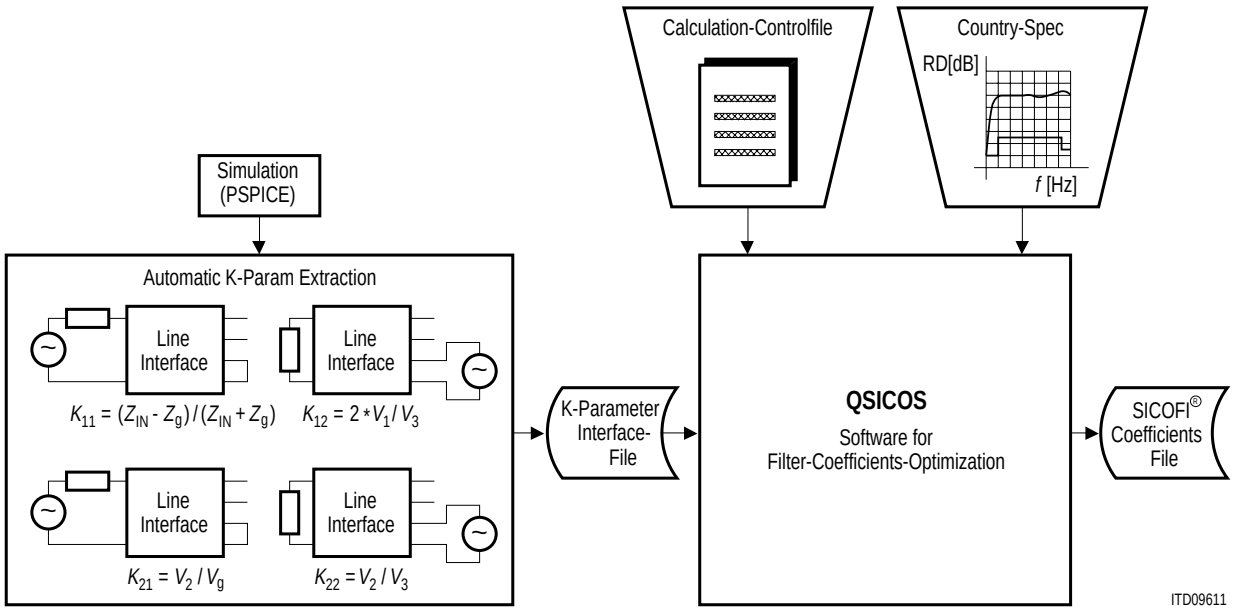


Figure 15

QSICOS Supports:

- **Calculation of Coefficients for the**
  - Impedance Filter (IM) for return loss calculation (please note that the IM filter coefficients are different for the PEB 2466 and for the PEB 2465. QSICOS calculates the programming bytes for the SICOFI-4 IOM version PEB 2465. These bytes have to be converted with an additional tool to get the required PEB 2466 programming bytes. The conversion tool QSUCCONV.EXE is part of the QSICOS software package.)
  - FRR and FRX-filters for frequency response in receive and transmit path
  - AR1, AR2 and AX1, AX2-filter for level adjustment in receive and transmit path
  - Trans Hybrid Balancing Filter (TH) and
  - two programmable tone generators (TG 1 and TG 2)
- **Simulation of the PEB 2466 and SLIC System** with fixed filter coefficients allows simulations of tolerances which may be caused e.g. by discrete external components.
- **Graphical Output of Transfer Functions to the Screen** for
  - Return Loss
  - Frequency responses in receive and transmit path
  - Transhybrid Loss
- **Calculation of the PEB 2466 and SLIC system Stability**. The IM-filter of the PEB 2466 adjust the total system impedance by making a feedback loop. Because the line is also a part of the total system, a very robust method has to used to avoid oscillations and to ensure system stability. The input impedance of the PEB 2466 and SLIC combination is calculated. If the real part of the system input impedance is positive, the total system stability can be guaranteed.

4 Transmission Characteristics

The figures in this specification are based on the subscriber-line board requirements. The proper adjustment of the programmable filters (transhybrid balancing, impedance matching, frequency-response correction) requires a complete knowledge of the µC-SICOFI-4's analog environment. Unless otherwise stated, the transmission characteristics are guaranteed within the test conditions.

Test Conditions

T_A = 0 °C to 70 °C; V_{DD} = 5 V ± 5%; GNDA1..4 = GNDD = 0 V
R_L[1] > 300 Ω; C_L < 50 pF; H(IM) = H(TH) = 0; H(R1) = H(FRX) = H(FRR) = 1;
HPR and HPX enabled;
AR[2]= 0 to – 9 dB
AX[3]= 0 to 9 dB for A-Law, 0 to 7 dB for µ-Law
f = 1014 Hz; 0 dBm0; A-Law or µ-Law;

AGX = 0 dB, 6.02 dB, AGR = 0 dB, – 6.02dB;

A-Law

A 0 dBm0 signal is equivalent to 1.095 Vrms. A + 3.14 dBm0 signal is equivalent to 1.57 Vrms which corresponds to the overload point of 2.223 V.

When the gain in the receive path is set at 0 dB, an 1014 Hz PCM sinewave input with a level 0 dBm0 will correspond to a voltage of 1.095 Vrms at the analog output.

When the gain in the transmit path is set at 0 dB, an 1014 Hz sine wave signal with a voltage of 1.095Vrms A-Law will correspond to a level of 0 dBm0 at the PCM output.

µ-Law

In transmit direction for µ-law an additional gain of 1.94 dB is implemented automatically, in the companding block (CMP). This additional gain has to be considered at all gain calculations, and reduces possible AX-gain from 9 dB (with A-Law) to 7 dB (with µ-Law)

A 0 dBm0[4] signal is equivalent to 1.0906 Vrms. A + 3.17 dBm0 signal is equivalent to 1.57 Vrms which corresponds to the overload point of 2.223 V.

When the gain in the receive path is set at 0 dB, an 1014 Hz PCM sinewave input with a level 0 dBm0 will correspond to a voltage of 1.0906 Vrms at the analog output.

When the gain in the transmit path is set at 0 dB, an 1014 Hz sine wave signal with a voltage of 1.0906 Vrms will correspond to a level of 1.94 dBm0 at the PCM output.

---

1) R_L, C_L forms the load on VOUT
2) Consider, in a complete system, AR = AR1 + AR2 + FRR + R1
3) Consider, in a complete system, AX = AX1 + AX2 + FRX
4) The absolute power level in decibels referred to (a point of zero relative level) the PCM interface levels.

Transmission Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Gain absolute (AGX = AGR = 0) T_A= 25 °C; V_{DD} = 5 V T_A = 0 – 70 °C; V_{DD} = 5 V ± 5%	G	 – 0.15 – 0.25	 ± 0.10	 + 0.15 + 0.25	 dB dB
Gain absolute (AGX = 6.02 dB, AGR = – 6.02 dB) T_A = 25°C; V_{DD} = 5 V T_A = 0-70°C; V_{DD} = 5 V ± 5%	G	 – 0.15 – 0.25	 ± 0.10	 + 0.15 + 0.25	 dB dB
Harmonic distortion, 0 dBm0; f = 1000 Hz; 2nd, 3rd order	HD		– 50	– 44	dB
Intermodulation[1)] R_2 R_3	IMD IMD			– 46 – 56	dB dB
Crosstalk 0 dBm0; f = 200 Hz to 3400 Hz any combination of direction and channel	CT		– 85	– 80	dB
Idle channel noise, Transmit, A-law, psophometric (V_{IN} = 0 V) Transmit, µ-law, C-message (V_{IN} = 0 V) Transmit, µ-law, C-message (V_{IN} = 0V) Receive, A-law, psophometric (idle code + 0) Receive, µ-law, C-message (idle code + 0) Receive, µ-law, C-message (idle code + 0)	 N_{TP} N_{TC} N_{TC} N_{RP} N_{RC} N_{RC}		 – 85 5 5	 – 67.4 17.5 17.5 – 78.0 12.0 12.0	 dBm0p dBmc dBrnC0 dBm0p dBmc dBrnC0

1) Using equal-level, 4-tone method (EIA) at a composite level of – 13 dBm0 with frequencies in the range between 300 Hz and 3400 Hz.

4.1 Frequency Response

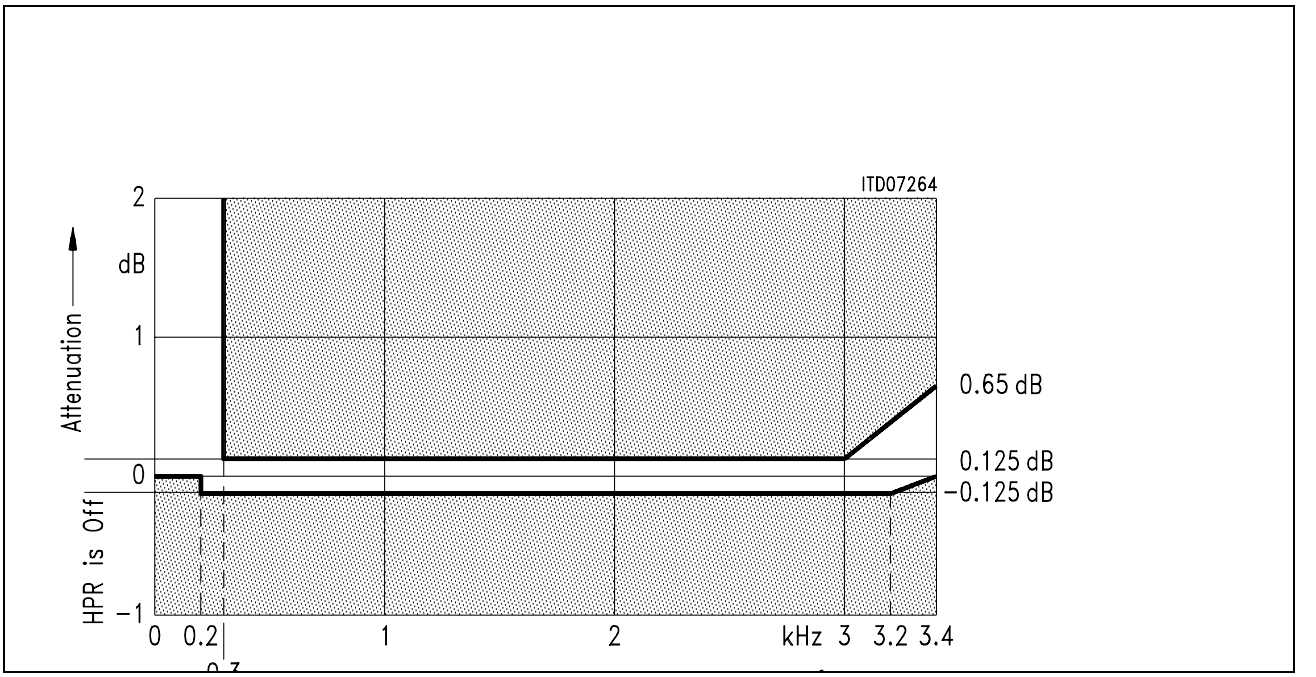


Figure 16
Receive: Reference Frequency 1014 Hz, Input Signal Level 0 dBm0

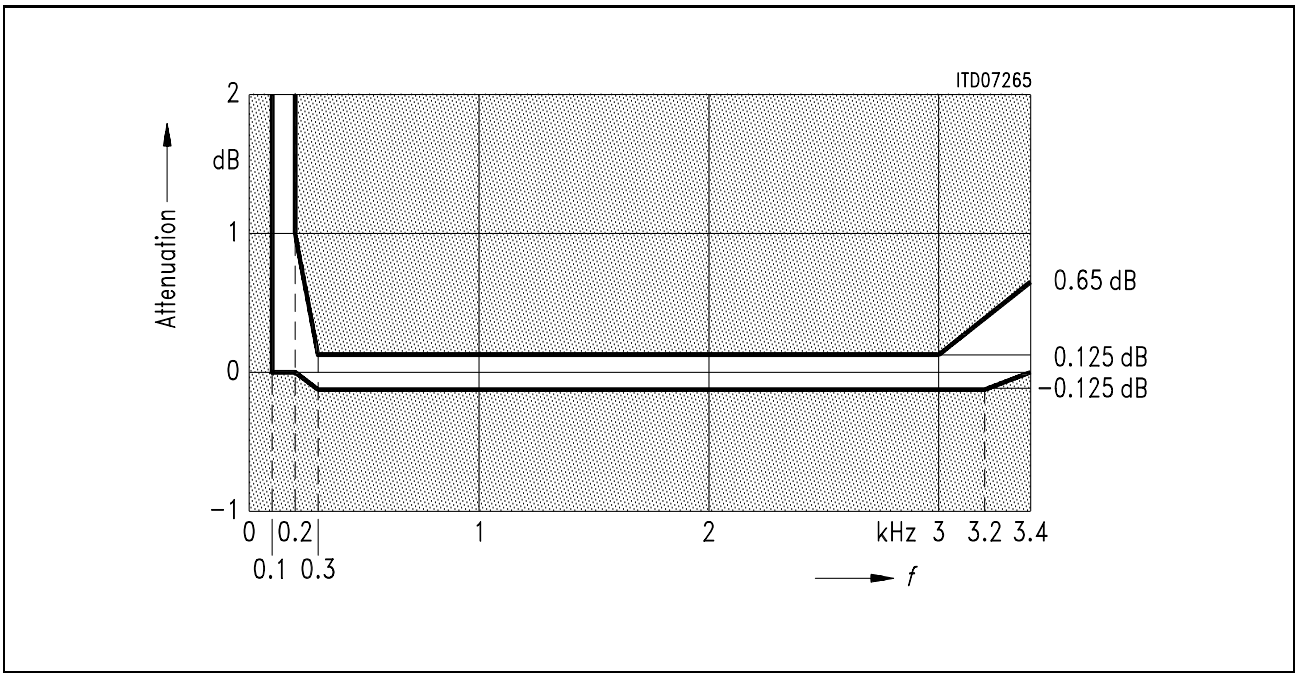


Figure 17
Transmit: Reference Frequency 1014 Hz, Input Signal Level 0 dBm0

4.2 Group Delay

Maximum delays when the SICOFI-4-µC is operating with H(TH) = H(IM) = 0 and H(FRR) = H(FRX) = 1 including delay through A/D- and D/A converters. Specific filter programming may cause additional group delays.

Group delay deviations stay within the limits in the figures below.

Group Delay Absolute Values: Input signal level 0 dBm0

Parameter	Symbol	Limit Values			Unit	Reference
		min.	typ.	max.		
Transmit delay	D_{XA}			300.	µs	
Receive delay	D_{RA}			250	µs	

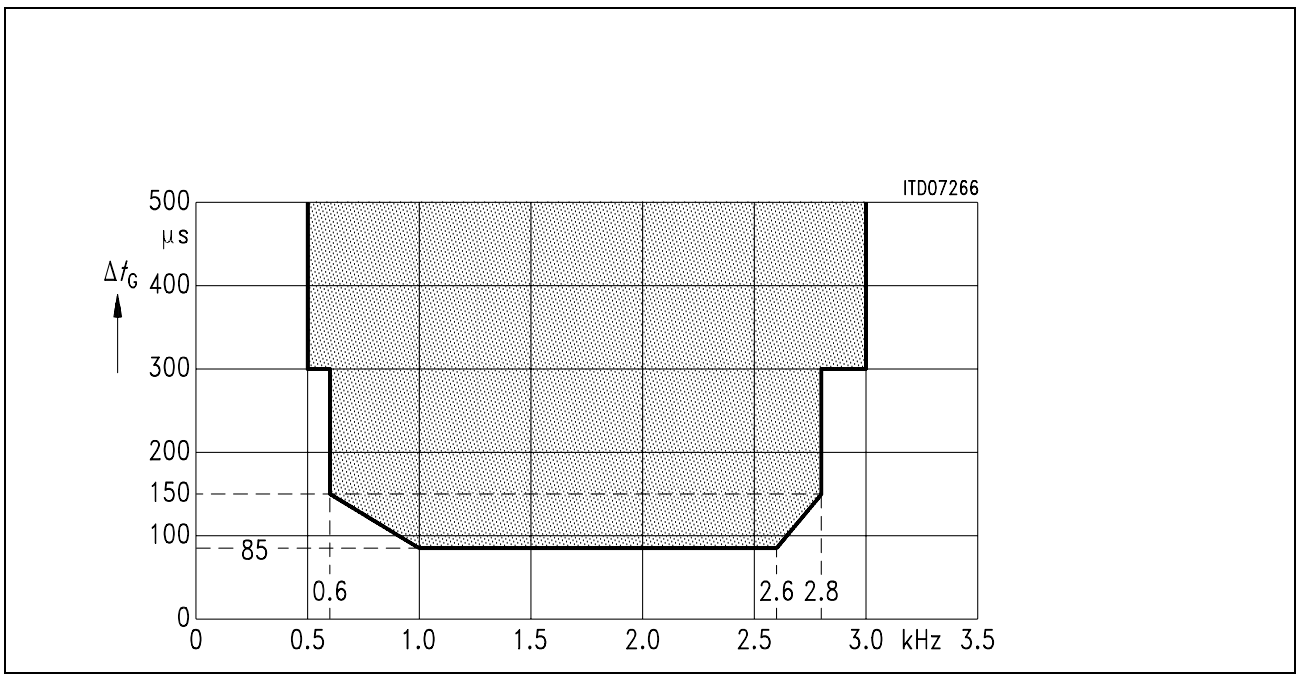


Figure 18
Group Delay Distortion Transmit: Input Signal Level 0 dBm0

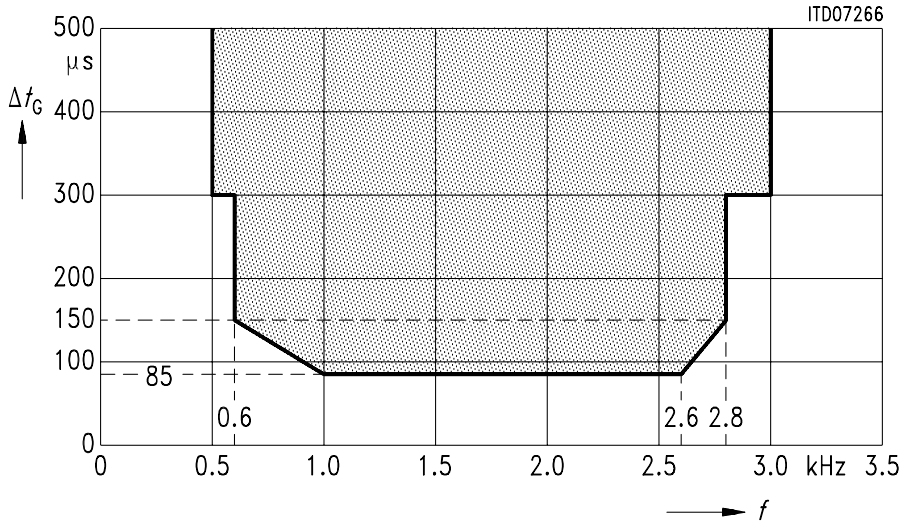
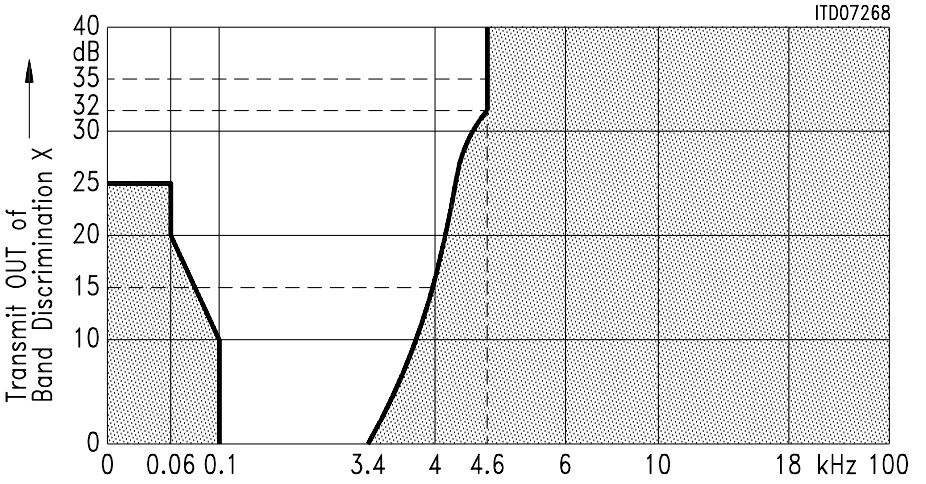


Figure 19
Group Delay Distortion Receive: Input Signal Level 0 dBm0 [1)]

[1)] HPR is switched on: reference point is at t_{Gmin}
HPR is switched off: reference is at 1.5 kHz

4.3 Out-of-Band Signals at Analog Input

With an 0 dBm0 out-of-band sine wave signal with frequency f (<<100 Hz or 3.4 kHz to 100 kHz) applied to the analog input, the level of any resulting frequency component at the digital output will stay at least X dB below a 0 dBm0, 1 kHz sine wave reference signal at the analog input.[1)]



$$3.4 \ldots 4.0 \text{ kHz: } X = -14\left(\sin\left(\pi \frac{4000 - f}{1200}\right) - 1\right)$$

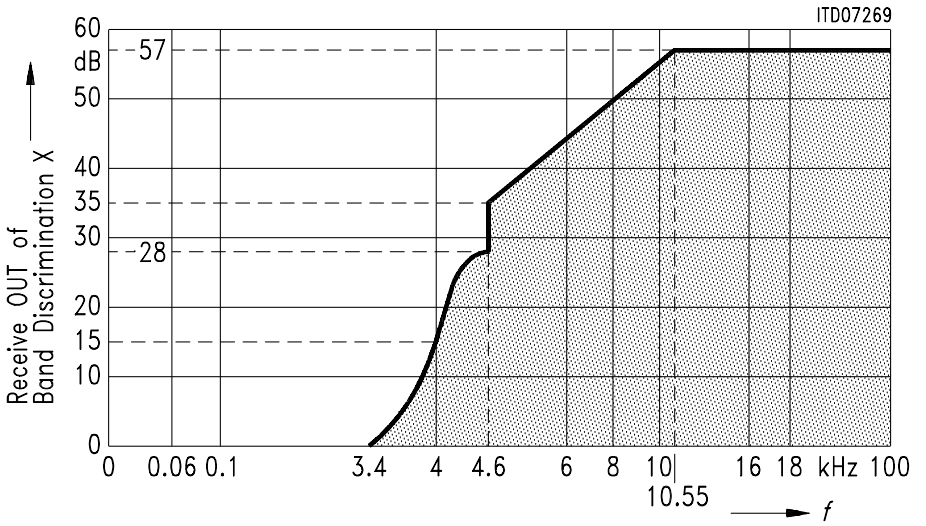
$$4{,}0 \ldots 4.\dot{6} \text{ kHz: } X = -18\left(\sin\left(\pi \frac{4000 - f}{1200}\right) - \frac{7}{9}\right)$$

Figure 20

1) Poles at 12 kHz ± 150 Hz and 16 kHz ± 150 Hz are provided

4.4 Out-of-Band Signals at Analog Output

With a 0 dBm0 sine wave with frequency f (300 Hz to 3.99 kHz) applied to the digital input, the level of any resulting out-of-band signal at the analog output will stay at least X dB below a 0 dBm0, 1 kHz sine wave reference signal at the analog output.



$$3.4 \ldots 4.6 \text{ kHz: } X = -14\left(\sin\left(\pi\,\frac{4000-f}{1200}\right)-1\right)$$

Figure 21

4.5 Out of Band Idle Channel Noise at Analog Output

With an idle code applied to the digital input, the level of any resulting out-of-band power spectral density (measured with 3 kHz bandwidth) at the analog output, will be not greater than the limit curve shown in the figure below.

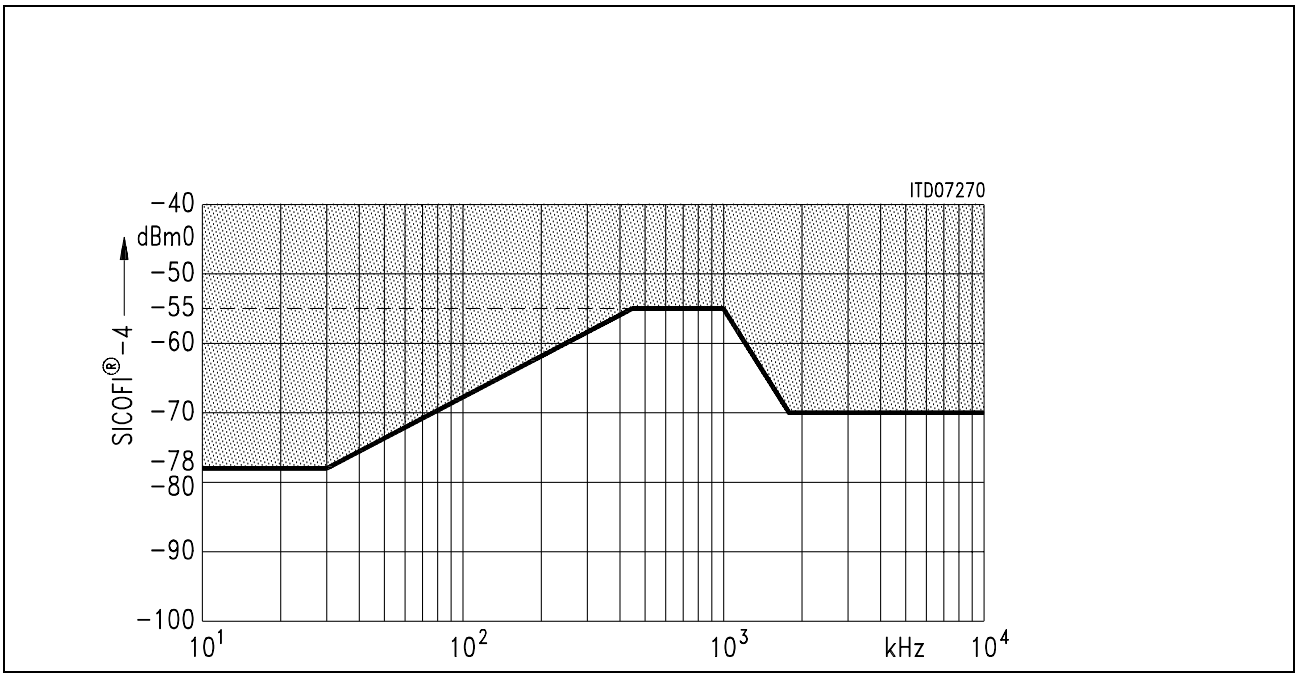


Figure 22

4.6 Overload Compression

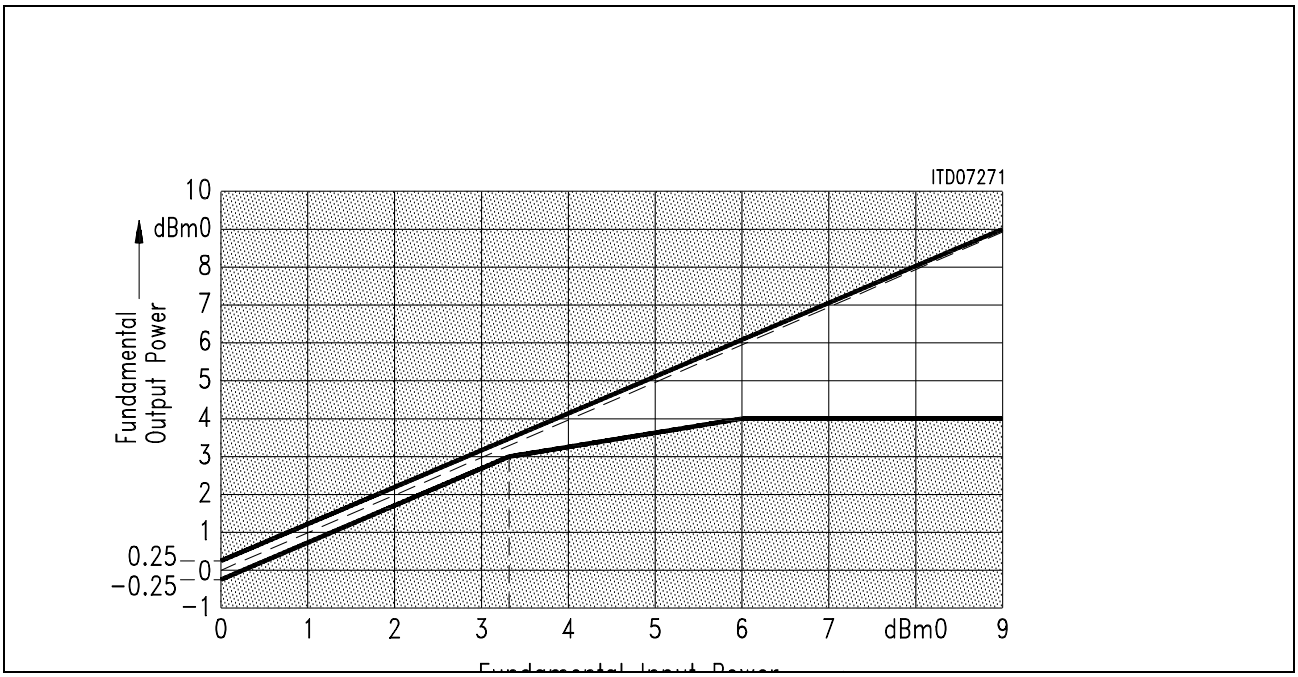


Figure 23
μ-Law, Transmit: measured with sine wave f = 1014 Hz.

4.7 Gain Tracking (receive or transmit)

The gain deviations stay within the limits in the figures below.

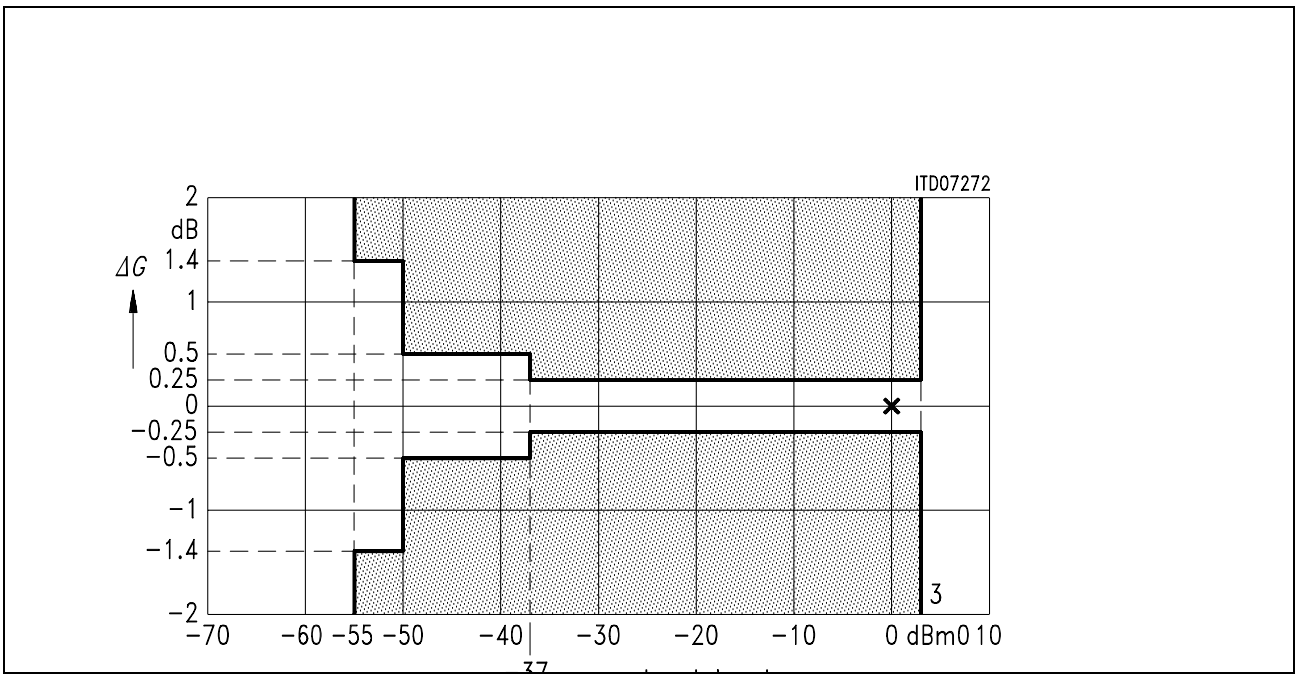


Figure 24
Gain Tracking: (measured with sine wave f = 1014 Hz, reference level is 0 dBm0)

4.8 Total Distortion

The signal to distortion ratio exceeds the limits in the following figure.

4.8.1 Total Distortion Measured with Sine Wave

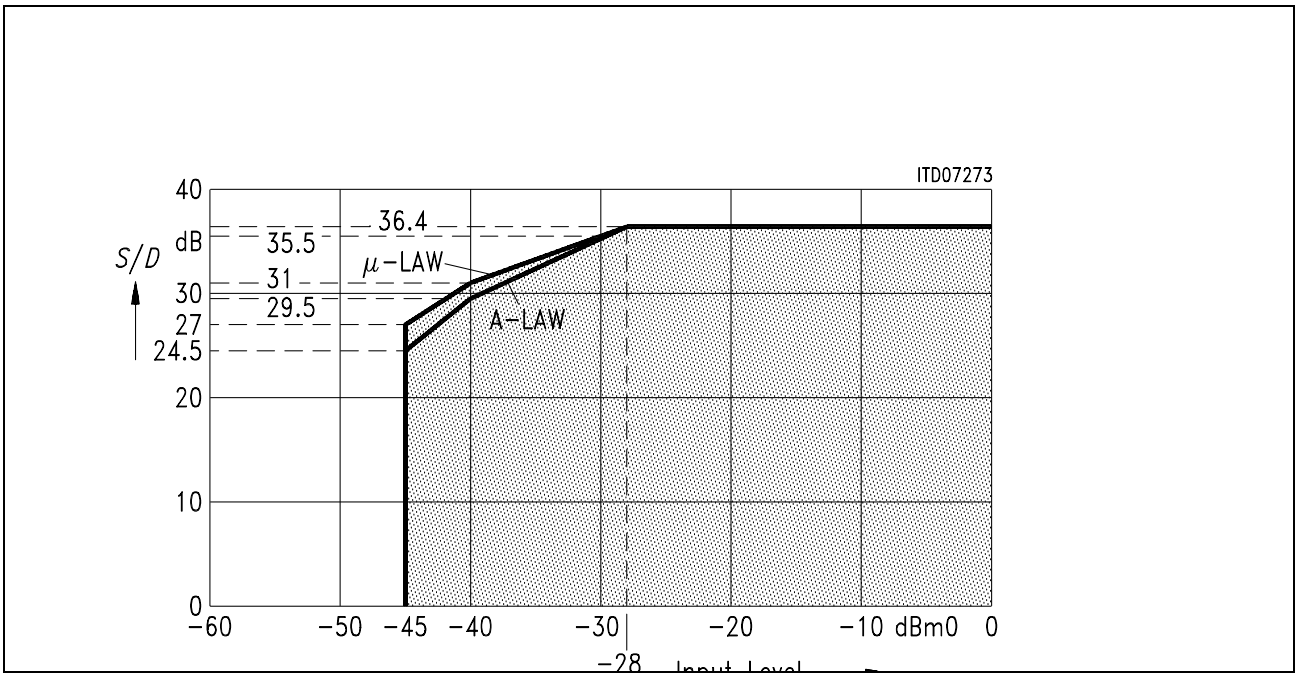


Figure 25
Receive or Transmit: measured with sine wave f = 1014 Hz. (C-message weighted for μ-law, psophometricaly weighted for A-law)

4.8.2 Total Distortion Measured with Noise According to CCITT

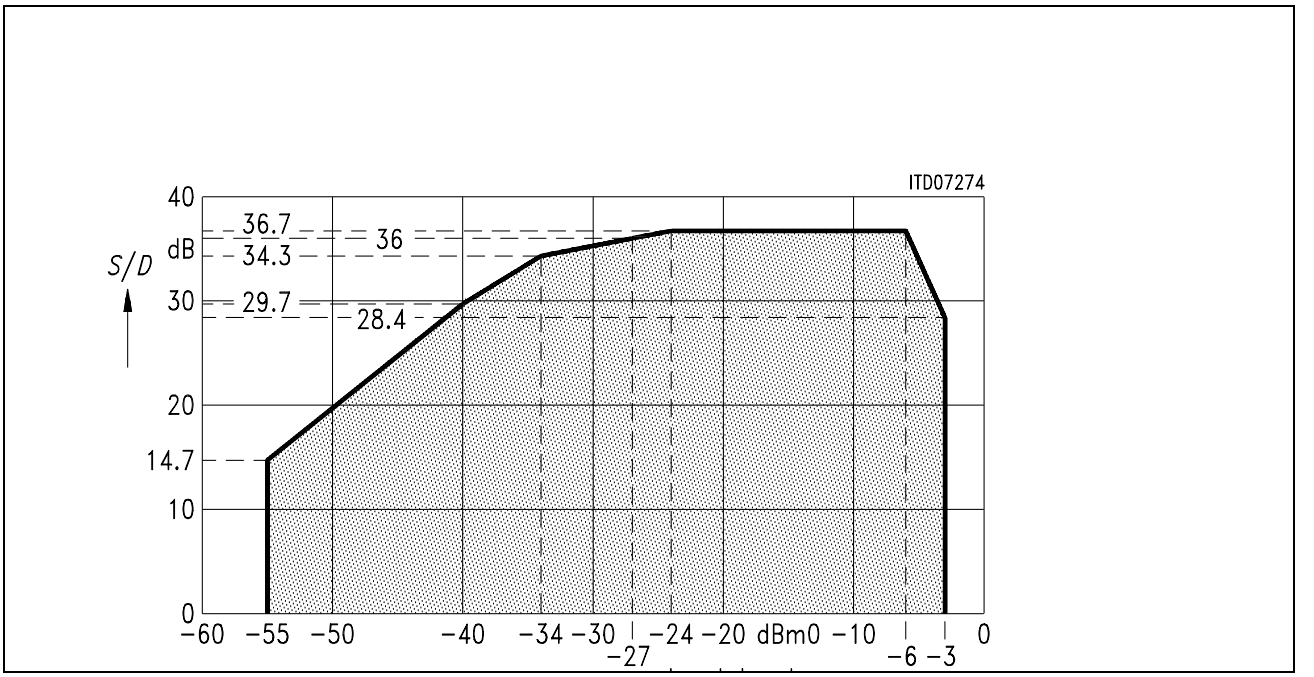


Figure 26
Receive

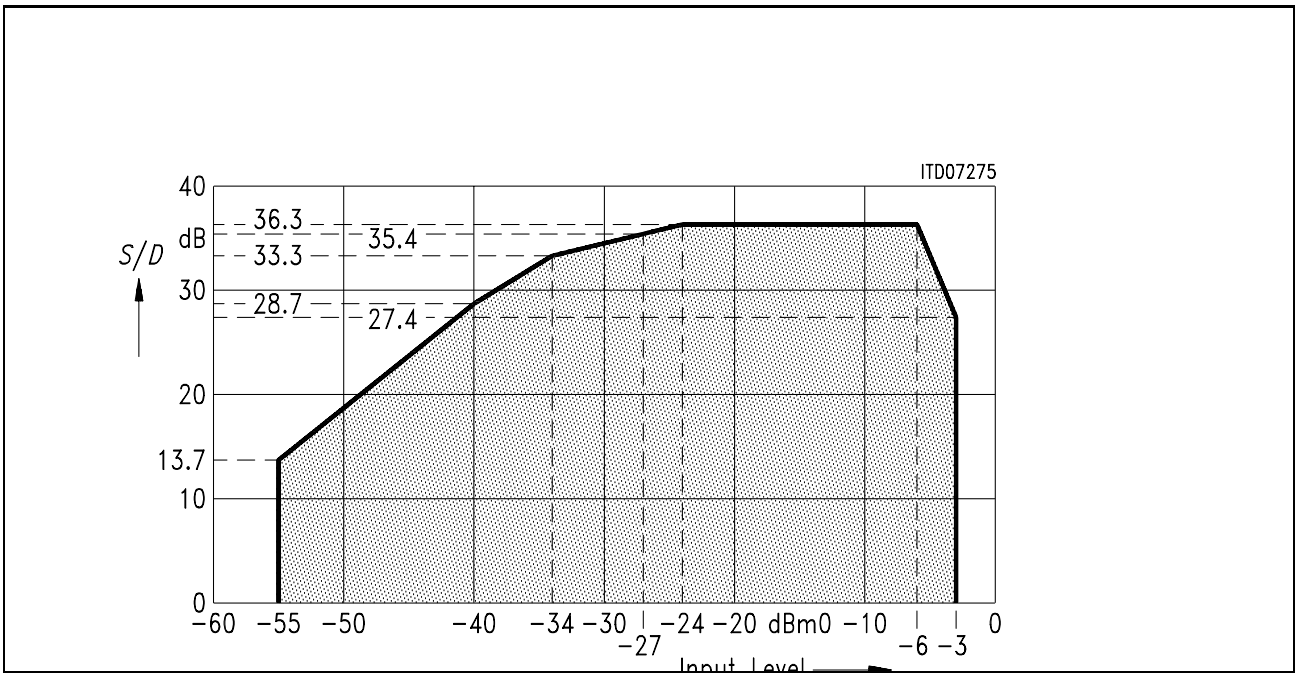


Figure 27
Transmit

4.9 Single Frequency Distortion

An input signal with its frequency swept between 0.3 to 3 kHz for the receive path, or 0 to 12 kHz for the transmit path, any generated output signal with other frequency than the input frequency will stay 28 dB below the maximum input level of 0 dBM0.

Receive		Transmit	
Frequency	**Max Input Level**	**Frequency**	**Max. Input Level**
300 Hz to 3.4 kHz	0 dBm0	0 to 12 kHz	0 dBm0

4.10 Transhybrid Loss

The quality of Transhybrid-Balancing is very sensitive to deviations in gain and group delay - deviations inherent to the SICOFI-4-µC A/D- and D/A-converters as well as to all external components used on a line card (SLIC, OP's etc.)

Measurement of SICOFI-4-µC Transhybrid-Loss: A 0 dBm0 sine wave signal and a frequency in the range between 300-3400 Hz is applied to the digital input. The resulting analog output signal at pin V_{OUT} is directly connected to V_{IN}, e.g. with the SICOFI-4-µC testmode "Digital Loop Back via Analog Port". The programmable filters FRR, AR, FRX, AX and IM are disabled, the balancing filter TH is enabled with coefficients optimized for this configuration (V_{OUT} = V_{IN}).

The resulting echo measured at the digital output is at least X dB below the level of the digital input signal as shown in the table below. (Filter coefficients will be provided)

Parameter	**Symbol**	**Limit Values**		**Unit**	**Test Condition**
		min.	**typ.**		
Transhybrid Loss at 300 Hz	THL_{300}	27	40	dB	T_A = 25 °C; V_{DD} = 5 V;
Transhybrid Loss at 500 Hz	THL_{500}	33	45	dB	T_A = 25 °C; V_{DD} = 5 V;
Transhybrid Loss at 2500 Hz	THL_{2500}	29	40	dB	T_A = 25 °C; V_{DD} = 5V;
Transhybrid Loss at 3000 Hz	THL_{3000}	27	35	dB	T_A = 25 °C; V_{DD} = 5V;
Transhybrid Loss at 3400 Hz	THL_{3400}	27	35	dB	T_A = 25 °C; V_{DD} = 5 V

The listed values for THL correspond to a typical variation of the signal amplitude and delay in the analog blocks.

Δamplitude = typ. $\pm$ 0.15 dB
Δdelay = typ $\pm$ 0.5 µs

5 Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
V_{DD} referred to GNDD		– 0.3	7.0	V	
GNDA to GNDD		– 0.6	0.6	V	
Analog input and output voltage Referred to V_{DD} = 5 V; Referred to GNDA = 0 V		 – 5.3 – 0.3	 0.3 5.3	 V V	
All digital input voltages Referred to GNDD = 0 V; (V_{DD} = 5V) Referred to V_{DD} = 5 V; (GNDD = 0 V)		 – 0.3 – 5.3	 5.3 0.3	 V V	
DC input and output current at any input or output pin (free from latch-up)			10	mA	
Storage temperature	T_{STG}	– 60	125	°C	
Ambient temperature under bias	T_A	– 10	80	°C	
Power dissipation (package)	P_D		1	W	

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Range

T_A = 0 to 70 °C; V_{DD} = 5 V ± 5%; GNDD = 0 V; GNDA = 0 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
V_{DD} supply current standby Operating (4 channels)	I_{DIN}		 0.5 26	 1.0 40	 mA mA	
Power supply rejection Of either supply/direction Receive V_{DD} target value	$PSRR$	 30 14			 dB dB	Ripple: 0 to 150 kHz, 70 mVrms Measured: 300 Hz to 3.4 kHz Measured: at *f*: = 3.4 to 150 kHz
Power dissipation standby[1)]	P_{DS}		2.5	6	mW	
Power dissipation operating	P_{Do1}		100	175	mW	1 channel
Power dissipation operating	P_{Do2}		110	200	mW	2 channels
Power dissipation operating	P_{Do3}		120	225	mW	3 channels
Power dissipation operating	P_{Do4}		130	250	mW	4 channels

1) Power dissipation values are target values

Note: In the operating range the functions given in the circuit description are fulfilled.

Digital Interface

T_A = 0 to 70 °C; V_{DD} = 5 V ± 5%; GNDD = 0 V; GNDA = 0 V

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Low-input voltage	V_{IL}	– 0.3	0.8	V	
High-input voltage	V_{IH}	2.0		V	
Low-output voltage	V_{OL}		0.45	V	I_0 = – 5mA
High-output voltage	V_{OH}	4.4		V	I_0 = 5 mA
Input leakage current	V_{IL}		± 1	µA	– 0.3 ≤ V_{IN} ≤ V_{DD}

Analog Interface

T_A = 0 to 70 °C; V_{DD} = 5 V ± 5%; GNDD = 0 V; GNDA = 0 V

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Analog input resistance	R_i	160	270	380	kΩ	
Analog output resistance	R_O			0.25	Ω	
Analog output load	R_L C_L	300		 50	Ω pF	
Input leakage current	I_{IL}		± 0.1	± 1.0	µA	$0 \le V_{IN} \le V_{DD}$
Input offset voltage	V_{IO}			± 50	mV	
Output offset voltage	V_{OO}			± 50	mV	
Input voltage range (AC)	V_{IN}			± 2.223	V	

5.1 Coupling Capacitors at the Analog Interface

In Transmit direction, a 39 nF capacitor has to be connected to V_{IN}-pins. To fulfil the frequency response requirement in Receive direction, the value of the coupling capacitor (C_{ext1}) needed, depends on the input resistance of the SLIC-circuitry (equals the Analog-Output-Load: R_{Load}).

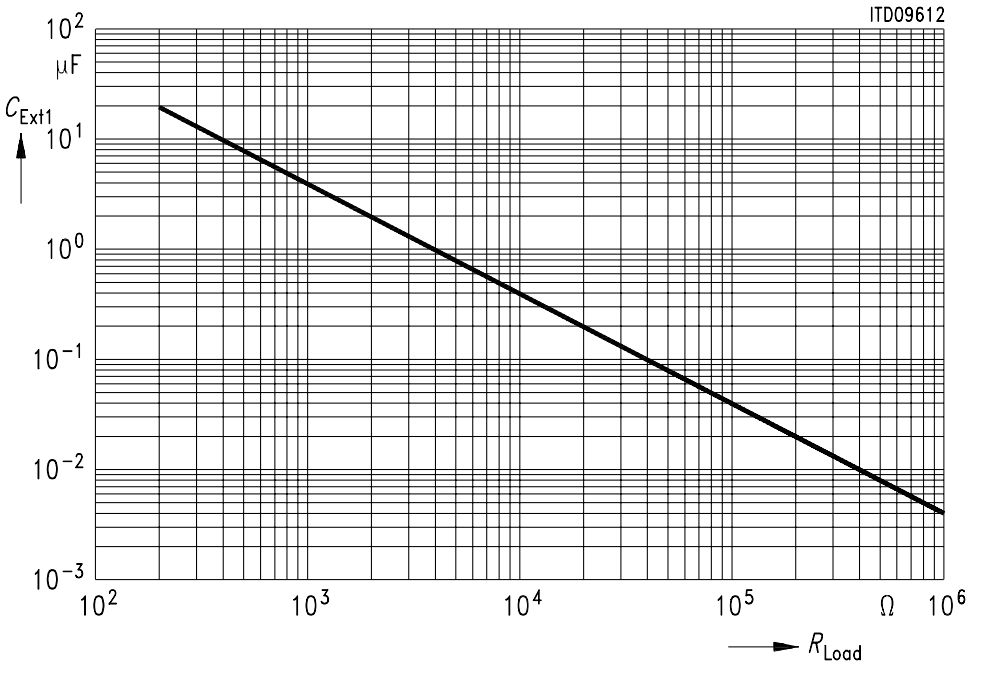


Figure 28

5.2 Reset Timing

To reset the SICOFI-4-µC to basic setting mode, negative pulses applied to pin RESET have to be lower than 1.2 V (TTL-Schmitt-Trigger Input) and have to be longer than 3 µs. Spikes shorter than 1 µs will be ignored.

5.3 PCM-Interface Timing

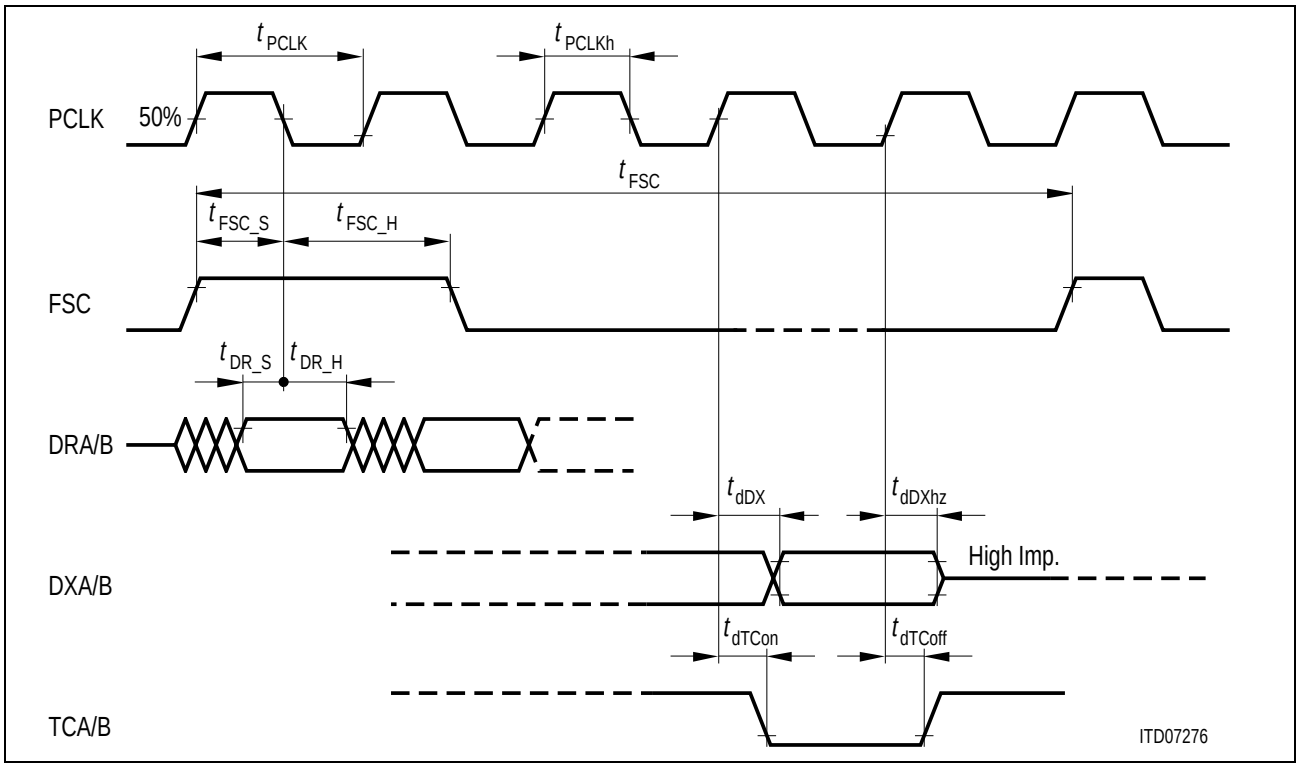


Figure 29
Single Clocking Mode

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period of PCLK	t_{PCLK}	1/8192		1/128	ms
PCLK high time	t_{PCLKh}		$t_{PCLK/2}$		µs
Period FSC	t_{FSC}		125		µs
FSC setup time	t_{FSC_s}	10	50		ns
FSC hold time	t_{FSC_h}	(t_{PCLK} - t_{PCLKh}) + 10	(t_{PCLK} - t_{PCLKh}) + 50		ns
DRA/B setup time	t_{DR_s}	10	50		ns
DRA/B hold time	t_{DR_h}	10	50		ns
DXA/B delay time [1)]	t_{dDX}	25	50 (@ 200 pF)		ns
DXA/B delay time to high Z	t_{dDXhz}	25	50		ns
TCA/B delay time on	t_{dTCon}	25	50		ns
TCA/B delay time off	t_{dTCoff}	25	100		ns

1) All delay times are made up by two components: an intrinsic time (min-time), caused by internal processings, and a second component caused by external circuitry (C-load)

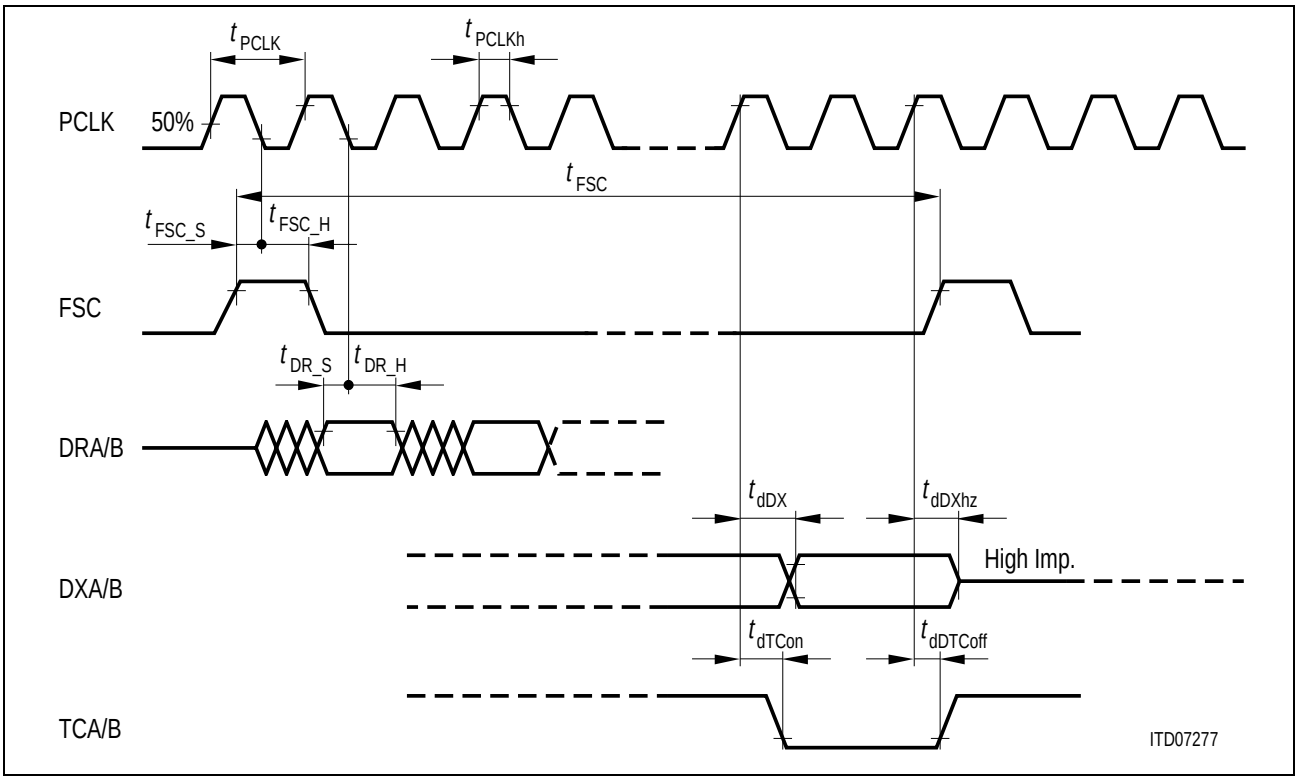


Figure 30
Double Clocking Mode

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period of PCLK	t_{PCLK}	1/8192		1/256	ms
PCLK high time	t_{PCLKh}		$t_{PCLK/2}$		µs
Period FSC	t_{FSC}		125		µs
FSC setup time	t_{FSC_s}	10	50		ns
FSC hold time	t_{FSC_h}	2 x (t_{PCLK} – t_{PCLKh}) + 10	2 x (t_{PCLK} – t_{PCLKh}) + 50		ns
DRA/B setup time	t_{DR_s}	10	50		ns
DRA/B hold time	t_{DR_h}	10	50		ns
DXA/B delay time [1)]	t_{dDX}	25	50 (@200 pF)		ns
DXA/B delay time to high Z	t_{dDXhz}	25	50		ns
TCA/B delay time on	t_{dTCon}	25	50		ns
TCA/B delay time off	t_{dTCoff}	25	100		ns

1) All delay times are made up by two components: an intrinsic time (min-time), caused by internal processings, and a second component caused by external circuitry (C-load)

5.4 µ-Controller Interface Timing

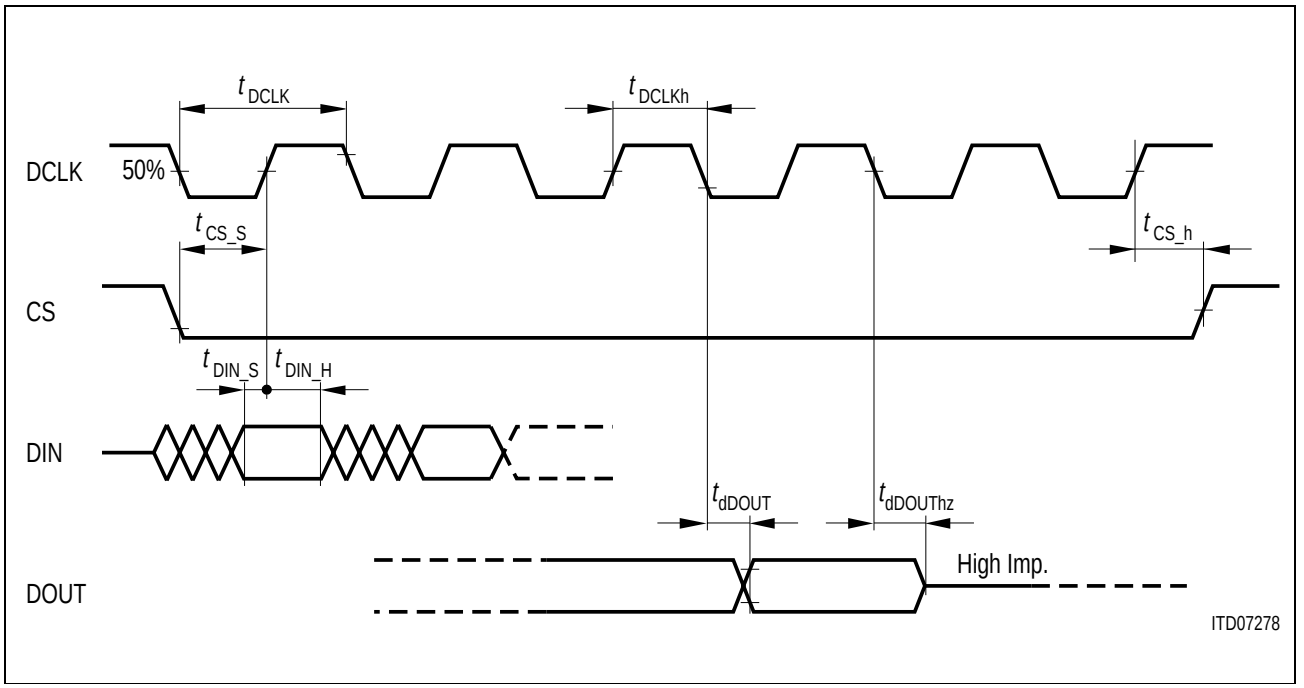


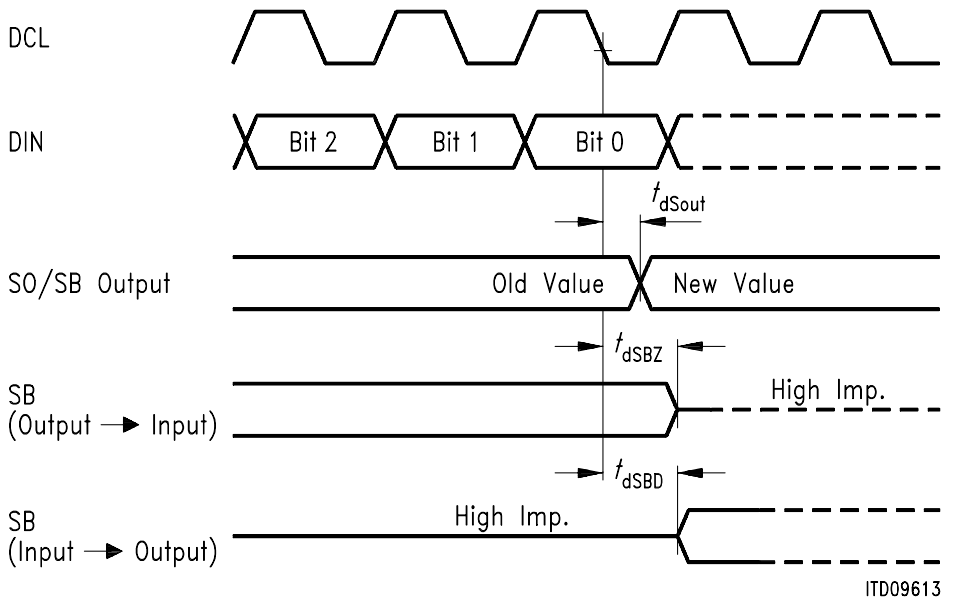
Figure 31

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period of DCLK	t_{DCLK}	1/8192			ms
DCLK high time	t_{DCLKh}		$t_{DCLK/2}$		µs
CS setup time	t_{CS_s}	10	50		ns
CS hold time	t_{CS_h}	30	50		ns
DIN setup time	t_{DIN_s}	10	50		ns
DIN hold time	t_{DIN_h}	10	50		ns
DOUT delay time [1)]	t_{dDOUT}	30	100		ns
DOUT delay time to high Z	$t_{dDOUThz}$	30	100		ns

1) All delay times are made up by two components: an intrinsic time (min-time), caused by internal processings, and a second component caused by external circuitry (C-load)

5.5 Signaling Interface

5.6 From the µC-interface to the SO/SB-pins (data downstream)



Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
SO/SB delay time [1]	t_{dSout}	30	100		ns
SB to 'Z' - time	t_{dSBZ}	40	100		ns
SB to 'drive'-time	t_{dSBD}	40	100		ns

[1] All delay times are made up by two components: an intrinsic time (min-time), caused by internal processings, and a second component caused by external circuitry (C-load)

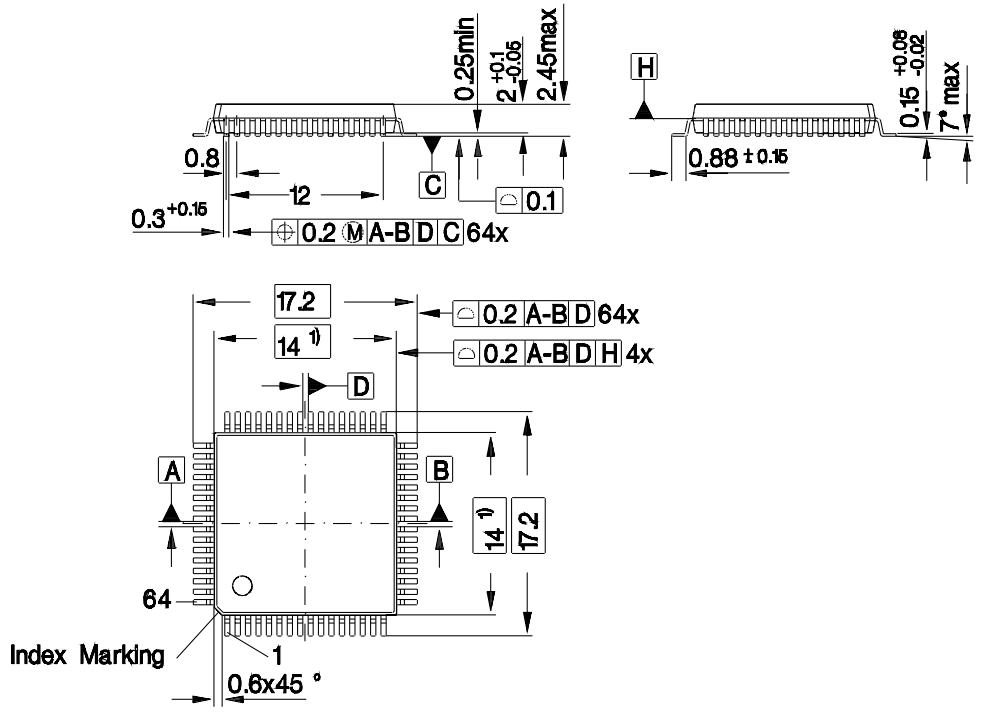
5.7 From the SI/SB-pins to the µC-interface (data upstream)

There is no way specifying the time when data applied to SI-pins (and SB-pins if programmed as signaling input pins) is sampled by the PEB 2466.

The time only depends on internal signals (16 MHz masterclock, and status of various counters), and there is no link to a low frequency external signal.

6 Package Outlines

P-MQFP-64
(Plastic Metric Quad Flat Package)



Sorts of Packing
Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

7 Appendix

7.1 Level Metering Function

This function allows a selftest of the SICOFI-4 and also of the SLIC circuitry connected to the analog interface.

The receive path has to be stimulated with a sine wave applied to the digital input, or generated by one of the internal tone generators. By closing an internal or external (via the SLIC) loop to the transmit path, the outgoing signal is compared with a programmable offset.

(For further information, an application-note describing the calculation of the offset value and the sensitivity, is available)

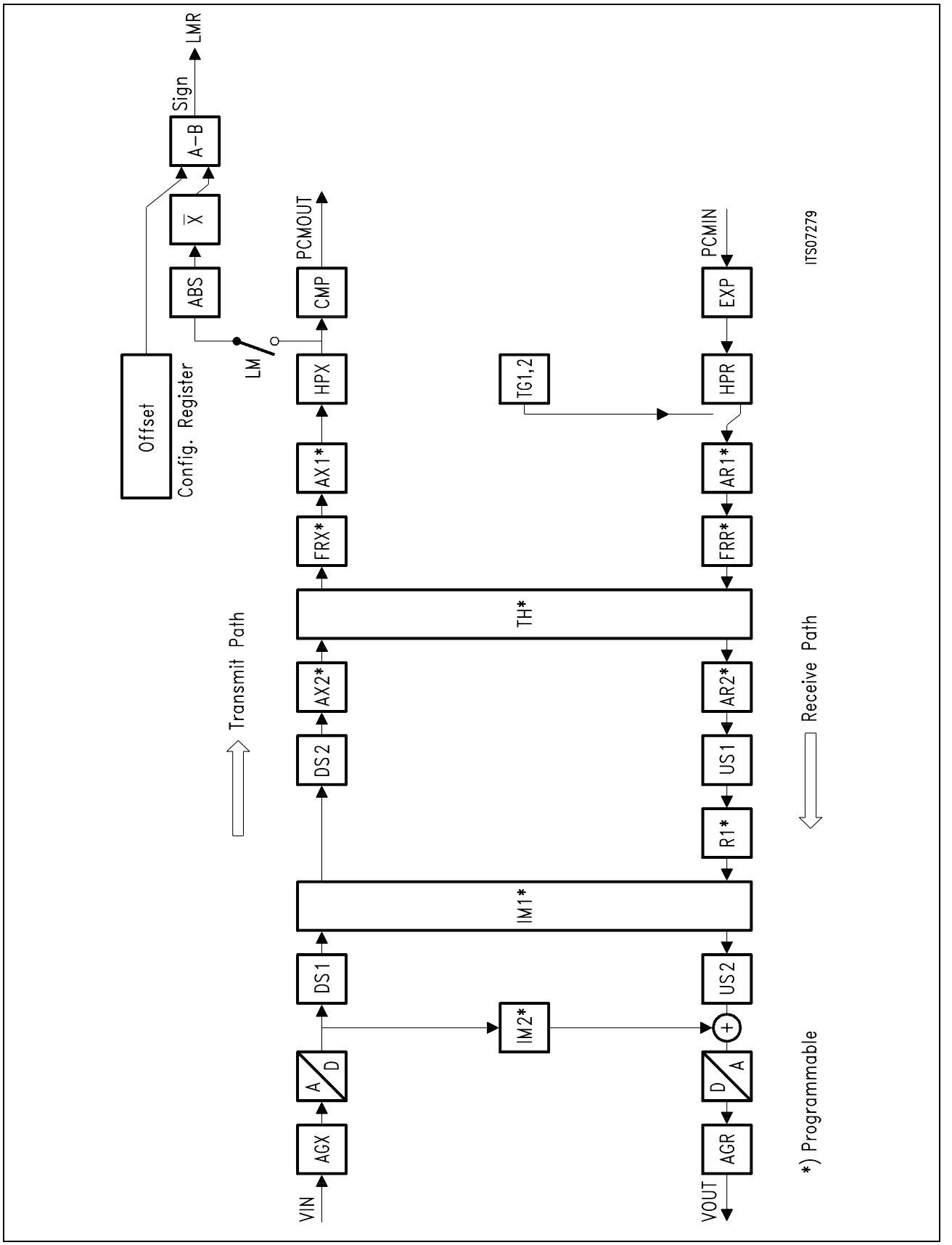

LMR
Sign
A–B
X̄
ABS
PCMOUT
CMP
PCMIN
EXP
ITS07279
Offset
Config. Register
LM
HPX
TG1,2
HPR
AX1*
AR1*
FRX*
FRR*
TH*
Transmit Path
AX2*
AR2*
Receive Path
DS2
US1
R1*
IM1*
DS1
US2
IM2*
A/D
D/A
AGX
AGR
VIN
VOUT
*) Programmable

Figure 32

7.2 Programming the SICOFI®-4-µC Tone Generators

Two independent Tone Generators are available per channel. Switching on/off the Tone Generators is done by a SOP-Command for CR1-register. The frequencies are programmed via a COP-Command, followed by the appropriate byte-sequence.

When one or both tone-generators are switched on, the voice signal is switched off, if V+T=0 (CR2) for the selected voice channel. To make the generated signal sufficient for DTMF, a programmable bandpass-filter is included. The default frequency for both tone generators is 1000 Hz. The QSICOS-program contains a program for generating coefficients for variable frequencies.

Byte sequences for programming both the tone generators and the bandpass-filters:

Table 2

Frequency	Command	Byte 1	Byte 2	Byte 3	Byte 4
697 Hz	0C/0D [1)]	0A	33	5A	2C
800 Hz	0C/0D [1)]	12	D6	5A	C0
950 Hz	0C/0D [1)]	1C	F0	5C	C0
1008 Hz	0C/0D [1)]	1A	AE	57	70
2000 Hz	0C/0D [1)]	00	80	50	09

[1)] 0C is used for programming Tone Generator 1, in channel 1
0D is used for programming Tone Generator 2, in channel 1

The resulting signal amplitude can be set by transmitting the AR1 and AR2 filters. By switching a ‘digital loop’ the generated sine-wave signal can be fed to the transmit path.

8 Proposed Test Circuit

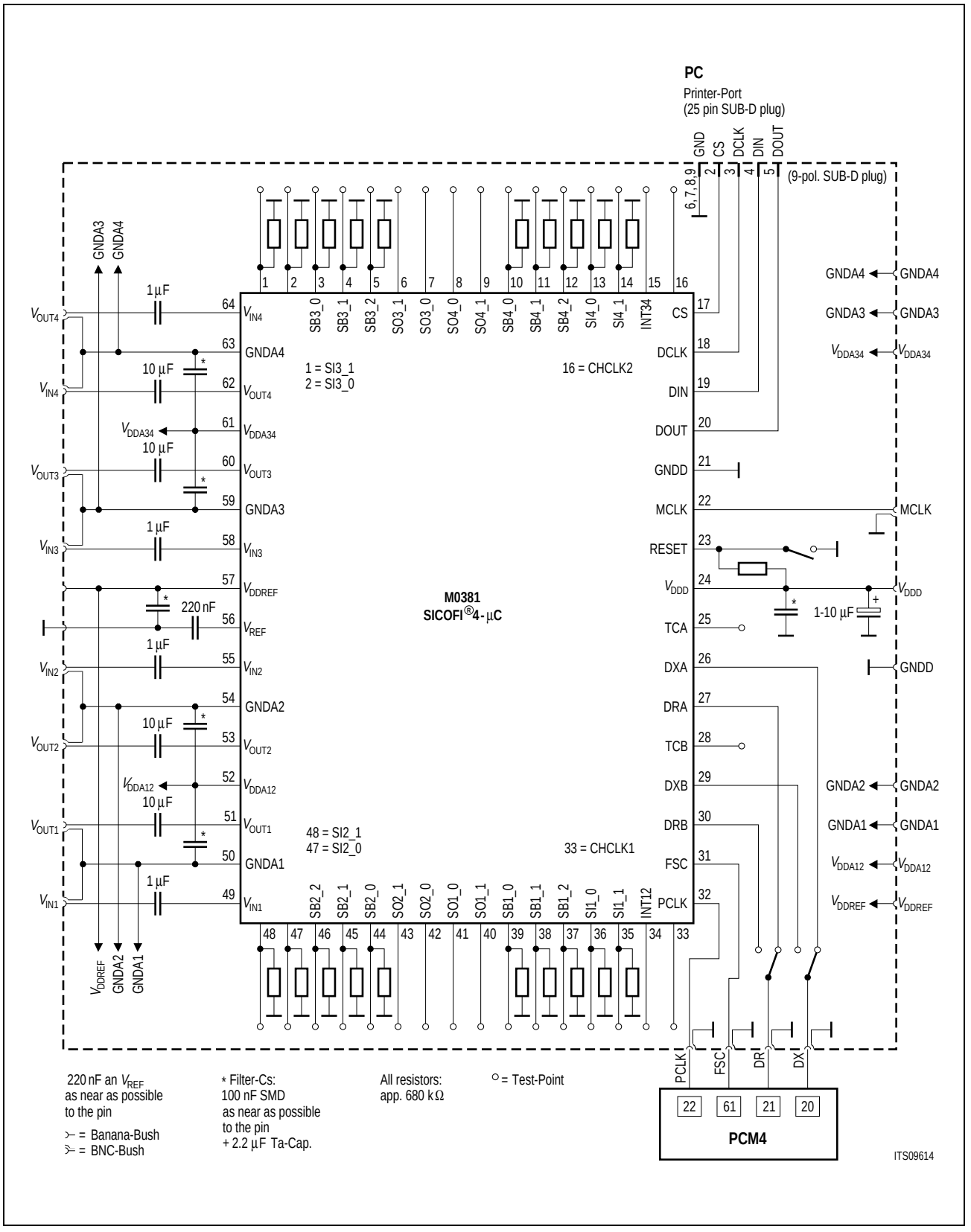


Figure 33

9 Guidelines for Board-Design

9.1 Board Layout Recommendation

Keep in mind that inside the SICOFI-4-µC all the different V_{DD}-supplies are connected via the substrate of the chip, and the areas connected to different grounds are separated on chip.

a) Separate all digital supply lines from analog supply lines as much as possible.
b) Use a separate GND-connection for the capacitor which is filtering the reference voltage (220 nF ceramic-capacitor at V_{REF}).
c) Don't use a common ground-plane under the SICOFI-4-µC.
d) Use a large ground-plane (distant from the SICOFI-4-µC) and use three single ground lines for connecting the SICOFI-4-µC: one common analog ground, one digital ground, and a third for the 220 nF capacitor connected to V_{REF}.

9.2 Filter Capacitors

a) To achieve a good filtering for the high frequency band, place SMD ceramic-capacitors with 100 nF from V_{DDA12}, V_{DDA32} and V_{DDREF} to GNDA.
b) One 100 nF SMD ceramic-capacitor is needed to filter the digital supply (V_{DDD} to GNDD).
c) Place all filter capacitors as close as possible to the SICOFI-4-µC (most important!!!).
d) Use one central Tantalum-capacitor with about 1 µF to 10 µF to block V_{DD} to GND.

9.3 Example of a PEB 2466-board

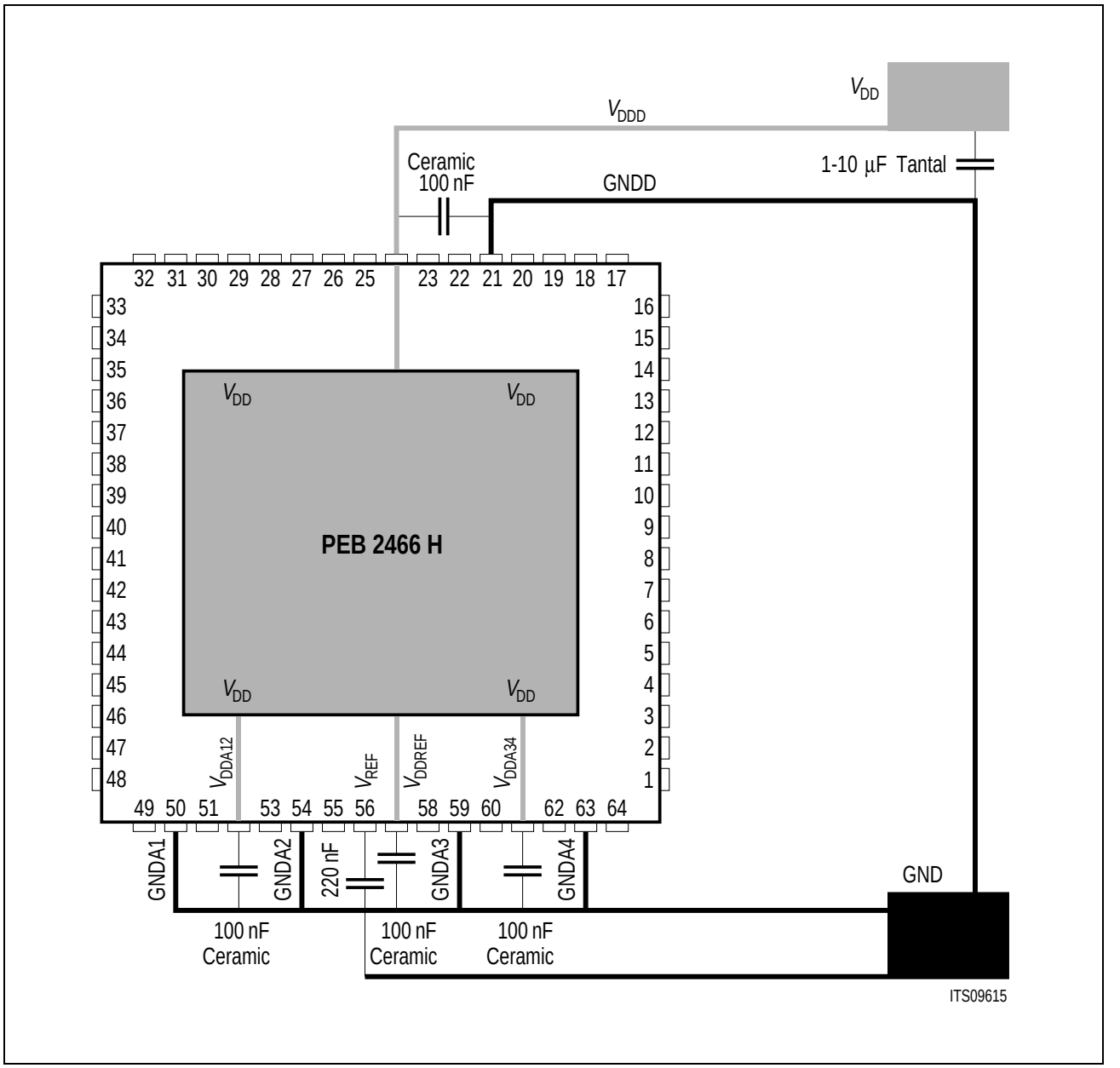


Figure 34