



PEEL™ 22LV10AZ-25 CMOS Programmable Electrically Erasable Logic Device

Features

Low Voltage, Ultra Low Power Operation

- Vcc = 2.7 to 3.6 V
- Icc = 5 µA (typical) at standby
- Icc = 1.5 mA (typical) at 1 MHz
- Meets JEDEC LV Interface Spec (JESD8-A)
- 5 Volt tolerant inputs and I/O's

CMOS Electrically Erasable Technology

- Superior factory testing
- Reprogrammable in plastic package
- Reduces retrofit and development costs

Application Versatility

- Replaces random logic
- Super set of standard PLDs
- Pin and JEDEC compatible with 22V10
- Ideal for battery powered systems
- Replaces expensive oscillators

Architectural Flexibility

- Enhanced architecture fits in more logic
- 133 product terms x 44 input AND array
- 12 inputs and 10 I/O pins
- 12 possible macrocell configurations
- Asynchronous clear, synchronous preset
- Independent output enables
- Programmable clock; pin 1 or p-term
- Programmable clock polarity
- 24 Pin DIP/SOIC/TSSOP and 28 Pin PLCC
- Schmitt triggers on clock and data inputs

Schmitt Trigger Inputs

- Eliminates external Schmitt trigger devices
- Ideal for encoder designs

General Description

The PEEL™22LV10AZ is a Programmable Electrically Erasable Logic (PEEL™) SPLD (Simple Programmable Logic Device) that operates over the supply voltage range of 2.7V-3.6V and features ultra-low, automatic “zero” power-down operation. The PEEL™22LV10AZ is logically and functionally similar to Anachip’s 5V PEEL™22CV10A+ and PEEL™22CV10AZ. The “zero power” (50 µA max. Icc) power-down mode makes the PEEL™22LV10AZ ideal for a broad range of battery-powered portable equipment applications, from hand-held meters to PCMCIA modems. EE-reprogrammability provides both the convenience of fast reprogramming for product development and quick product personalization in manufacturing, including Engineering Change Orders.

The differences between the PEEL™22LV10AZ and PEEL™22CV10A include the addition of programmable clock polarity, p-term clock, and Schmitt trigger input buffers on all inputs, including the clock. Schmitt trigger inputs allow direct input of slow signals such as biomedical and sine waves or clocks. Like the PEEL™22CV10, the PEEL™22LV10AZ is a pin and JEDEC compatible, logical superset of the industry standard PAL22V10 SPLD (Figure 26). The PEEL™22LV10AZ provides additional architectural features that allow more logic to be incorporated into the design. The PEEL™22LV10AZ architecture allows it to replace over twenty standard 24-pin DIP, SOIC, TSSOP and PLCC packages.

Figure 26 Pin Configuration

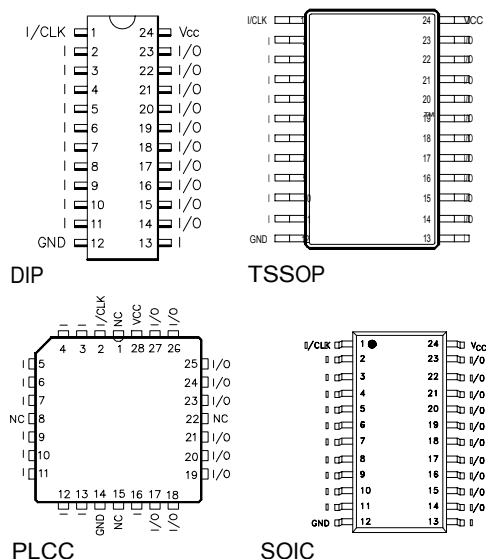
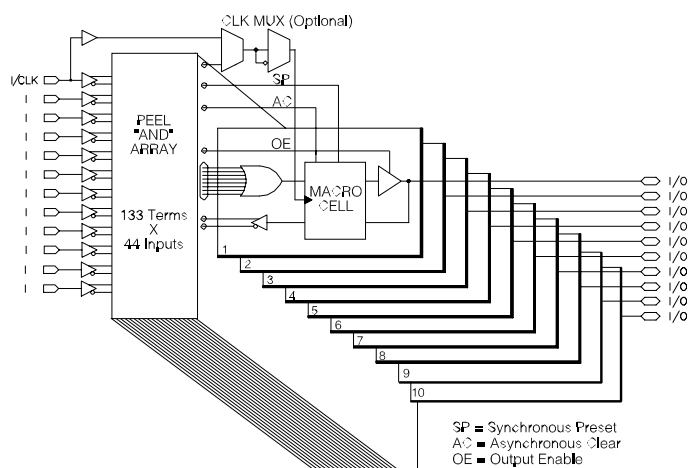


Figure 26 Block Diagram





Function Description

The PEEL™22LV10AZ implements logic functions as sum-of-products expressions in a programmable-AND/fixed-OR logic array. User-defined functions are created by programming the connections of input signals into the array. User-configurable output structures in the form of I/O macrocells further increase logic flexibility.

Architecture Overview

The PEEL™22LV10AZ architecture is illustrated in the block diagram of Figure 26. Twelve dedicated inputs and 10 I/Os provide up to 22 inputs and 10 outputs for creation of logic functions. At the core of the device is a programmable electrically-erasable AND array that drives a fixed OR array. With this structure, the PEEL™22LV10AZ can implement up to 10 sum-of-products logic expressions.

Associated with each of the ten OR functions is an I/O macrocell that can be independently programmed to one of 12 different configurations, including the four standard 22V10 modes. The programmable macrocells allow each I/O to be used to create sequential or combinatorial logic functions of active-high or active-low polarity, while providing three different feedback paths into the AND array.

AND/OR Logic Array

The programmable AND array of the PEEL™22LV10AZ (shown in Figure 3) is formed by input lines intersecting product terms. The input lines and product terms are used as follows:

44 Input Lines:

- 24 input lines carry the true and complement of the signals applied to the 12 input pins
- 20 additional lines carry the true and complement values of feedback or input signals from the 10 I/Os

133 Product Terms:

- 120 product terms (arranged in 2 groups of 8, 10, 12, 14, and 16) are used to form sum of product functions
- 10 output enable terms (one for each I/O)
- 1 global synchronous preset term
- 1 global asynchronous clear term
- 1 programmable clock term

At each input-line/product-term intersection, there is an EEPROM memory cell that determines whether or not there is a logical connection at that intersection. Each product term is essentially a 44-input AND gate. A product term that is connected to both the true and complement of an input signal will always be FALSE and thus will not affect the OR function that it drives. When all the connections on a product term are opened, a “don’t care” state exists and that term will always be TRUE. When programming the PEEL™22LV10AZ, the device programmer first performs a bulk erase to remove the previous pattern. The erase cycle opens every logical connection in the array. The device is configured to perform the user-defined function by programming selected connections in the AND array. (Note that

PEEL™ device programmers automatically program all of the connections on unused product terms so that they will have no effect on the output function).

Programmable I/O Macrocell

The unique twelve-configuration output macrocell provides complete control over the architecture of each output. The ability to configure each output independently lets you to tailor the configuration of the PEEL™22LV10AZ to the precise requirements of your design.

Macrocell Architecture

Each I/O macrocell, as shown in Figure 27, consists of a D-type flip-flop and two signal-select multiplexers. The configuration of each macrocell is determined by the four EEPROM bits controlling these multiplexers. These bits determine output polarity, output type (registered or non-registered) and input-feedback path (bidirectional I/O, combinatorial feedback). Refer to Table 1 for details.

Equivalent circuits for the twelve macrocell configurations are illustrated in Figure 1. In addition to emulating the four PAL-type output structures (configurations 3, 4, 9, and 10), the macrocell provides eight additional configurations. When creating a PEEL™ device design, the desired macrocell configuration is generally specified explicitly in the design file. When the design is assembled or compiled, the macrocell configuration bits are defined in the last lines of the JEDEC programming file.

Output Type

The signal from the OR array can be fed directly to the output pin (combinatorial function) or latched in the D-type flip-flop (registered function). The D-type flip-flop latches data on the rising edge of the clock and is controlled by the global preset and clear terms. When the synchronous preset term is satisfied, the Q output of the register is set HIGH at the next rising edge of the clock input. Satisfying the asynchronous clear sets Q LOW, regardless of the clock state. If both terms are satisfied simultaneously, the clear will override the preset.

Output Polarity

Each macrocell can be configured to implement active-high or active-low logic. Programmable polarity eliminates the need for external inverters.

Output Enable

The output of each I/O macrocell can be enabled or disabled under the control of its associated programmable output enable product term. When the logical conditions programmed on the output enable term are satisfied, the output signal is propagated to the I/O pin. Otherwise, the output buffer is switched into the high-impedance state.

Under the control of the output enable term, the I/O pin can function as a dedicated input, a dedicated output, or a bi-directional I/O. Opening every connection on the output enable term will permanently enable the output buffer and yield a dedicated output. Conversely, if every connection is intact, the enable term will



always be logically false and the I/O will function as a dedicated input.

Input/Feedback Select

The PEEL™22LV10AZ macrocell also provides control over the feedback path. The input/feedback signal associated with each I/O macrocell can be obtained from three different locations; from the I/O input pin, from the Q output of the flip-flop (registered feedback), or directly from the OR gate (combinatorial feedback).

Bi-directional I/O

The input/feedback signal is taken from the I/O pin when using the pin as a dedicated input or as a bi-directional I/O. (Note that it is possible to create a registered output function with a bi-directional I/O, refer to Figure 27).

Combinatorial Feedback

The signal-select multiplexer gives the macrocell the ability to feedback the output of the OR gate, bypassing the output buffer, regardless of whether the output function is registered or combinatorial. This feature allows the creation of asynchronous latches, even when the output must be disabled. (Refer to configurations 5, 6, 7, and 8 in Figure 1.)

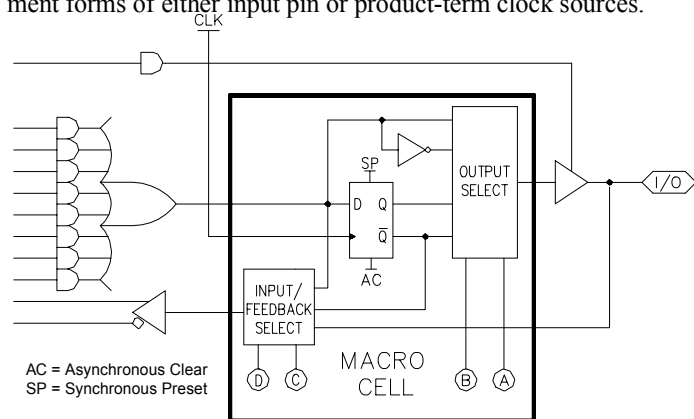
Registered Feedback

Feedback also can be taken from the register, regardless of whether the output function is programmed to be combinatorial or registered. When implementing a combinatorial output function, registered feedback allows for the internal latching of states without giving up the use of the external output.

Figure 27 Block Diagram of the PEEL™22LV10AZ I/O Macrocell

Programmable Clock Options

A unique feature of the PEEL™22LV10AZ is a programmable clock multiplexer that allows the user to select true or complement forms of either input pin or product-term clock sources.



Operates in both 3 Volt and 3.3 Volt Systems

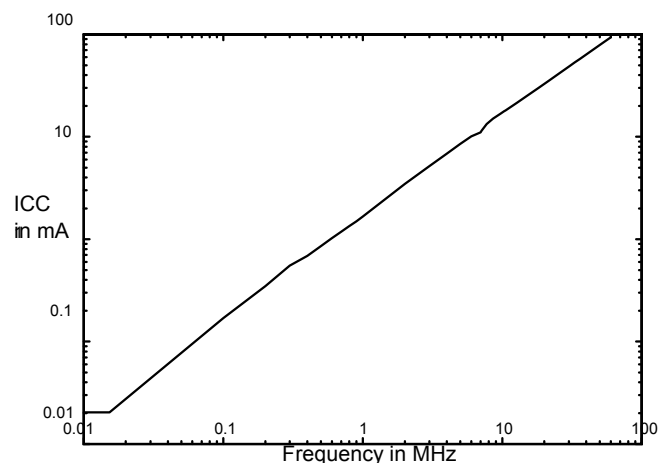
The PEEL™22LV10AZ is designed to operate with a VCC range of 2.7 to 3.6 Volts D.C. This allows operation in both 3 Volt ±10% (battery operated) and 3.3 Volt ±10% (power supply operated) systems. The propagation delay tPD is 5 ns slower at the lower voltage, but this is typically not an issue in battery-operated systems (see “A.C. Electrical Characteristics” on page 64).

Zero Power Feature

The CMOS PEEL™22LV10AZ features “Zero-Power” standby operation for ultra-low power consumption. With the “Zero-Power” feature, transition-detection circuitry monitors the inputs, I/Os (including CLK) and feedbacks. If these signals do not change for a period of time greater than approximately two tPD’s, the outputs are latched in their current state and the device automatically powers down. When the next signal transition is detected, the device will “wake up” for active operation until the signals stop switching long enough to trigger the next power-down. (Note that the tPD is approximately 5 ns. slower on the first transition from sleep mode.)

As a result of the “Zero-Power” feature, significant power savings can be realized for combinatorial or sequential operations when the inputs or clock change at a modest rate. See Figure 28. When the PEEL™22LV10AZ is powered up, a built-in feature holds the outputs in tri-state until Vcc reaches 2.2V. This prevents output transitions during power-up.

Figure 28 Typical ICC vs. Input Clock Frequency for the 22LV10AZ



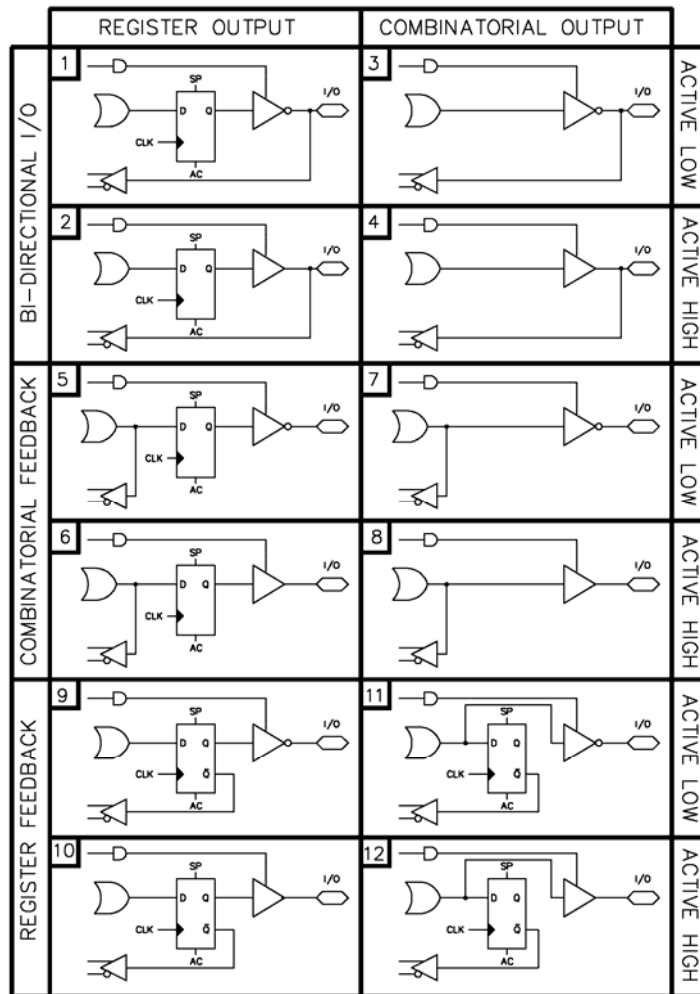


Figure 1 Equivalent Circuits for the Twelve Configurations of the PEEL™22LV10AZ+ I/O Macrocell

Configuration					Input/Feedback Select	Output Select	
#	A	B	C	D			
1	0	0	1	0	Bi-directional I/O	Register	Active Low
2	1	0	1	0			Active High
3	0	1	0	0		Combinatorial	Active Low
4	1	1	0	0			Active High
5	0	0	1	1	Combinatorial Feedback	Register	Active Low
6	1	0	1	1			Active High
7	0	1	1	1		Combinatorial	Active Low
8	1	1	1	1			Active High
9	0	0	0	0	Register Feedback	Register	Active Low
10	1	0	0	0			Active High
11	0	1	1	0		Combinatorial	Active Low
12	1	1	1	0			Active High



Schmitt Trigger Inputs

The PEEL™22LV10AZ has Schmitt trigger input buffers on all inputs, including the clock. Schmitt trigger inputs allow direct input of slow signals such as biomedical and sine waves or clocks. They are also useful in cleaning up noisy signals. This makes the PEEL™22LV10AZ especially desirable in portable applications where the environment is less predictable.

Design Security

The PEEL™22LV10AZ provides a special EEPROM security bit that prevents unauthorized reading or copying of designs programmed into the device. The security bit is set by the PLD programmer, either at the conclusion of the programming cycle or as a separate step, after the device has been programmed. Once the security bit is set it is impossible to verify (read) or program the PEEL™ until the entire device has first been erased with the bulk-erase function.

Signature Word

The signature word feature allows a 64-bit code to be programmed into the PEEL™22LV10AZ if the PEEL™22LV10AZ+ software option is used. The code can be read back even after the security bit has been set. The signature word can be used to identify the pattern programmed into the device or to record the design revision, etc.

Programming Support

Anachip's JEDEC file translator allows easy conversion of existing 24 pin PLD designs to the PEEL™22LV10AZ, without the need for redesign. Anachip also offers (for free) its proprietary WinPLACE software, an easy-to-use entry level PC-based software development system.

Programming support includes all the popular third party programmers such as BP Microsystems, System General, Logical Devices, and numerous others.



This device has been designed and tested for the specified operating ranges. Improper operation outside of these levels is not guaranteed. Exposure to absolute maximum ratings may cause permanent damage.

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Rating	Unit
VCC	Supply Voltage	Relative to Ground	-0.5 to + 6.0	V
VI, VO	Voltage Applied to Any Pin ²	Relative to Ground ¹	-0.5 to 5.5	V
IO	Output Current	Per Pin (IOL, IOH)	±25	mA
TST	Storage Temperature		-65 to +150	°C
TLT	Lead Temperature	Soldering 10 Seconds	+300	°C

Operating Range

Symbol	Parameter	Conditions	Min	Max	Unit
Vcc	Supply Voltage ³	Commercial	2.7	3.6	V
TA	Ambient Temperature	Commercial	0	+70	°C
TRVCC	VCC Rise Time	See Note 4.		250	ms

D.C. Electrical Characteristics Over the operating range (Unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Unit
VOH	Output HIGH Voltage - TTL	VCC=Min, IOH=-2.0mA	VCC-0.5		V
VOHC	Output HIGH Voltage - CMOS	VCC=Min, IOH=-10µA	VCC-0.3		V
VOL	Output LOW Voltage - TTL	VCC=Min, IOL=8.0mA		0.4	V
VOLC	Output LOW Voltage - CMOS	VCC=Min, IOL=10µA		0.15	V
VIH	Input HIGH Level	VCC=3.3V	2.0	5.5	V
VIL	Input LOW Level	VCC=3.3V	-0.3	0.8	V
VH	Input Voltage Hysteresis		0.2		V
IIN	Input and I/O Leakage Current	VCC=Max, GND≤VIN≤VCC, I/O=High Z		±10	µA
		VCC=Max, GND≤VIN≤5.5V, I/O=High Z		1	mA
ISC ¹⁰	Output Short Circuit Current	VCC=Max, VO=0.5V, TA=25°C	-30	-135	mA
ICCS	VCC Current, Standby	VIN=0V or VCC, All Outputs disabled ⁵	5(typ)	25	µA
ICC ¹¹	VCC Current, f=1MHz	VIN=0V or VCC, All Outputs disabled ⁵	1.5(typ)	3	mA
CIN ⁸	Input Capacitance	TA=25°C, VCC=Max		6	pF
COUT ⁸	Output Capacitance	@f=1MHz		12	pF

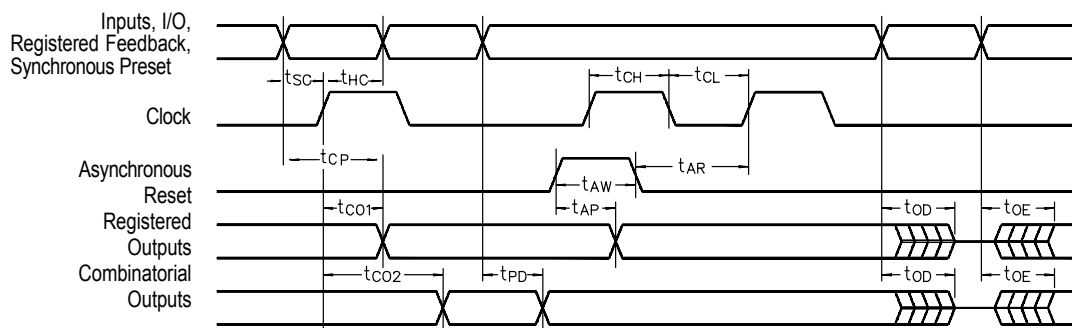


A.C. Electrical Characteristics

Over the operating range ⁹

Symbol	Parameter	-25				Units
		3V ±10%		3.3V ±10%		
		Min	Max	Min	Max	
tPD	Input ⁶ to non-registered output in continuous mode ¹³		30		25	ns
tOE	Input ⁶ to output enable ⁷		30		25	ns
tOD	Input ⁶ to output disable ⁷		30		25	ns
tCO1	Clock to Output		20		15	ns
tCO2	Clock to comb. output delay via internal registered feedback		40		35	ns
tCF	Clock to Feedback		14		9	ns
tSC	Input ⁶ or feedback setup to clock	20		15		ns
tHC	Input ⁶ hold after clock	0		0		ns
tCL, tCH	Clock low time, clock high time ⁹	20		13		ns
tCP	Min clock period Ext (tSC + tCO1)	40		30		ns
fMAX1	Internal feedback (1/tSC+tCF) ¹²	29.4		41.6		MHz
fMAX2	External Feedback (1/tCP) ¹²	25		33.3		MHz
fMAX3	No Feedback (1/tCL+tCH) ¹²	25		38.4		MHz
tAW	Asynchronous Reset Pulse Width	30		25		ns
tAP	Input to Asynchronous Reset		30		25	ns
tAR	Asynchronous Reset recovery time		30		25	ns
tRESET	Power-on reset time for registers in clear state ¹⁴		5		5	µs

Switching Waveforms



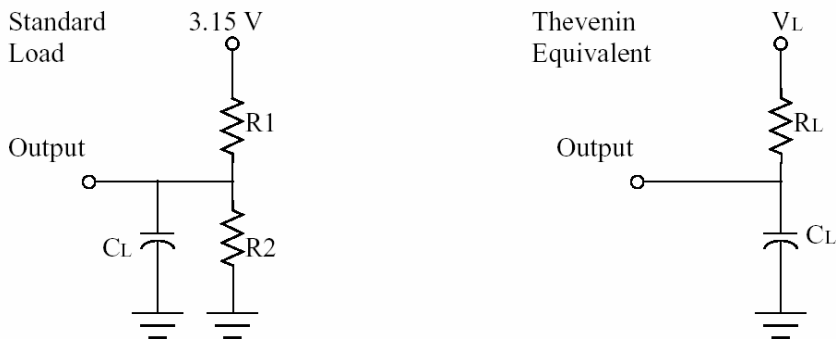
Notes:

1. Minimum DC input is -0.5V, however, inputs may undershoot to -2.0V for periods less than 20 ns.
2. VI and VO are not specified for program/verify operation.
3. The Supply Voltage range of 2.7 to 3.6V was chosen to allow this part to be used in both 3V ±10% and 3.3V ±10% applications.
4. Test Points for Clock and VCC in tr and tr are referenced at the 10% and 90% levels.
5. I/O pins are 0V and VCC.
6. "Input" refers to an input pin signal.
7. tOE is measured from input transition to VREF±0.1V, TOD is measured from input transition to VOH-0.1V or VOL+0.1V; VREF=VL.
8. Capacitances are tested on a sample basis.

9. Test conditions assume: signal transition times of 3ns or less from the 10% and 90% points, timing reference levels of 1.5V (Unless otherwise specified).
10. Test one output at a time for a duration of less than 1 second.
11. ICC for a typical application: This parameter is tested with the device programmed as a 10-bit Counter.
12. Parameters are not 100% tested. Specifications are based on initial characterization and are tested after any design process modification that might affect operational frequency.
13. tPD, tOE, tOD, tCO, tSC, and tAP are approximately 5 ns. slower on the first transaction from sleep mode.
14. Input at GND.



PEEL™ Device and Array Test Loads

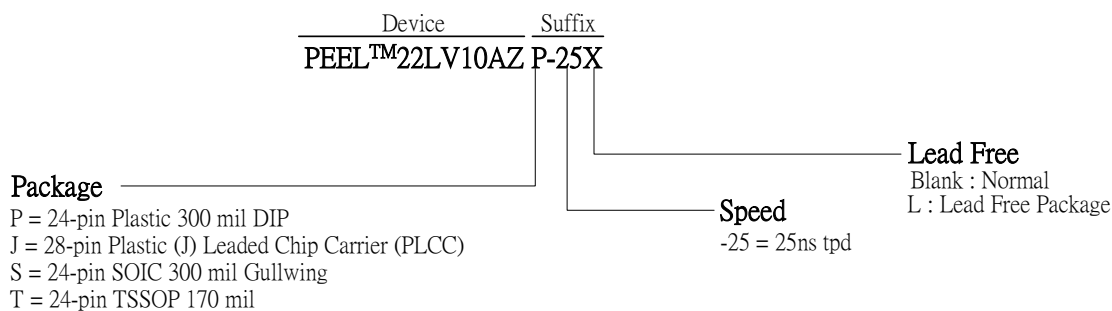


Technology	R1	R2	RL	VL	CL
CMOS	274kΩ	257kΩ	110kΩ	1.30V	33 pF
TTL	315Ω	548Ω	200Ω	2.00V	33 pF

Ordering Information

Part Number	Speed	Temperature	Package
PEEL22LV10AZP-25 (L)	25ns	Commercial	24-pin Plastic DIP
PEEL22LV10AZJ-25 (L)	25ns	Commercial	28-pin PLCC
PEEL22LV10AZS-25 (L)	25ns	Commercial	24-pin SOIC
PEEL22LV10AZT-25 (L)	25ns	Commercial	24-pin TSSOP

Part Number





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