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Kind regards,

Team Nexperia

PEMB2; PUMB2

PNP/PNP resistor-equipped transistors;
R1 = 47 k Ω , R2 = 47 k Ω

Rev. 3 — 17 November 2011

Product data sheet

1. Product profile

1.1 General description

PNP/PNP double Resistor-Equipped Transistors (RET) in Surface-Mounted Device (SMD) plastic packages.

Table 1. Product overview

Type number	Package		NPN/PNP complement	NPN/NPN complement	Package configuration
	NXP	JEITA			
PEMB2	SOT666	-	PEMD12	PEMH2	ultra small and flat lead
PUMB2	SOT363	SC-88	PUMD12	PUMH2	very small

1.2 Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- AEC-Q101 qualified

1.3 Applications

- Low current peripheral driver
- Control of IC inputs
- Replaces general-purpose transistors in digital applications

1.4 Quick reference data

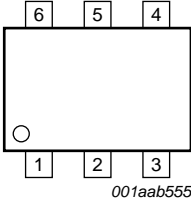
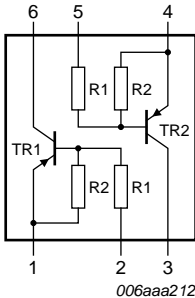
Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
V _{CEO}	collector-emitter voltage	open base	-	-	-50	V
I _O	output current		-	-	-100	mA
R1	bias resistor 1 (input)		33	47	61	k Ω
R2/R1	bias resistor ratio		0.8	1	1.2	



2. Pinning information

Table 3. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	GND (emitter) TR1		
2	input (base) TR1		
3	output (collector) TR2		
4	GND (emitter) TR2		
5	input (base) TR2		
6	output (collector) TR1		

3. Ordering information

Table 4. Ordering information

Type number	Package		Version
	Name	Description	
PEMB2	-	plastic surface-mounted package; 6 leads	SOT666
PUMB2	SC-88	plastic surface-mounted package; 6 leads	SOT363

4. Marking

Table 5. Marking codes

Type number	Marking code ^[1]
PEMB2	B2
PUMB2	B*2

[1] * = placeholder for manufacturing site code

5. Limiting values

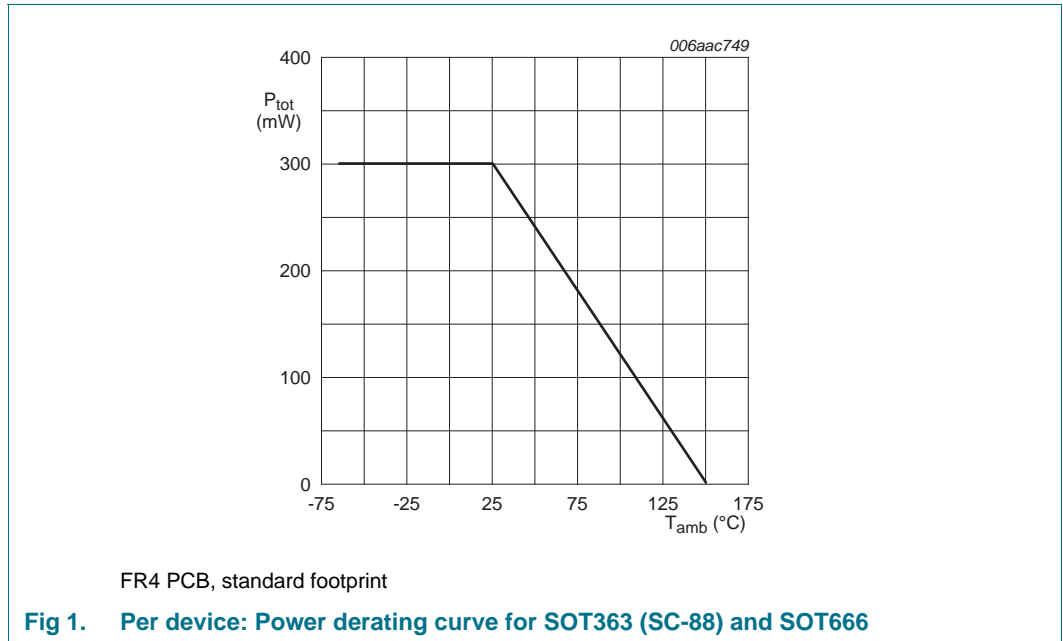
Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
Per transistor						
V_{CBO}	collector-base voltage	open emitter	-	-50	V	
V_{CEO}	collector-emitter voltage	open base	-	-50	V	
V_{EBO}	emitter-base voltage	open collector	-	-10	V	
V_I	input voltage					
	positive		-	+10	V	
	negative		-	-40	V	
I_O	output current		-	-100	mA	
I_{CM}	peak collector current	single pulse; $t_p \leq 1$ ms	-	-100	mA	
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C				
	PEMB2 (SOT666)		[1][2]	-	200	mW
	PUMB2 (SOT363)		[1]	-	200	mW
Per device						
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C				
	PEMB2 (SOT666)		[1][2]	-	300	mW
	PUMB2 (SOT363)		[1]	-	300	mW
T_j	junction temperature		-	150	°C	
T_{amb}	ambient temperature		-65	+150	°C	
T_{stg}	storage temperature		-65	+150	°C	

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.



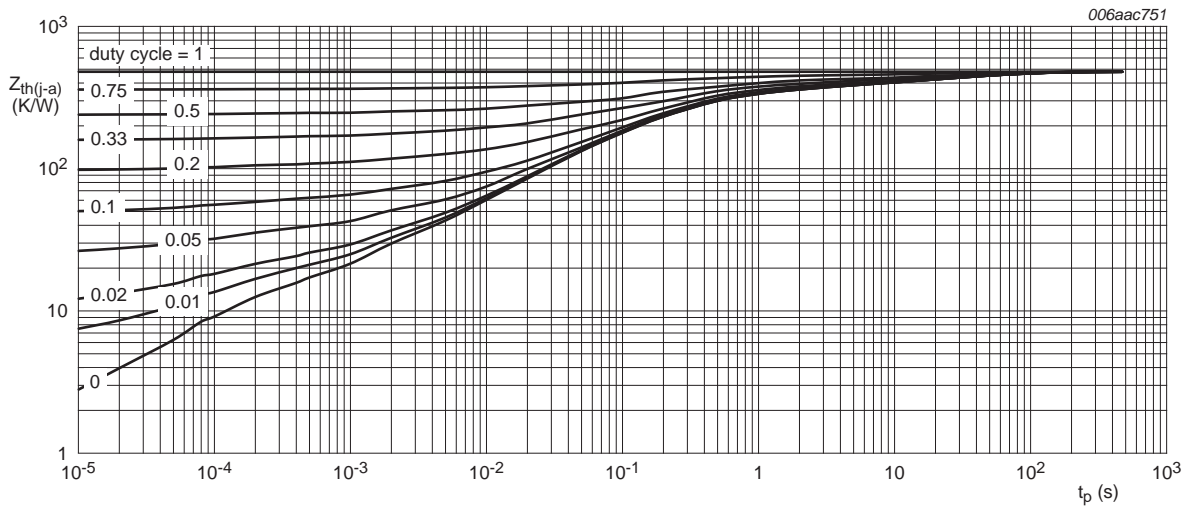
6. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air				
	PEMB2 (SOT666)		[1][2]	-	625	K/W
	PUMB2 (SOT363)		[1]	-	625	K/W
Per device						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air				
	PEMB2 (SOT666)		[1][2]	-	417	K/W
	PUMB2 (SOT363)		[1]	-	417	K/W

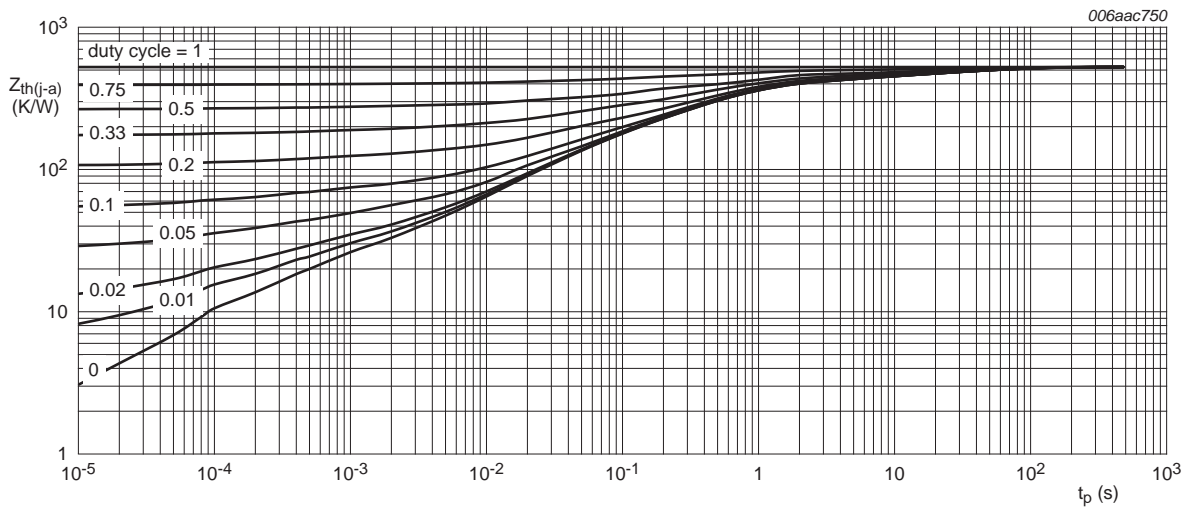
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.



FR4 PCB, standard footprint

Fig 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration for PEMB2 (SOT666); typical values



FR4 PCB, standard footprint

Fig 3. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration for PUMB2 (SOT363); typical values

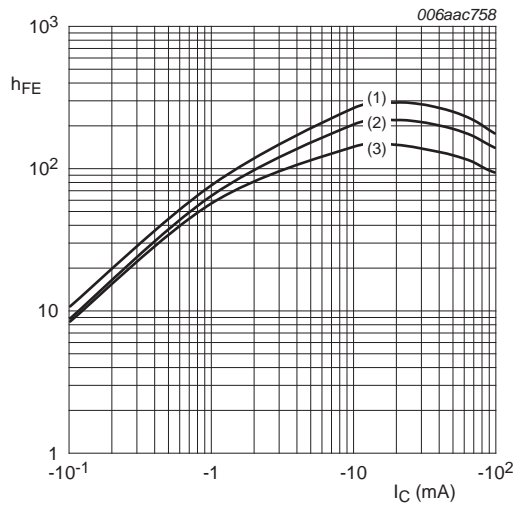
7. Characteristics

Table 8. Characteristics

$T_{amb} = 25\text{ °C}$ unless otherwise specified.

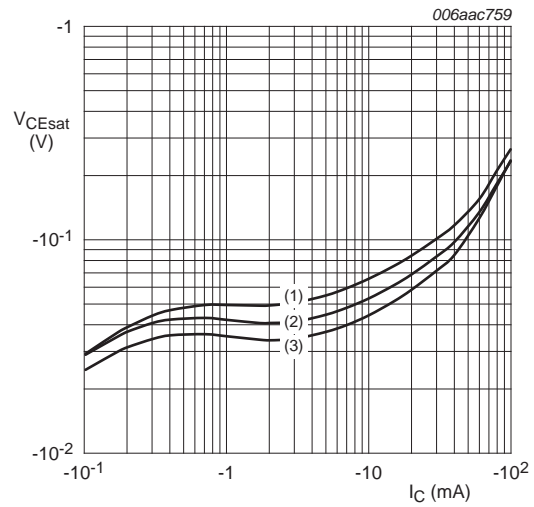
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Per transistor						
I_{CBO}	collector-base cut-off current	$V_{CB} = -50\text{ V}; I_E = 0\text{ A}$	-	-	-100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = -30\text{ V}; I_B = 0\text{ A}$	-	-	-1	μA
		$V_{CE} = -30\text{ V}; I_B = 0\text{ A}; T_j = 150\text{ °C}$	-	-	-5	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = -5\text{ V}; I_C = 0\text{ A}$	-	-	-90	μA
h_{FE}	DC current gain	$V_{CE} = -5\text{ V}; I_C = -5\text{ mA}$	80	-	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = -10\text{ mA}; I_B = -0.5\text{ mA}$	-	-	-150	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = -5\text{ V}; I_C = -100\text{ μA}$	-	-1.2	-0.8	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = -0.3\text{ V}; I_C = -2\text{ mA}$	-3	-1.6	-	V
R1	bias resistor 1 (input)		33	47	61	kΩ
R2/R1	bias resistor ratio		0.8	1	1.2	
C_c	collector capacitance	$V_{CB} = -10\text{ V}; I_E = i_e = 0\text{ A}; f = 1\text{ MHz}$	-	-	3	pF
f_T	transition frequency	$V_{CE} = -5\text{ V}; I_C = -10\text{ mA};$ [1] $f = 100\text{ MHz}$	-	180	-	MHz

[1] Characteristics of built-in transistor



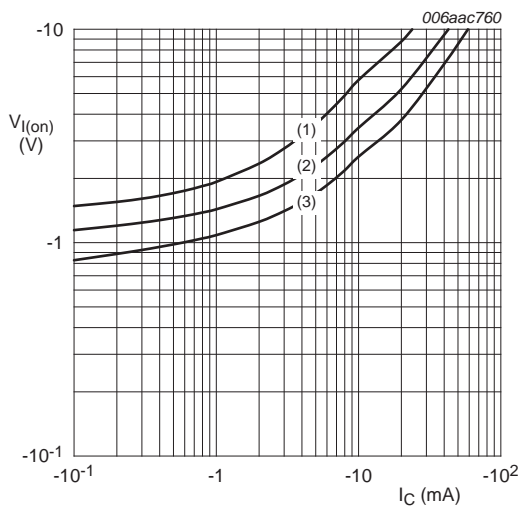
- $V_{CE} = -5\text{ V}$
- (1) $T_{amb} = 100\text{ °C}$
 - (2) $T_{amb} = 25\text{ °C}$
 - (3) $T_{amb} = -40\text{ °C}$

Fig 4. DC current gain as a function of collector current; typical values



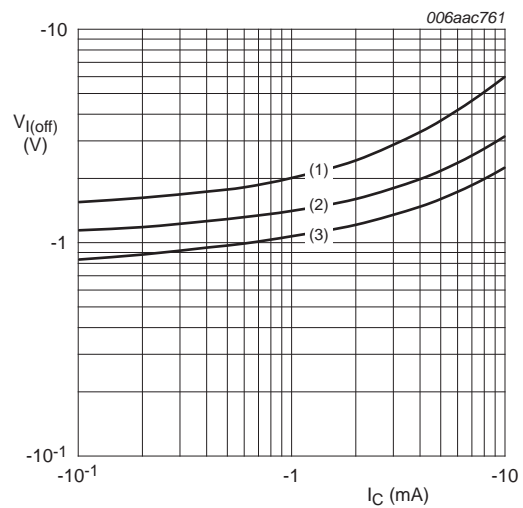
- $I_C/I_B = 20$
- (1) $T_{amb} = 100\text{ °C}$
 - (2) $T_{amb} = 25\text{ °C}$
 - (3) $T_{amb} = -40\text{ °C}$

Fig 5. Collector-emitter saturation voltage as a function of collector current; typical values



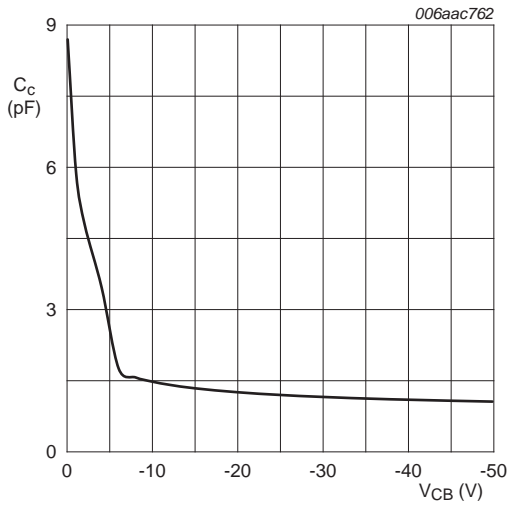
- $V_{CE} = -0.3\text{ V}$
- (1) $T_{amb} = -40\text{ °C}$
 - (2) $T_{amb} = 25\text{ °C}$
 - (3) $T_{amb} = 100\text{ °C}$

Fig 6. On-state input voltage as a function of collector current; typical values



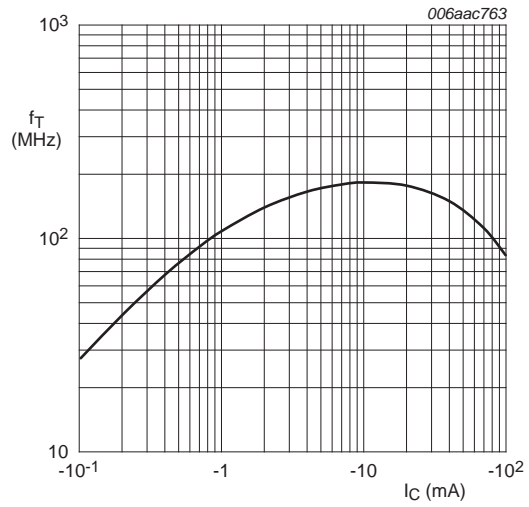
- $V_{CE} = -5\text{ V}$
- (1) $T_{amb} = -40\text{ °C}$
 - (2) $T_{amb} = 25\text{ °C}$
 - (3) $T_{amb} = 100\text{ °C}$

Fig 7. Off-state input voltage as a function of collector current; typical values



f = 1 MHz; T_{amb} = 25 °C

Fig 8. Collector capacitance as a function of collector-base voltage; typical values of built-in transistor



V_{CE} = -5 V; T_{amb} = 25 °C

Fig 9. Transition frequency as a function of collector current; typical values of built-in transistor

8. Test information

8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

9. Package outline

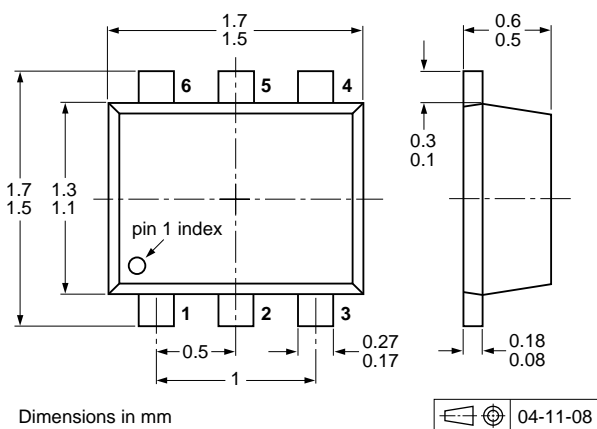


Fig 10. Package outline PEMB2 (SOT666)

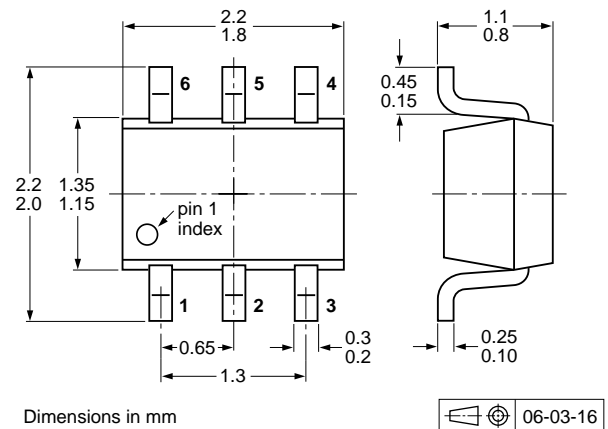


Fig 11. Package outline PUMB2 (SOT363)

10. Packing information

Table 9. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.^[1]

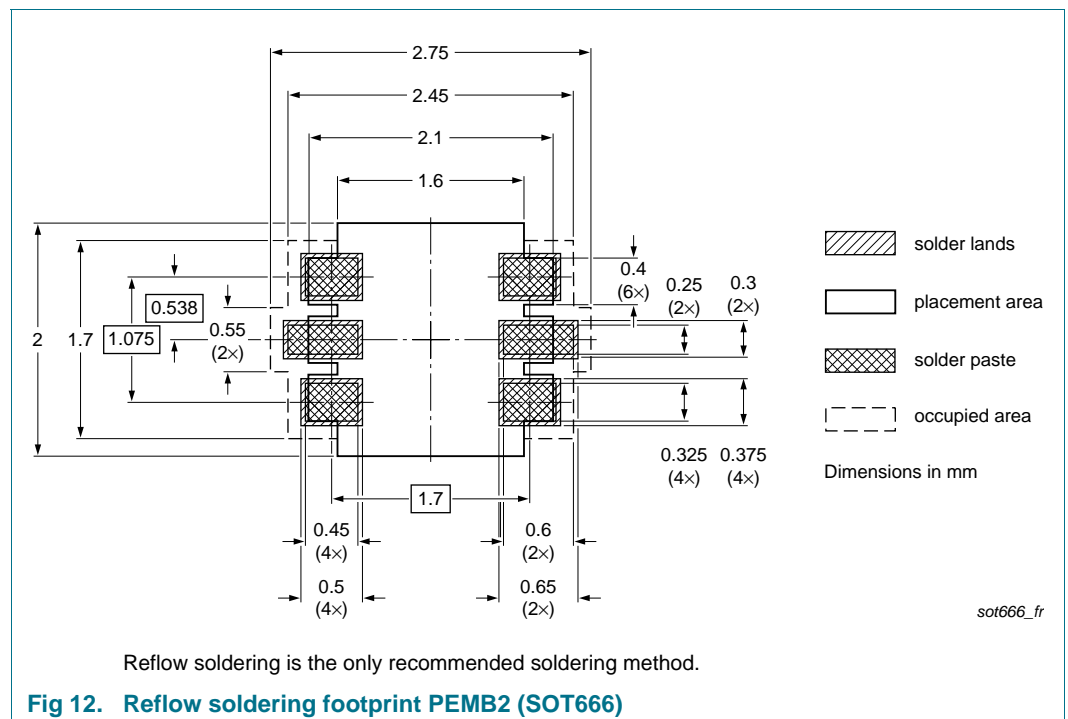
Type number	Package	Description	Packing quantity			
			3000	4000	8000	10000
PEMB2	SOT666	2 mm pitch, 8 mm tape and reel	-	-	-315	-
		4 mm pitch, 8 mm tape and reel	-	-115	-	-
PUMB2	SOT363	4 mm pitch, 8 mm tape and reel; T1 ^[2]	-115	-	-	-135
		4 mm pitch, 8 mm tape and reel; T2 ^[3]	-125	-	-	-165

[1] For further information and the availability of packing methods, see [Section 14](#).

[2] T1: normal taping

[3] T2: reverse taping

11. Soldering



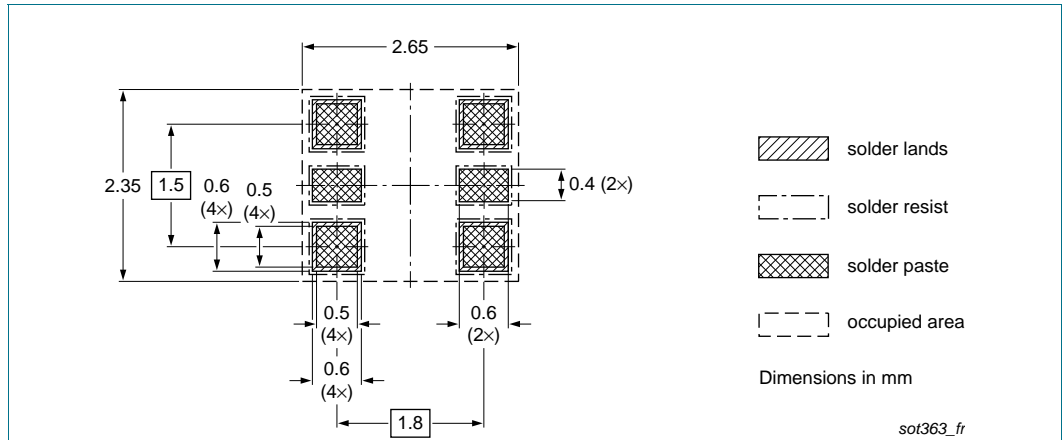


Fig 13. Reflow soldering footprint PUMB2 (SOT363)

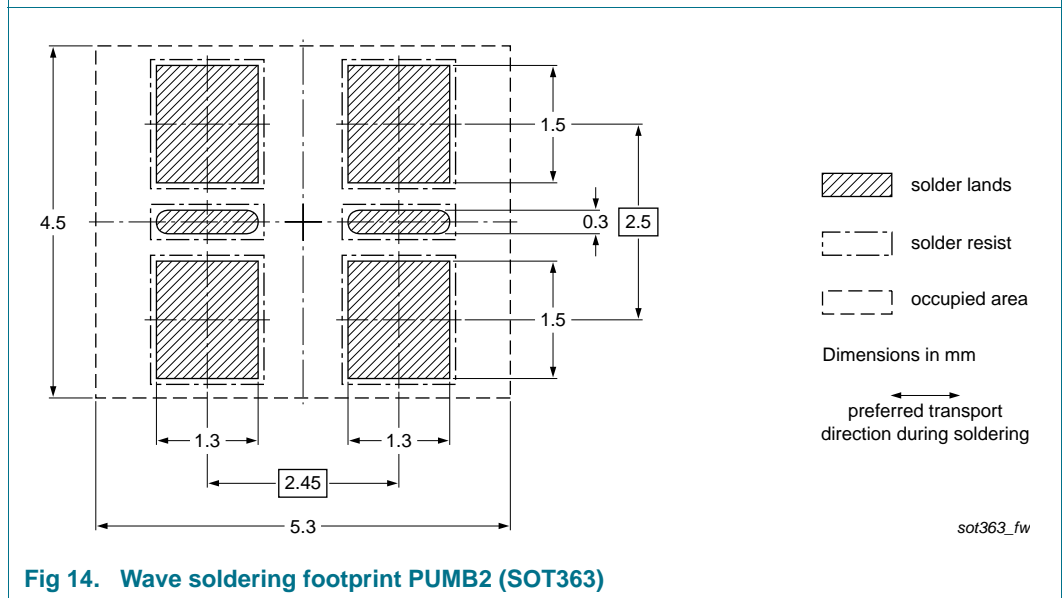


Fig 14. Wave soldering footprint PUMB2 (SOT363)

12. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PEMB2_PUMB2 v.3	20111117	Product data sheet	-	PEMB2_PUMB2 v.2
Modifications:	<ul style="list-style-type: none"> • The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Section 1 "Product profile": updated • Section 4 "Marking": updated • Figure 1 to 9: added • Section 5 "Limiting values": updated • Section 6 "Thermal characteristics": updated • Table 8 "Characteristics": $V_{i(on)}$ redefined to $V_{I(on)}$ on-state input voltage, $V_{i(off)}$ redefined to $V_{I(off)}$ off-state input voltage, I_{CEO} updated, f_T added • Section 8 "Test information": added • Section 9 "Package outline": superseded by minimized package outline drawing • Section 10 "Packing information": added • Section 11 "Soldering": added • Section 13 "Legal information": updated 			
PEMB2_PUMB2 v.2	20031015	Product data sheet	-	PUMB2 v.1 PEMB2 v.1
PEMB2 v.1	20010914	Product specification	-	-
PUMB2 v.1	19910803	Product specification	-	-

13. Legal information

13.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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