

DATA SHEET

PEMD12; PUMD12
NPN/PNP resistor-equipped
transistors; R1 = 47 k Ω , R2 = 47 k Ω

Product data sheet
Supersedes data of 2001 Nov 7

2003 Oct 08

NPN/PNP resistor-equipped transistors;
R1 = 47 kΩ, R2 = 47 kΩ

PEMD12; PUMD12

FEATURES

- Built-in bias resistors
- Simplified circuit design
- Reduction of component count
- Reduced pick and place costs.

APPLICATIONS

- Low current peripheral driver
- Replacement of general purpose transistors in digital applications
- Control of IC inputs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V _{CEO}	collector-emitter voltage	–	50	V
I _O	output current (DC)	–	100	mA
TR1	NPN	–	–	–
TR2	PNP	–	–	–
R1	bias resistor	47	–	kΩ
R2	bias resistor	47	–	kΩ

DESCRIPTION

NPN/PNP resistor-equipped transistors (see “Simplified outline, symbol and pinning” for package details).

PRODUCT OVERVIEW

TYPE NUMBER	PACKAGE		MARKING CODE	PNP/PNP COMPLEMENT	NPN/PNP COMPLEMENT
	PHILIPS	EIAJ			
PEMD12	SOT666		D2	PEMB2	PEMH2
PUMD12	SOT363	SC-88	D*1 ⁽¹⁾	PUMB2	PUMH2

Note

- * = p: Made in Hong Kong.
 * = t: Made in Malaysia.
 * = W: Made in China.

SIMPLIFIED OUTLINE, SYMBOL AND PINNING

TYPE NUMBER	SIMPLIFIED OUTLINE AND SYMBOL	PINNING	
		PIN	DESCRIPTION
PEMD12 PUMD12	<p>Top view</p> <p>MAM468</p>	1	emitter TR1
		2	base TR1
		3	collector TR2
		4	emitter TR2
		5	base TR2
		6	collector TR1

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ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PEMD12	–	plastic surface mounted package; 6 leads	SOT666
PUMD12	–	plastic surface mounted package; 6 leads	SOT363

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor; for the PNP transistor with negative polarity					
V _{CBO}	collector-base voltage	open emitter	–	50	V
V _{CEO}	collector-emitter voltage	open base	–	50	V
V _{EBO}	emitter-base voltage	open collector	–	10	V
V _I	input voltage TR1 positive negative		–	+40	V
			–	–10	V
V _I	input voltage TR2 positive negative		–	+10	V
			–	–40	V
I _O	output current (DC)		–	100	mA
I _{CM}	peak collector current		–	100	mA
P _{tot}	total power dissipation SOT363	T _{amb} ≤ 25 °C note 1	–	200	mW
	SOT666	notes 1 and 2	–	200	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	junction temperature		–	150	°C
T _{amb}	operating ambient temperature		–65	+150	°C
Per device					
P _{tot}	total power dissipation SOT363	T _{amb} ≤ 25 °C note 1	–	300	mW
	SOT666	notes 1 and 2	–	300	mW

Notes

1. Device mounted on an FR4 printed-circuit board, single-sided copper, standard footprint.
2. Reflow soldering is the only recommended soldering method.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
Per transistor				
$R_{th \text{ j-a}}$	thermal resistance from junction to ambient	$T_{amb} \leq 25 \text{ }^\circ\text{C}$		
	SOT363	note 1	625	K/W
	SOT666	notes 1 and 2	625	K/W
Per device				
$R_{th \text{ j-a}}$	thermal resistance from junction to ambient	$T_{amb} \leq 25 \text{ }^\circ\text{C}$		
	SOT363	note 1	416	K/W
	SOT666	notes 1 and 2	416	K/W

Notes

1. Device mounted on an FR4 printed-circuit board, single-sided copper, standard footprint.
2. Reflow soldering is the only recommended soldering method.

CHARACTERISTICS

$T_{amb} = 25 \text{ }^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor; for the PNP transistor with negative polarity						
I_{CBO}	collector-base cut-off current	$V_{CB} = 50 \text{ V}$; $I_E = 0$	–	–	100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 30 \text{ V}$; $I_B = 0$	–	–	1	μA
		$V_{CE} = 30 \text{ V}$; $I_B = 0$; $T_j = 150 \text{ }^\circ\text{C}$	–	–	50	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5 \text{ V}$; $I_C = 0$	–	–	90	μA
h_{FE}	DC current gain	$V_{CE} = 5 \text{ V}$; $I_C = 5 \text{ mA}$	80	–	–	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 10 \text{ mA}$; $I_B = 0.5 \text{ mA}$	–	–	150	mV
$V_{i(off)}$	input-off voltage	$I_C = 100 \text{ }\mu\text{A}$; $V_{CE} = 5 \text{ V}$	–	1.2	0.8	V
$V_{i(on)}$	input-on voltage	$I_C = 2 \text{ mA}$; $V_{CE} = 0.3 \text{ V}$	3	1.6	–	V
R1	input resistor		33	47	61	$\text{k}\Omega$
$\frac{R2}{R1}$	resistor ratio		0.8	1	1.2	
C_c	collector capacitance	$I_E = I_e = 0$; $V_{CB} = 10 \text{ V}$; $f = 1 \text{ MHz}$				
	TR1 (NPN)		–	–	2.5	pF
	TR2 (PNP)		–	–	3	pF

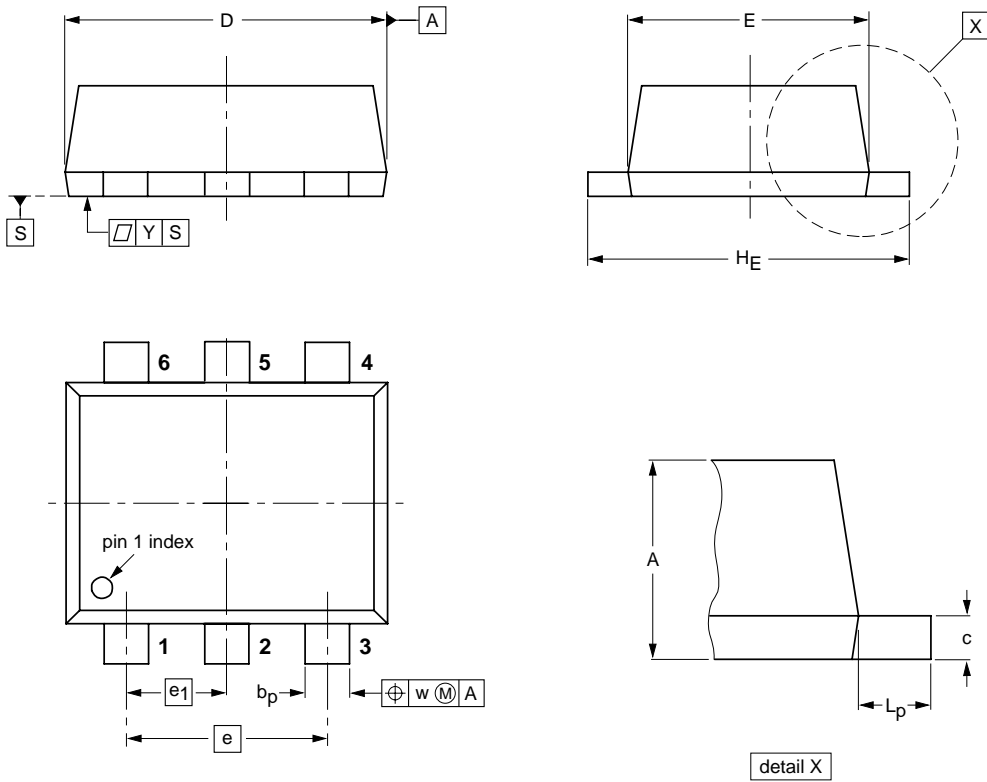
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PEMD12; PUMD12

PACKAGE OUTLINES

Plastic surface mounted package; 6 leads

SOT666



DIMENSIONS (mm are the original dimensions)

UNIT	A	b_p	c	D	E	e	e_1	H_E	L_p	w	y
mm	0.6 0.5	0.27 0.17	0.18 0.08	1.7 1.5	1.3 1.1	1.0	0.5	1.7 1.5	0.3 0.1	0.1	0.1

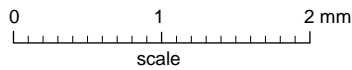
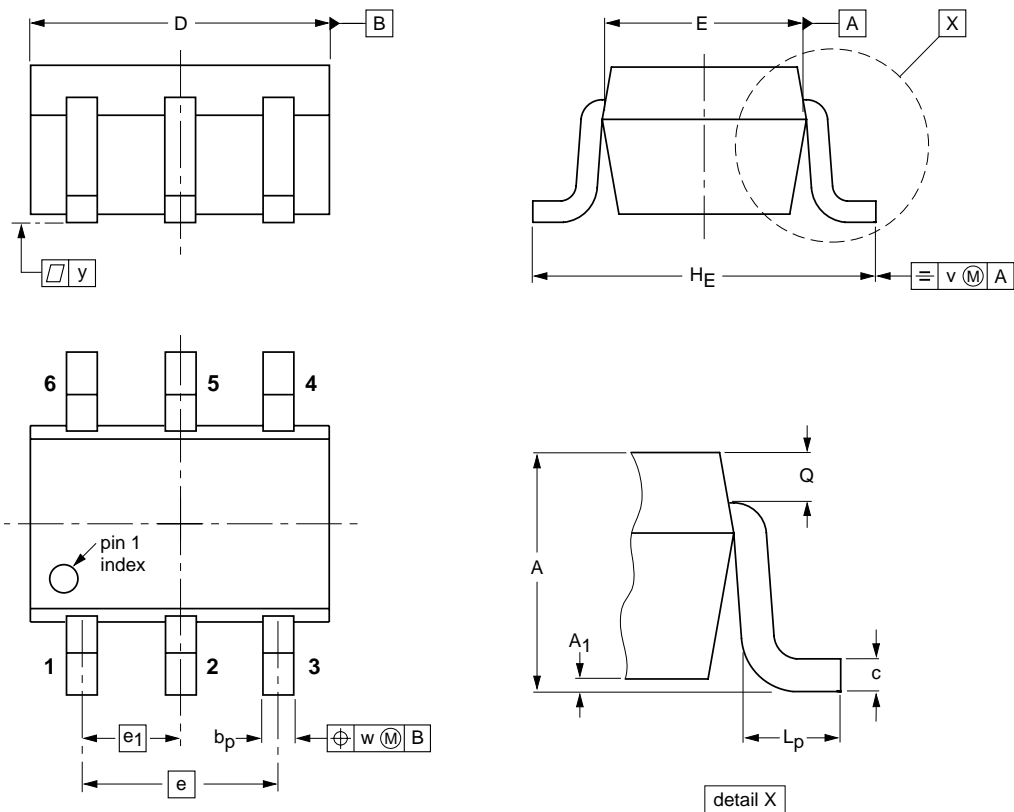
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT666					01-01-04 01-08-27

NPN/PNP resistor-equipped transistors;
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SOT363



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	bp	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT363			SC-88			97-02-28

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DATA SHEET STATUS

DOCUMENT STATUS⁽¹⁾	PRODUCT STATUS⁽²⁾	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

Notes

1. Please consult the most recently issued document before initiating or completing a design.
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