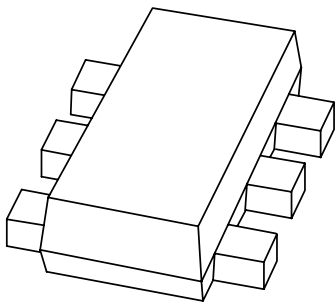


DATA SHEET



PEMD12 NPN/PNP resistor-equipped transistors

Product specification
Supersedes data of 2001 Aug 30

2001 Nov 07

NPN/PNP resistor-equipped transistors

PEMD12

FEATURES

- 300 mW total power dissipation
- Very small 1.6 mm x 1.2 mm ultra thin package
- Excellent coplanarity due to straight leads
- Replaces two SC-75/SC-89 packaged transistors on same PCB area
- Reduces required PCB area
- Reduced pick and place costs.

APPLICATIONS

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver.

DESCRIPTION

NPN/PNP resistor-equipped transistor in a SOT666 plastic package.

MARKING

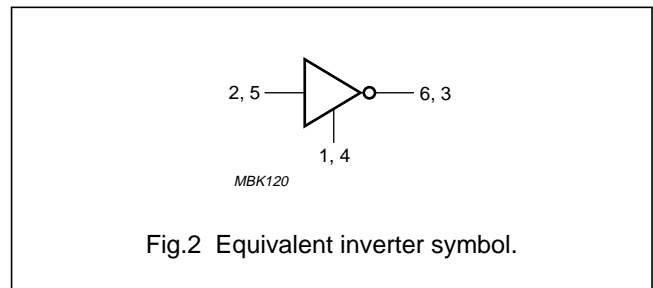
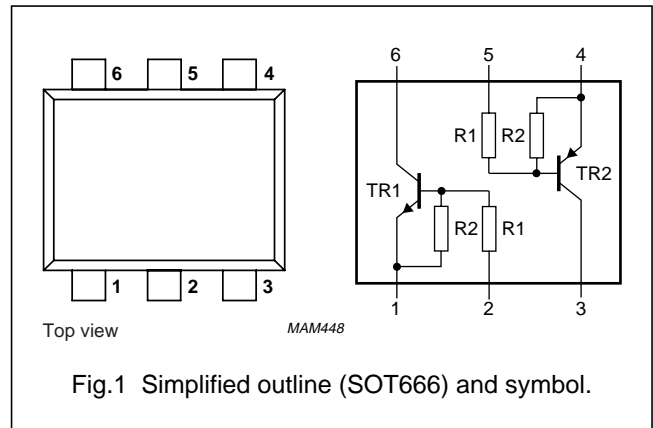
TYPE NUMBER	MARKING CODE
PEMD12	D2

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{CEO}	collector-emitter voltage	50	V
I_{CM}	peak collector current	100	mA
R1	bias resistor	47	k Ω
R2	bias resistor	47	k Ω

PINNING

PIN	DESCRIPTION
1, 4	emitter TR1; TR2
2, 5	base TR1; TR2
6, 3	collector TR1; TR2



NPN/PNP resistor-equipped transistors

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor for the PNP transistor with negative polarity					
V _{CBO}	collector-base voltage	open emitter	–	50	V
V _{CEO}	collector-emitter voltage	open base	–	50	V
V _{EBO}	emitter-base voltage	open collector	–	10	V
V _I	input voltage TR1		–	+40	V
			–	–10	V
	input voltage TR2		–	+10	V
			–	–40	V
I _o	output current (DC)		–	100	mA
I _{CM}	peak collector current		–	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C; notes 1 and 2	–	200	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	junction temperature		–	150	°C
T _{amb}	operating ambient temperature		–65	+150	°C
Per device					
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C; note 1	–	300	mW

Notes

1. Transistor mounted on an FR4 printed-circuit board.
2. The only recommended soldering is reflow soldering.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
R _{th j-a}	thermal resistance from junction to ambient	notes 1 and 2	416	K/W

Notes

1. Transistor mounted on an FR4 printed-circuit board.
2. The only recommended soldering is reflow soldering.

NPN/PNP resistor-equipped transistors

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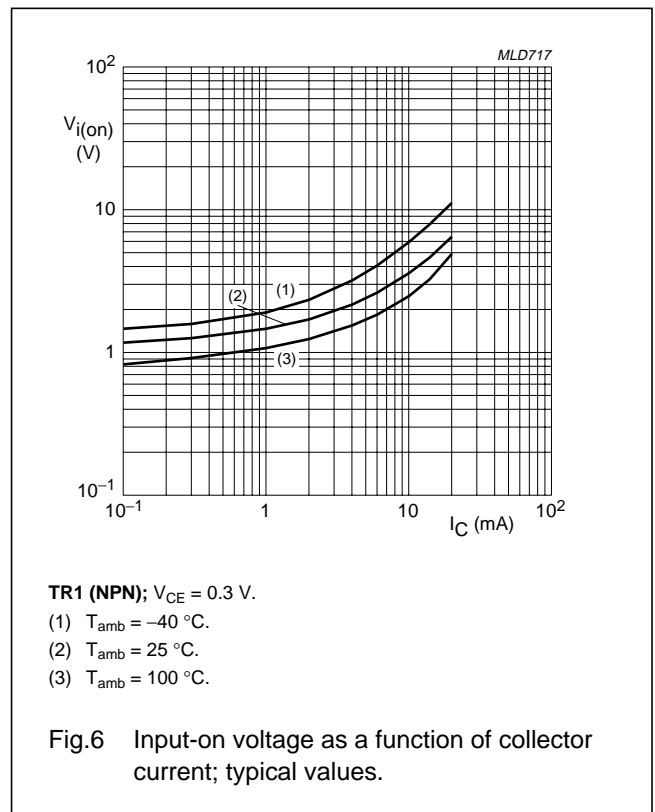
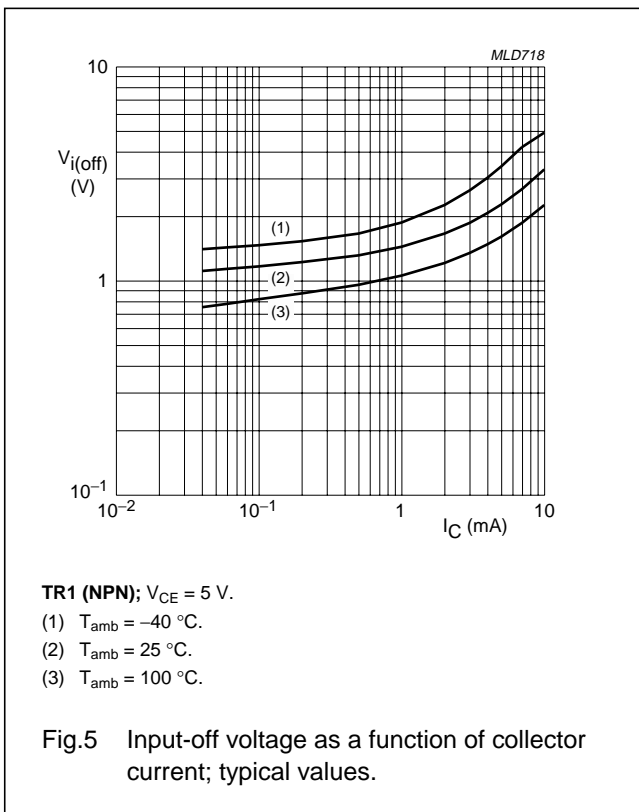
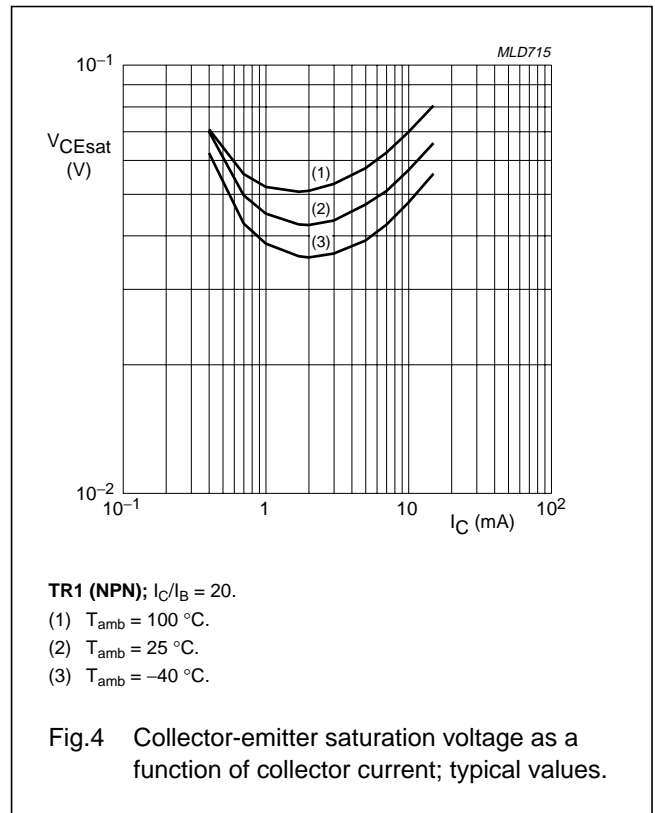
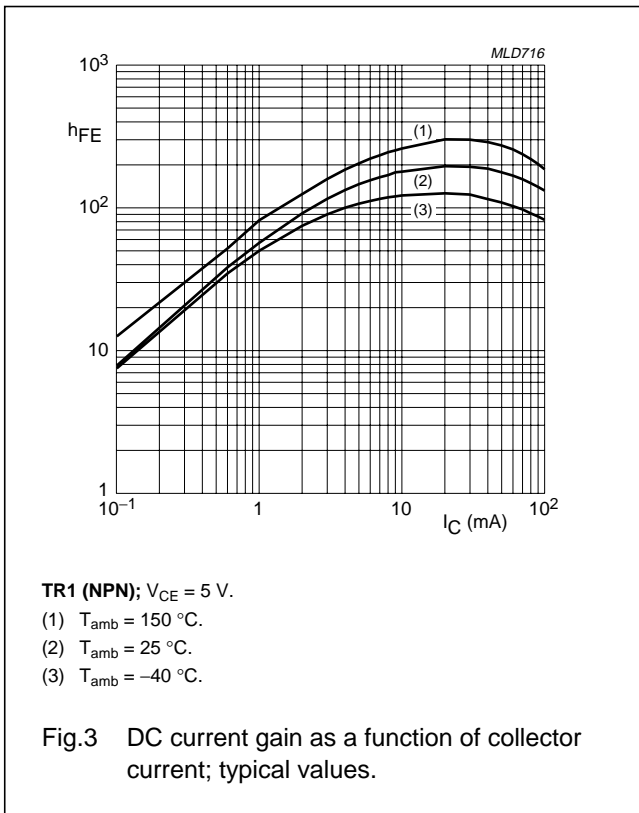
CHARACTERISTICS

$T_{amb} = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor for the PNP transistor with negative polarity						
I_{CBO}	collector-base cut-off current	$V_{CB} = 50\text{ V}; I_E = 0$	–	–	100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 50\text{ V}; I_B = 0$	–	–	1	μA
		$V_{CE} = 30\text{ V}; I_B = 0; T_j = 150\text{ °C}$	–	–	50	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5\text{ V}; I_C = 0$	–	–	90	μA
h_{FE}	DC current gain	$V_{CE} = 5\text{ V}; I_C = 5\text{ mA}$	80	–	–	
V_{CEsat}	saturation voltage	$I_C = 10\text{ mA}; I_B = 0.5\text{ mA}$	–	–	150	mV
$V_{i(off)}$	input off voltage	$V_{CE} = 5\text{ V}; I_C = 100\text{ }\mu\text{A}$	–	1.2	0.8	V
$V_{i(on)}$	input on voltage	$V_{CE} = 0.3\text{ V}; I_C = 2\text{ mA}$	3	1.6	–	V
R_1	input resistor		33	47	61	$\text{k}\Omega$
$\frac{R_2}{R_1}$	resistor ratio		0.8	1	1.2	
C_c	collector capacitance	$I_E = i_e = 0; V_{CB} = 10\text{ V};$ $f = 1\text{ MHz}$	–	–	2.5	pF
	TR1 (NPN)				3	pF
	TR2 (PNP)		–	–		

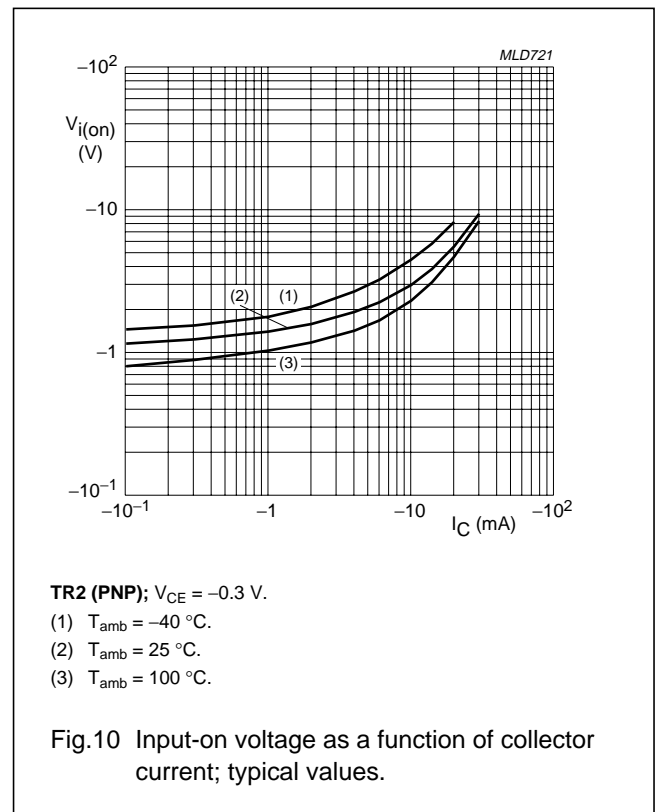
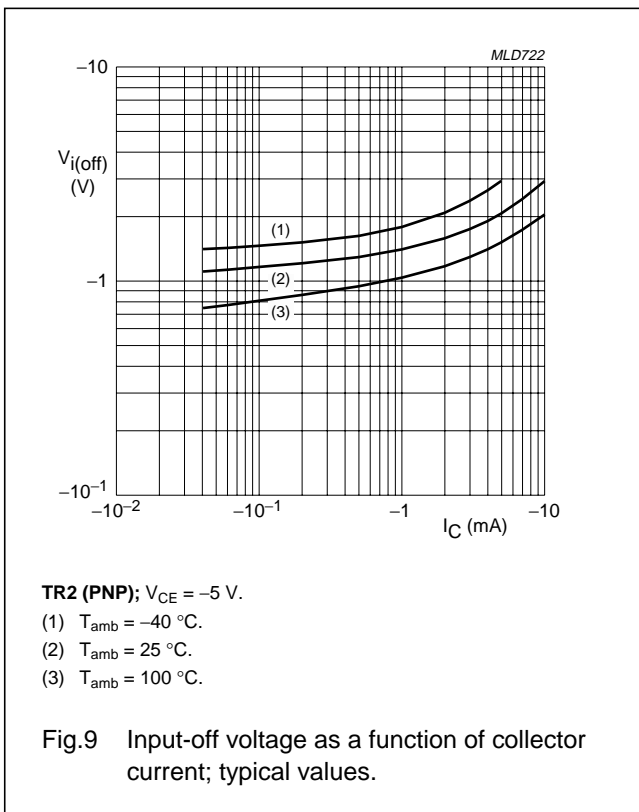
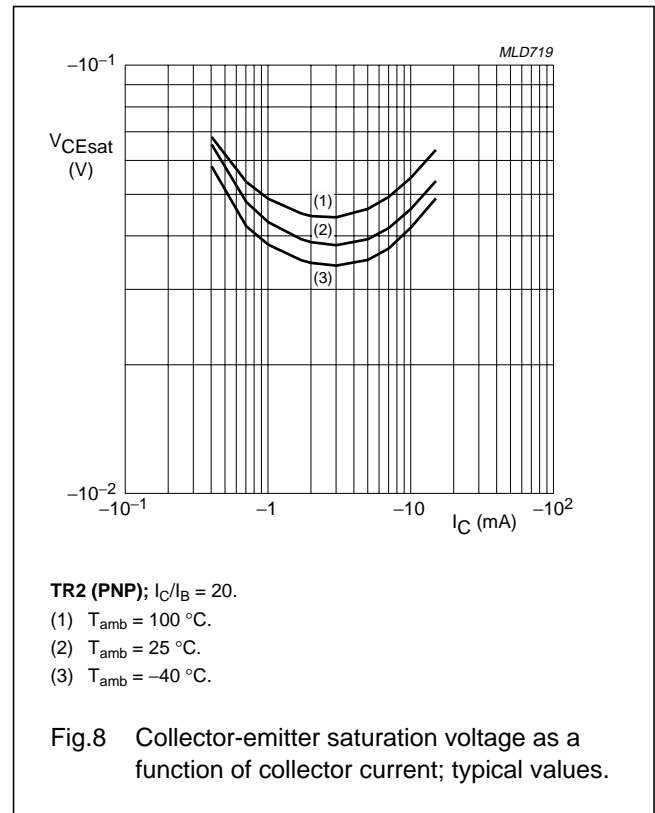
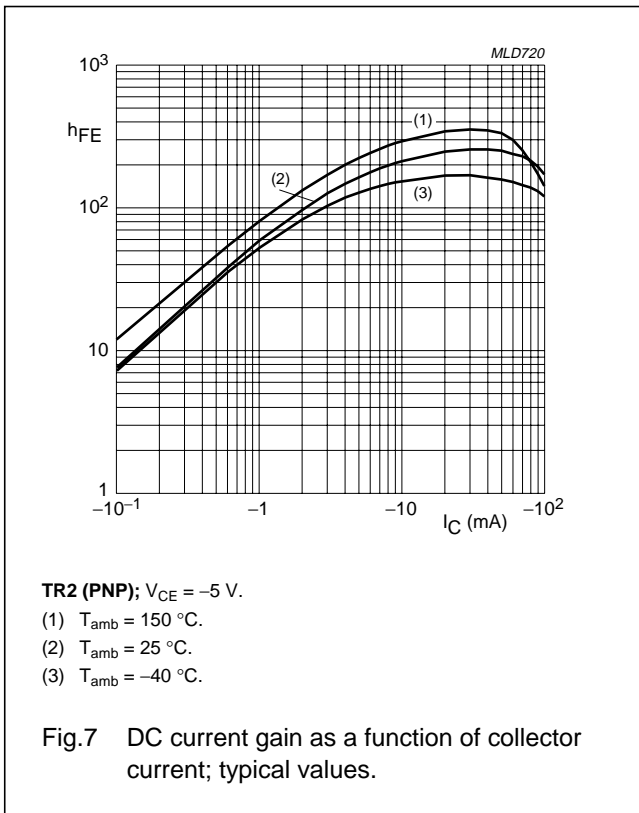
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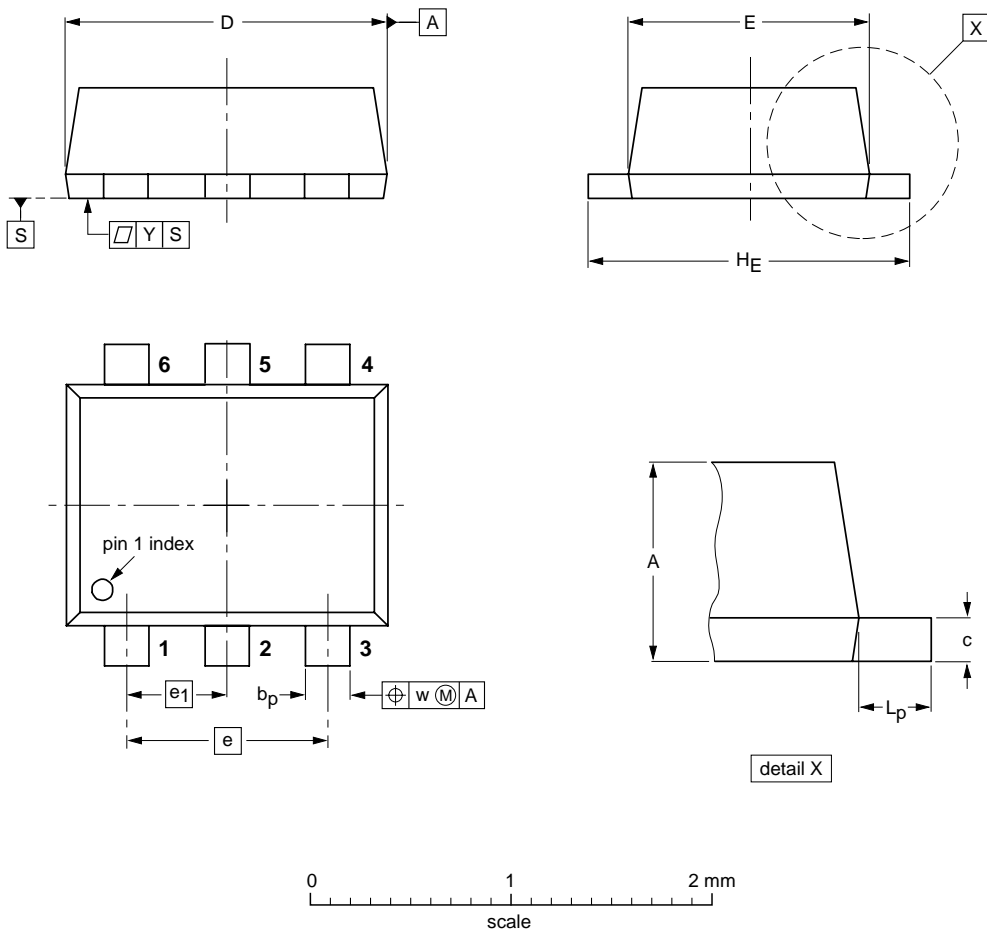
NPN/PNP resistor-equipped transistors

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PACKAGE OUTLINE

Plastic surface mounted package; 6 leads

SOT666



DIMENSIONS (mm are the original dimensions)

UNIT	A	b_p	c	D	E	e	e_1	H_E	L_p	w	y
mm	0.6 0.5	0.27 0.17	0.18 0.08	1.7 1.5	1.3 1.1	1.0	0.5	1.7 1.5	0.3 0.1	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT666						01-01-04 01-08-27

NPN/PNP resistor-equipped transistors

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NOTES

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NOTES

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