POWERTIP TECH. CORP.

DISPLAY DEVICES FOR BETTER ELECTRONIC DESIGN

Specification For Approval

【產品規格書】

Customer : _____

Model Type : LCD Module

Sample Code : PG12864LRU-ORA-H-S0

Mass Production Code : _____

Edition : 0

Customer Sign	Sales Sign	Approved By	Prepared By

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1. SPECIFICATIONS

1.1 Features

- Full dot-matrix structure with 128 dots *64 dots
- 1/64 Duty, 1/9 bias
- STN LCD, positive
- Transflective LCD, Yellow Green type
- 6 o'clock viewing angle
- 8 bits parallel data input , using 80-family MPU Interface
- LED edge type Backlight

1.2 Mechanical Specifications

- Outline dimension : 80.0mm(L)*54.0mm(W)*10.2mm (H)
- Viewing area : 73.6mm *41.0mm
- Active area : 66.52mm *33.24mm
- Dot size : 0.48mm * 0.48mm
- Dot pitch : 0.52mm * 0.52mm

1.3 Absolute Maximum Ratings

Item	Symbol	Conditions	Min.	Max.	Unit
Power supply Voltage	V_{DD}	-	0	6.0	V
LCD drive Supply voltage	V_{DD}-V_{LC}	-	0	15.0	V
Input voltage	V_{IN}	-	0	V_{DD}+0.3	V
Operating temperature	T_{OPR}	-	-20	+70	°C
Storage temperature	T_{STG}	-	-30	+80	°C
Humidity	H_D	-	-	90	%RH

1.4 DC Electrical Characteristics

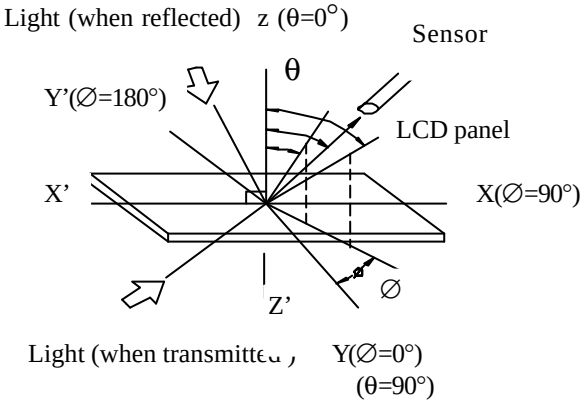
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Logic Supply voltage	V_{DD}	-	-	5.0	-	V
"H" input voltage	V_{IH}	-	0.7V_{DD}	-	V_{DD}	V
"L" input voltage	V_{IL}	-	0	-	0.3V_{DD}	V
Supply current	I_{DD}	V_{DD}=5V	-	1.0	1.2	mA
LCD driving voltage	V_{OP}	70°C	9.0	9.4	9.9	V
		25°C	10.1	10.5	11.0	
		-20°C	10.9	11.5	12.1	

1.5 Optical Characteristics

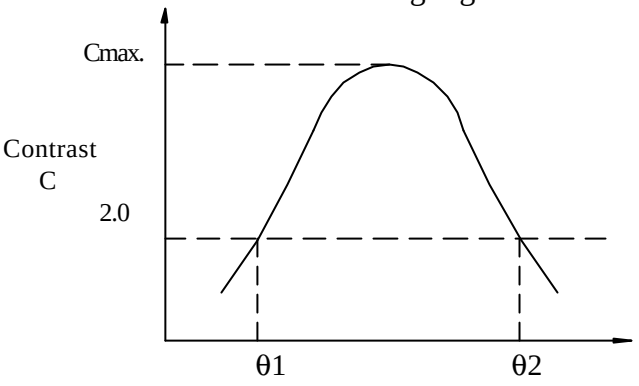
1/64 duty, 1/9 bias, Vopr=10.5V, Ta=25°C

Item	Symbol	Conditions	Min.	Typ.	Max	Reference
Viewing angle	θ	C≥2.0,∅=0°	30°	-	-	Notes 1 & 2
Contrast	C	θ=5°, ∅=0°	3	5	-	Note 3
Response time(rise)	tr	θ=5°, ∅=0°	-	140ms	200ms	Note 4
Response time(fall)	tf	θ=5°, ∅=0°	-	300ms	500ms	Note 4

Note 1: Definition of angles θ and ∅



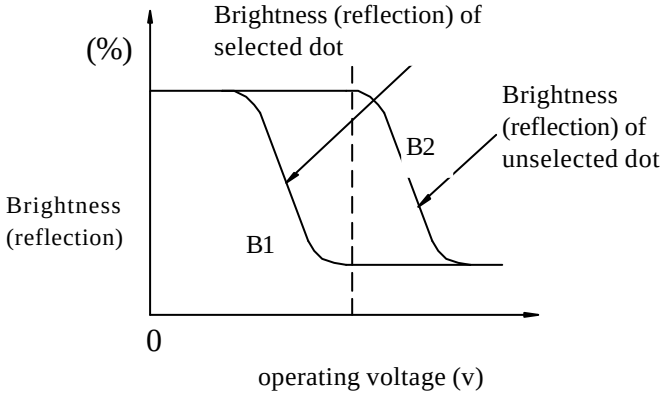
Note 2: Definition of viewing angles θ1 and θ2



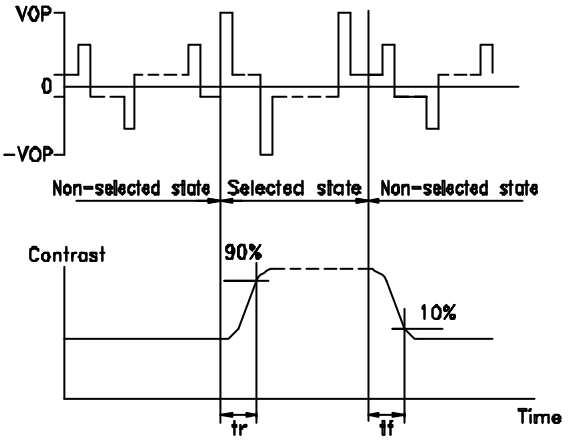
Note : Optimum viewing angle with the same naked eye and viewing angle θ at Cmax. Above are not always the same.

Note 3: Definition of contrast C

$$C = \frac{\text{Brightness (reflection) of unselected dot (B2)}}{\text{Brightness (reflection) of selected dot (B1)}}$$



Note 4: Definition of response time



Note: Measured with a transflective LCD panel which is displayed 1 cm^2

V_{OPR} : Operating voltage
f_{FRM} : Frame frequency
t_r : Response time (rise)
t_f : Response time (fall)

1.6 Backlight Characteristic

The LCD Module is backlight using a LED panel

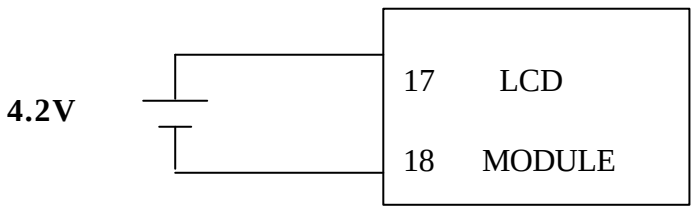
•.Maximum Ratings

Item	Symbol	Conditions	Min.	Max.	Unit
Forward current	IF	TA=25°C	-	200	mA
Reverse voltage	VR	TA=25°C	-	8	V
Power dissipation	PO	TA=25°C	-	0.92	W
Operating Temperature	TOPR	-	-20	70	°C
Storage temperature	TSTG	-	-40	80	°C

•.Electrical Ratings

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Forward voltage	VF	IF=80mA	4.0	4.2	4.6	V
Reverse current	IR	VR=8V	-	-	0.2	mA
Luminous intensity*	IV	IF=80mA	9.6	12.0		cd/m^2
Wavelength	HUE	IF=80mA	569	-	576	nm
Color	Yellow Green					

*Used BM-8 tester ,high=300mm



2. MODULE STRUCTURE

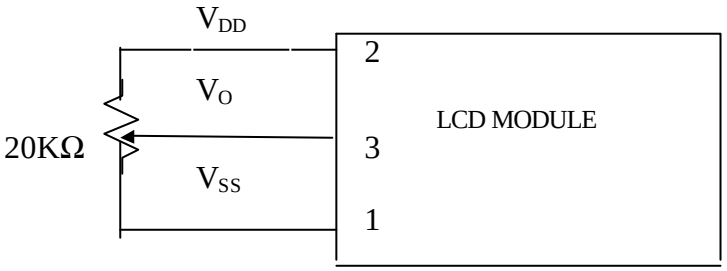
2.1 Counter Drawing

*See Appendix

2.2 Interface Pin Description

Pin No.	Symbol	Function
1	V_{SS}	Power Supply (Vss=0)
2	V_{DD}	Power Supply (V_{DD}>V_{SS})
3	V_O	Operating voltage for LCD
4	/RES	Controller reset (module reset)
5	/CS	Used to enter chip select signal.
6	RS	Used to identify data sent by MPU at D0 to D7.
7	/WR	Data write (write data to the module at “L”)
8	/RD	Data read (read data from the module at “L”)
9~16	DB0~DB7	Data bus
17	A	Power supply LED backlight (+)
18	K	Power supply LED backlight (-)

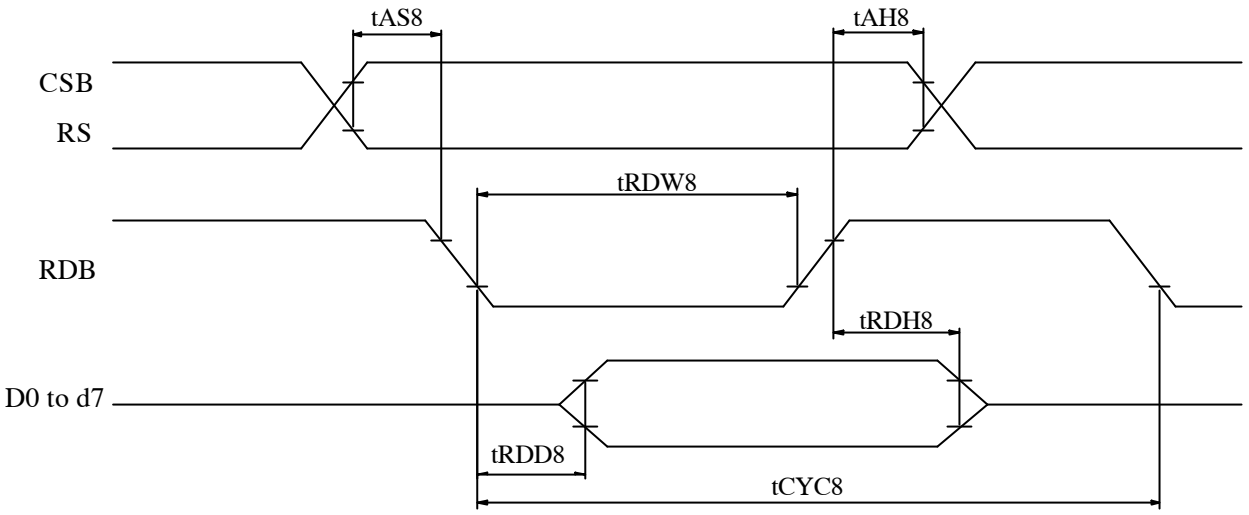
Contrast Adjust



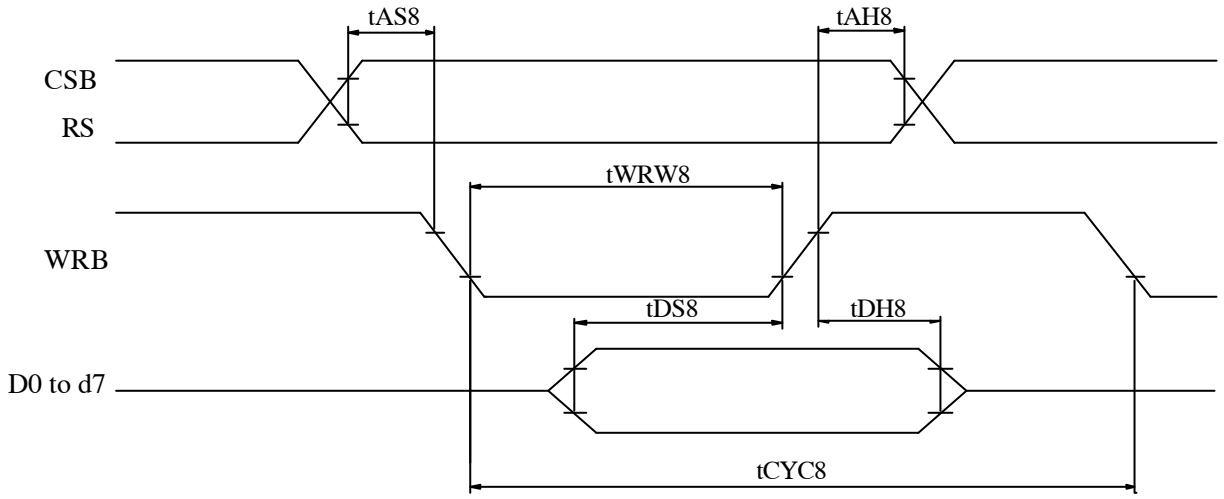
2.3 Timing Characteristics

2.3.1 system Bus Read/Write Timing (80 Family MPU)

Read timing



Write timing



(MPU timing characteristics)

(VDD=2.7 to 5.5V,Ta=-30 to +85℃)

Item	Symbol	Mesauring condition	MIN	MAX	Unit	Appllcable pin
Address hold time	tAH8		60		ns	CSB
Address setup time	tAS8		40		ns	RS
System cycle time	tCYC8		450		ns	RDB
Road pulse width (READ)	tRDW8		270		ns	WRB
Write pulse width (WRITE)	tWRW8		100		ns	
Data setup time	tDS8		100		ns	D0 to D7
Data hold time	tDH8		40		ns	
Read data output delay time	tRDD8	CL=15pF		220	ns	D0 to D7
Read data hold time	tRDH8		10		ns	
Input signal rise and fall time	tr,tf			30	ns	All of above pins

(VDD=2.4 to 2.7V,Ta=-30 to +85℃)

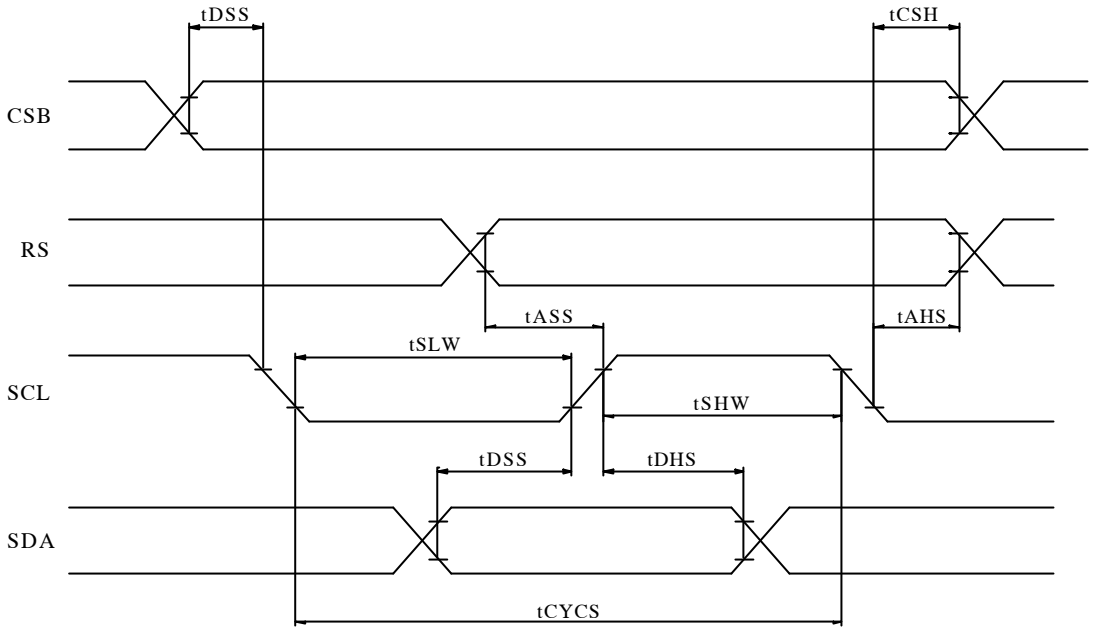
Item	Symbol	Mesauring condition	MIN	MAX	Unit	Appllcable pin
Address hold time	tAH8		80		ns	CSB
Address setup time	tAS8		80		ns	RS
System cycle time	tCYC8		900		ns	RDB
Road pulse width (READ)	tRDW8		500		ns	WRB
Write pulse width (WRITE)	tWRW8		200		ns	
Data setup time	tDS8		200		ns	D0 to D7
Data hold time	tDH8		80		ns	
Read data output delay time	tRDD8	CL=15pF		320	ns	D0 to D7
Read data hold time	tRDH8		10		ns	
Input signal rise and fall time	tr,tf			30	ns	All of above pins

. (VDD=1.8 to 2.4V,Ta=-30 to +85℃)

Item	Symbol	Mesauring condition	MIN	MAX	Unit	Appllcable pin
Address hold time	tAH8		160		ns	CSB
Address setup time	tAS8		160		ns	RS
System cycle time	tCYC8		1800		ns	RDB
Road pulse width (READ)	tRDW8		1000		ns	WRB
Write pulse width (WRITE)	tWRW8		400		ns	
Data setup time	tDS8		400		ns	D0 to D7
Data hold time	tDH8		160		ns	
Read data output delay time	tRDD8	CL=15pF		640	ns	D0 to D7
Read data hold time	tRDH8		10		ns	
Input signal rise and fall time	tr,tf			30	ns	All of above pins

Note:All the timings must be specified relative to 20% and 80% of VDD voltage

2-3.2 Serial Interface Timing



(VDD=2.4~5.5V,Ta=-30 to +85℃)

Item	Symbol	Mesauring condition	MIN	MAX	Unit	Appllcable pin
Serial clock period	tCYCS		1000		ns	SCL
SCL “H” pulse width	tSHW		400		ns	
SCL “L” pulse width	tSLW		400		ns	
Address setup time	tASS		80		ns	RS
Address hold time	tAHS		80		ns	
Data set up time	tDSS		400			SDA
Data hold time	tDHS		400		ns	
DSB to SCL time	tCSS		80		ns	CSB
CSB hold time	tCSH		80		ns	
Input signal rise and fall time	tr,tf			30	ns	All of above pins

(VDD=1.8~2.4V,Ta=-30 to +85℃)

Item	Symbol	Mesauring condition	MIN	MAX	Unit	Appllcable pin
Serial clock period	tCYCS		2000		ns	SCL
SCL “H” pulse width	tSHW		800		ns	
SCL “L” pulse width	tSLW		800		ns	
Address setup time	tASS		160		ns	RS
Address hold time	tAHS		160		ns	
Data set up time	tDSS		800			SDA
Data hold time	tDHS		800		ns	
DSB to SCL time	tCSS		160		ns	CSB
CSB hold time	tCSH		160		ns	
Input signal rise and fall time	tr,tf			30	ns	All of above pins

Note: All the timings must be specified relative to 20% and 80% of VDD voltage.

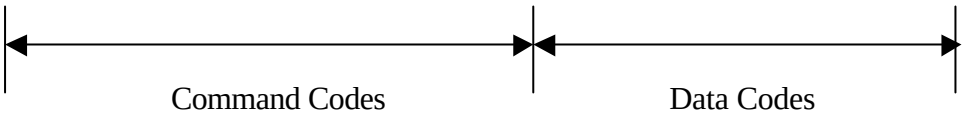
2.4 Command Function

The LH155BA has a lot of commands as shown in a list of command and each command is explaned in detall as follows.

Data codes and command codes are defined as follows and execution of commands must be made in the state of chip select (CSB="L")

(For example X address)

RS	D7	D6	D5	D4	D3	D2	D1	D0
e※	0	0	0	0	AX3	AX2	AX1	AX0



※RS = "0" : RAM Data Access (7-1,7-2)
RS = "1" : Register Access (7-3~7-16)
The undefined command codes are inhibited.

2-4.1 Data Write to Display RAM

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	0	Display RAM write data							

The Display RAM data of 8-bit are written in the designated X and Y address.

2-4.2 Data Read to Display RAM

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	0	Display RAM read data							

The 8-bit contents of Display RAM designated in X and Y address and read out immediately after data are set in X and Y address, dummy read is necessary once.

2-4.3 X Address Register Set

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	0	0	AX3	AX2	AX1	AX0

(At the time of reset AX3~AX0 = 0H, read address : 0H)

Addresses of Display RAM's X direction are set. The values of AX3 to AX0 are usable up to 00H-0F, but 10H-FFH are inhibited. When the register setting SEG output normal/reverse is REF = "0", the data of AX3~AX0 are addressed to Display RAM as they are.

When REF = "1", the data of 0FH-(AX3~AX0)H are addressed to Display RAM.

2-4.4 Y Address Register Set

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	0	AY3	AY2	AY1	AY0

(At the time of reset AX3~AX0 = 0H, read address : 2H)

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	1	1	※	AY6	AY5	AY4

※ mark shows "Don't care"

(At the time of reset:AY6~AY4=0H, read address:3H

Addresses of Display RAM's Y direction are set. In data setting, lower place and upper place are divided with 4 bit and 3 bit respectively.

When data set, lower place must be set first and upper place must be set second.

The values of AY6 to AY0 are usable up to 00H-42H, but 43H-FFH are inhibited.

The addresses of 40H to 42H are for the Segment Display RAM.

2-4.5 Display Starting Line Register Set

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	0	LY3	LY2	LY1	LY0

(At the time of reset AX3~AX0 = 0H, read address: 4H)

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	0	1	※	※	LA5	LA4

※ mark shows "Don't care" (At the time of reset :LA4,LA5 = 0H, read address: 5H)

The display line address is required to designate, and the designated address become the display line of COM0.

The display of LCD panel is indicated in he increment direction of the designated display starting address to the line address.

LA5	LA4	LA3	LA2	LA1	LA0	LINE ADDRESS
0	0	0	0	0	0	0
0	0	0	0	0	1	1
1	1	1	1	1	1	63

2-4.6 n Line Alternated Register Set

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	0	N3	N2	N1	N0

(At the time of reset: N3~N0 = 0H, read address: 6H)

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	1	1	※	※	N5	N4

※ mark shows "Don't care"(At the time of reset: N5~N4 = 0H, read address: 7H)

The reverse line number of LCD alternated drive is required to set in the register. The line number possible to set is 2-64 lines.

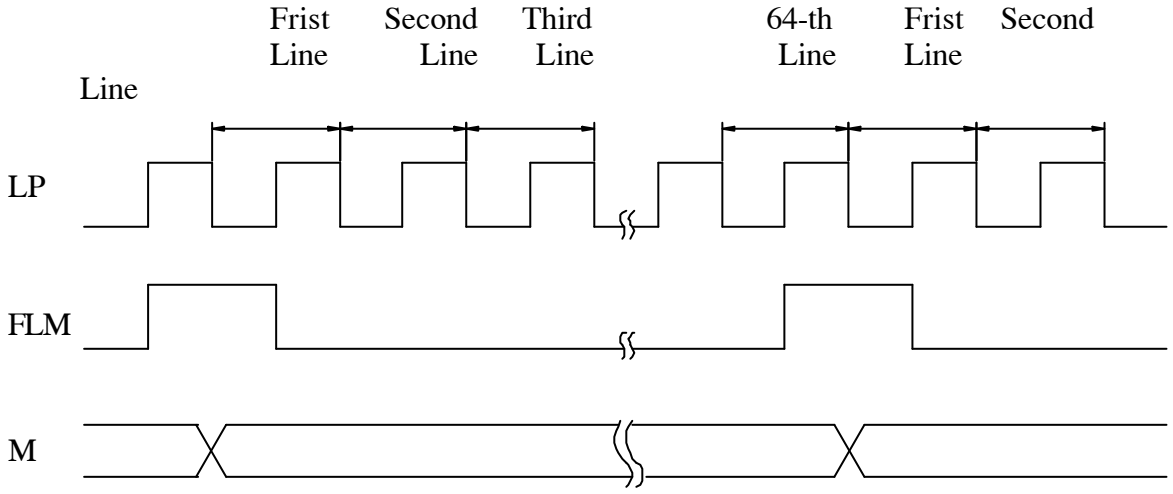
The values set up by the n-line alternated register become enable when the n line alternated drive command of ON. (NLIN="1")

When the n line alternated drive command is OFF (NLIN="0"), alternated drive waveform which reverses by frame cycle is generated.

LA5	LA4	LA3	LA2	LA1	LA0	LINE ADDRESS
0	0	0	0	0	0	-
0	0	0	0	0	1	2
1	1	1	1	1	1	64

2-4.7 Alternated Timing

At the Time of n Line Alternated OFF (in case of 1/64 DUTY Display)



2-4.8 Display Control(1) Register Set

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	0	0	SHIFT	SEGMENT	ALLON	ON/OFF

(At the time of reset: (SHIFT, SEGON, ALLON, ON/OFF)=0H, read address: 8H)

Various control of display is set up.

(I) ON/OFF Command (For the Graphic Display only)

To control ON/OFF of the Graphic Display

ON/OFF = "0": display OFF

ON/OFF ="1" : display ON

(II) ALLON Command (For the Graphic Display only)

Regardless of the data of the Graphic Display RAM, the Graphic Display are on.

This command has priority over display normal/reverse commands.

SEGON="0":display OFF The terminals are specified VSS level.

SEGON="1":display ON

(III) SEGMENT Command (For the Segment Display only)

To control ON/OFF of the Segment Display

SEGON="0":display OFF The terminals are specified VSS level.

SEGON="1":display ON

(IV) SHIFT Command (For the Graphic Display only)

The shift direction of the Graphic Display scanning data in the common driver output is selected.

SHIFT="0":COM0->COM63 shift-scan

SHIFT="1":COM63->COM0 shift-scan

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	0	0	※	※	ER	IR

※ mark shows "Don't care"(At the time of reset: (ER,IR)=0H,read address:8H)

(i) IR Command (For the Segment Display only)

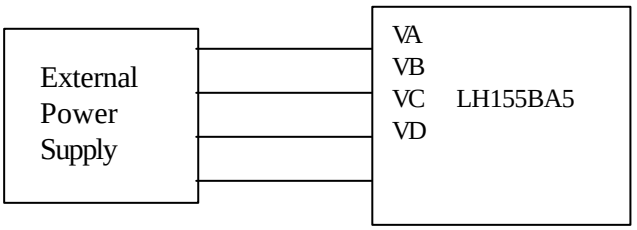
IR command is not available now. When using the Segment Display, please set "0"

(ii) ER Command (For the Segment Display only)

ER command is not available now. When using the Segment Display, please set "1"

And when using the Segment Display, please input VA, VB, VC and VD level externaly.

2-4.9 Display Control(2) Register Set



RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	0	1	REV	NLIN	SWAP	REF

(At the time of reset: (REV, NLIN, SWAP, REF)=0H, read address: 9H)

Various control of display is set up.

(I) REF Command

When MPU accesses to the Graphic Display RAM, the relationship between X address and write data is normalized or reversed.

Therefore, the order of segment driver output can be reversed by register setting, lessening the limitation of IC location in assembling into the LCD panel.

REF	ACCESS FROM MPU		INTERNAL ACCESS		DDRRESPONDING SEG OUTPUT
	X ADDRESS	D7~D0	X ADDRESS	D7-D0	
0	NH	D0(LSB) D7(MSB)	NH	(LSB) (MSB)	SEG(8*NH) Output SEG(8*NH+7) Output
1	NH	D0(LSB) D7(MSB)	0FH-NH	(MSB) (LSB)	SEG(8*(0F-NH)+7) Output SEG(8*(0F-NH)) Output

When using this command. Output of Segment Display Circuits are set as below.
However the order of D0->D7 are not changed.

REF	ACCESS FROM MPU		INTERNAL ACCESS		DDRRESPONDING SEG OUTPUT
	X ADDRESS	D7~D0	X ADDRESS	D7-D0	
0	00H	D0(LSB) D7(MSB)	00H	D0(LSB) D7(MSB)	D7->D0 SEGS0->SEGS7
0	01H	D0(LSB) D3(MSB)	01H	D0(LSB) D3(MSB)	D0~D3 SEGS8->SEGS11
1	0FH	D0(LSB) D7(MSB)	00H	D0(LSB) D7(MSB)	D0->D7 SEGS0->SEGS7
1	H0E	D0(LSB) D3(MSB)	01H	D0(LSB) D3(MSB)	D0->D3 SEGS8->SEGS11

When REF="1",please set X address of Segment Display Circuits like below.

00H->0FH

01H->0EH

(iii) SWAP Command (For the Graphic Display only)

When data to the Graphic Display RAM are written, the write data are swapped.

SWAP="1": Normal mode. In data-writing, the data of D7~D0 can be written to the Graphic Display RAM.

SWAP="1": SWAP mode ON. In data-writing, the swapped data of D7~D0 can be written to the Graphic Display RAM.

	SWAP="0"	SWAP="1"
EXTERNAL DATA	D7 D6 D5 D4 D3 D2 D1 D0	D7 D6 D5 D4 D3 D2 D1 D0
INTERNAL DATA	d7 d6 d5 d4 d3 d2 d1 d0	d0 d1 d2 d3 d4 d5 d6 d7

(iii) NLIN Command (For the Graphic Display only)

The ON/OFF control of n-line alternated drive is performed.

NLIN="0" : n line alternated drive OFF. By using frame cycle, the alternated signals (M) are reversed.

NLIN="1" : n line alternated drive ON. According to data set up in n line alternated register, the alternation is made.

(iv) REV Command (For the Graphic Display only)

Corresponding to the data of the Graphic Display RAM, the lighting or not-lighting of the display is set up.

REV="0": When RAM data at "H", LCD at ON voltage (normal)

REV="1": When RAM data at "L", LCD at ON voltage (reverse)

2-4.10 Increment Control Register Set

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	1	0	※	AIM	AY1	AX1

※ mark shows "Don't care"(At the time of reset: (AIM, AY1, AX1)= 0H, read address :AH)

The increment mode is set up when accessing to the Graphic Display RAM. (The Graphic Display RAM only)

By AIM, AY1 and AX1 registers, the setting-up of increment operation /non-operation for the X-address counter and the Y-address counter every write access of every read access to the Graphic Display RAM is possible.

In setting to this control register, the increment operation of address can be made without setting successive addresses for writing data or for reading data to the Graphic Display RAM from MPU.

After setting this register be sure to set the X and Y Address Register.

Because it is not assuring the data of X and Y Address Register after setting increment Control Register.

The increment control of X and Y address by AIM, AY1 and AX1 registers is as follows.

ALM	SELECTION OF INCREMENT TIMING	REFERENCE
0	When writing to Graphic Display RAM or reading from Graphic Display RAM	<1>
1	Only when writing to Graphic Display RAM (read modify)	<2>

<1> This is effective when subsequently writing and reading the successive address area.

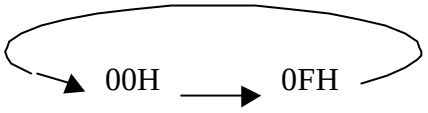
<2> This is effective in the case that after reading and writing the successive address area every address, the read data are modified to write.

AY1	AX1	SELECTION OF INCREMENT ADDRESS	REFERENCE
0	0	Increment is not made	<1>
0	1	X address automatic increment	<2>
1	0	Y address automatic increment	<3>
1	1	X and Y address cooperative, automatic increment	<4>

<1> Regardless of AIM, no increment for X and Y address.

<2> According to the setting-up of AIM, increment or decrement for only X address.
In accordance with the REF conditions of SEG normal/reverse output setting register, X address become as follows.

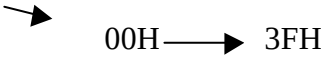
・At REF="0" (normal output), increment by loop of



・At REF="1" (reverse output), decrement by loop of

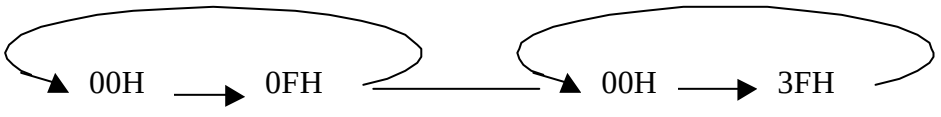
<3> According to the setting-up of AIM, increment for only Y address.
Regardless of REF, increment by loop of

for Y address.



<4> According to the setting-up of AIM, cooperative variation for X and Y address.
When the access of X address is made up to 0FH, Y address increment occurs.

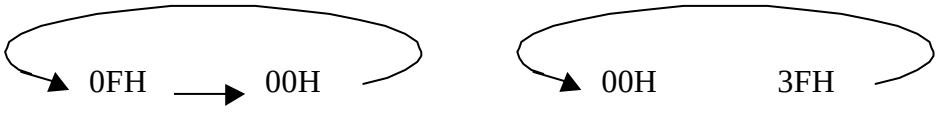
・At REF="0" (normal output)



(X address)
vary in the above loops.

(Y address)

・At REF="1" (reverse output)



2-4.11 Power Control Register Set (1)

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
		(X address) vary in the above loops.				(Y address)			
0	1	1	0	1	1	BIAS	HALT	PON	ACL

(At the time of reset:BIAS,HLT,PON,ACL)=0H, read address: BH)

(1) ACL Command

The internal circuit can be initiallized. This command is enabled only at Master operation mode.

ACL="0":Normal operation

ACL="1":Initialization ON

If the power control register is read out immediately after executing ACL command (ACL=1), the D0 bit becomes "0".

In executing ACL command, the internal reset signals are internary generated by using display-clock onginal oscillation (oscillation by OSC1 and OSC0, or clock input at CK pin).

Therefore, after executiting ACL command, allow WAIT period having at least two cycle portion of the original oscillation clock before the next processing is made.

(2) PON Command

The internal power supply for the Graphic Display circult is set ON/OFF.

PON="0: Power supply for the Graphic Display circuit OFF

PON="1: Power supply for the Graphic Display circuit ON

At PON="1": the booster and volage converter for the Graphic Display circuit function.

In accordance with the setting conditions of PMODE pin, the operative circuit part changes. See the Function Description in detall.

(3) HALT Command

The conditions of power-saving are set ON/OFF by this command.

HALT="0": Nornal operation

HALT="1": Power-saving operation

When setting in the power-saving state, the consumed current can be reduced to a value near to the stanby current. The intrnal conditions at power-saving are as follows.

(a) The oscillating circuit and power supply circuit are stopped.

(b) The LCD drive is stopped, and output of the segment drive and common driver are VSS lovel.

(c) The clock input from CK pin is inhibited.

(d) The contents of the Display RAM data are mintained.

(e) The operational mode maintains the state of command execution before executing power-saving command.

(4) BIAS Command

The internal bias value for the Graphic display can be set by this command.

BIAS="0": 1/9 bias

BIAS="1": 1/7 bias

(Bias value for the Segment Display is 1/3 Fixed)

2-4.12 Power Control Register Set (2)

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	0	1	MSS	·····	LSB	

(At the time of reset:DVOL)=0H, read address: DH

The LCD drive voltage V0 output from the built-in power circuit can be controlled and the display controlled and the display tone on the LCD can be also controlled.

The LCD drive V0 takes one out of 16 voltage values by setting 4 bit data register.

MSB	···		LSB	V0/SV0
0	0	0	0	Smaller
1	1	1	1	Larger

If the electronic control is not used, specify(1,1,1,1) in the 4-bit data register.

After the LH155BA is reset, the 4-bit data register is automatically set to (1,1,1,1)

2-4.13 Power Control register Set (3)

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	1	0	SEGPON	※	EXA	ICON

※mark show "Don't care" (At the time of reset: (SEGPON, EXA, ICON)=0H, read address: EH)

(1) ICON Command

ICON Display ON/OFF

ICON ="0": ICON is OFF

ICON = "1": ICON is ON, See the Function Description in detall.

(2) EXA Command

Clock for ICON Display External/Internal

EXA="0": Internal Clock

EXA="1": External Clock from EXA terminal

(3) SEGPON Command

A power supply for the Segment Display is set ON/OFF

SEGPON="0": Power supply circuit OFF

SEGPON="1": Power supply circuit ON

At SEGPON ="1", the sub-voltage converter for Segment Display function.

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	1	0	DU1	DU0	BS1	BS0

(At the time of reset: (DU1,DU0,BS1,BS0)=0H, read address: EH)

(1) BS Command

Select booat voltage level below.

BS		BOOST VOLTAGE LEVEL
BS1	BS0	
0	0	PROHIBITION
0	1	3 TIMES
1	0	2 TIMES
1	1	PROHIBITION

(2) Duty Command

Select Duty ratic below..

DUTY		DUTY RATIO
D3	D2	
0	0	1/64
0	1	1/48
1	0	1/32
1	1	1/16

This module is 1/64 duty.

2-4.14 RE Register Set

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0/1	1	1	1	1	0	※	※	※	RE

※mark show "Don't care" (At the time of reset: (RE)=0H, read address: FH)

RE Command

RE="0": the below register cannot be accessed.

RE="1": the extended function set, electric volume for the Segment

Display, Duty ratio select and boost voltage level select can be accessed.

2-4.15 Address Set for Internal Register Read

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	0	0	RA3	RA2	RA1	RA0

(At the time of reset: (RA3, RA2, RA1, RA0)=CH)

Then data set up in the internal registers ate read out, set the address for Read allotted to each register by this command before executing the Read command of the internal registers.

For example, when the data of the command register in the display control (**1**) are read out, set the values of (RA3, RA2, RA**1**, RA0)=8H.

Refer to the Function description of each command or at list of commands on the address for Read allotted to each command register.

2-4.16 Internal Register Read

RE	RS	D7	D6	D5	D4	D3	D2	D1	D0
0	1	※	※	※	※	Internal register read data			

※ mark shows "Don't care"

Command for reading out the data of the internal registers.

When this command is executed, the address for read in the internal registers to be read must be read must be preset.

2.5 Function Description

2.5.1 MPU Interface

2.5.1-1 Interface Type Selection

The LH155BA performs data transfer via the 8-bit data bus or the serial data input (the SDA or SCL pin). The parallel or serial interface is selected by setting the poiarity of the P/S pin to “H’ or “L”. When selecting serial interface, data-reading cannot be performed.
but only data writing can.

P/S	I/F type	CSB	RS	RDB	WRB	M86	SDA	SCL	Data
H	Parallel	CSB	RS	RDB	WRB	M86	-	-	D0 to D7
L	Serial	CSB	RS	-	-	-	SDA	SCL	-

2.5.1-2 Parallel input

The LH155BA allows parallel data transfer by connecting the data bus to an 8-bit
MPU
if the parallel interface is selected with the P/S pin.
For this 8-bit MPU, the 80-family or 68-family MPU type interface can be selected with the M86 pin.

M86	MPU type	CSB	RS	RDB	WRB	Data
L	80-fimily MPU	CSB	RS	RDB	WRB	D0 to D7

2.5.1-3 Data identification

The LH155BA identifies the data types over the 8-bit data bus by combinations of RS,RDB and WRB signals.

RS	80-family		FUNCTION
	WRB	RDB	
1	0	1	Read internal register
1	1	0	Write internal register
0	0	1	Read display data
0	1	0	Write display data

2.5.1-4 Serial interface

The serial interface for the LH155BA is enabled to accept the SDA and SCL inputs when the chip is selected. If the chip is not selected, the internal shift register and counter are reset to the initial state.

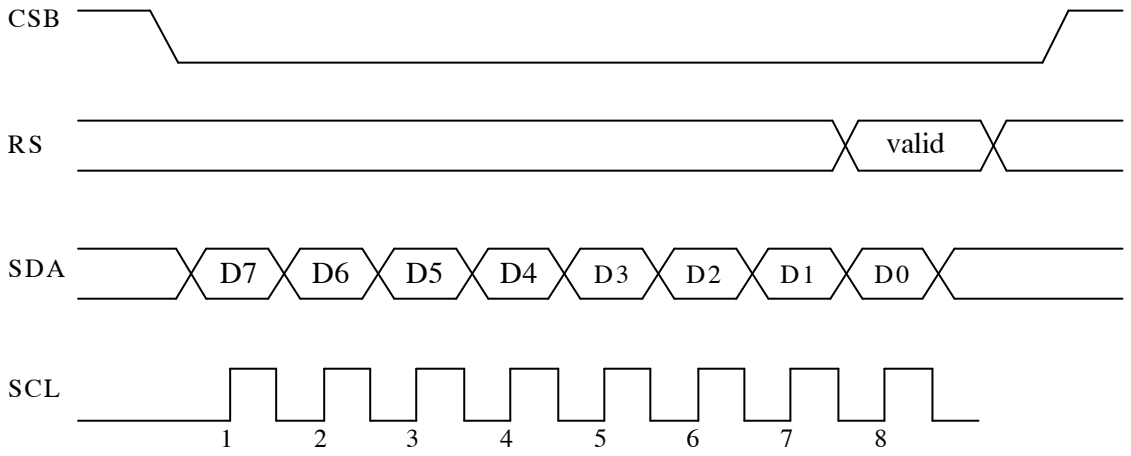
The data input is taken in the order of D7…D1, and D0 starting with the serial data input SDA when the serial clock (SCL) rises. At the leading edge of the 8th serial clock , the serial data is converted into 8-bit parallel data and then processed according to its type.

The serial data input (SDA) is identified with input at the RS pin.

The serial clock input (SCL) must be set to "L' if it is not accessed. After 8-bit data transfer is finished, it must be also set to "L".

For the SDA and SCL signals, sufficient care must be taken for external noise. In order to prevent continuous error recognition of transferred data occurring from external noise, the chip selected must be released (CSB="H") whenever 8-bit data transfer is finished.

2.5.2 Access to Display RAM and Internal Register



The LH155BA makes access to Display RAM, and internal register register by data bus D0~D7, chip select CSB is at "H", it is in non-selective state and cannot make access to Display RAM and internal registers, in making access to them , set CSB to "L".

The access to either Display RAM or internal registers can be shifted by RS input.

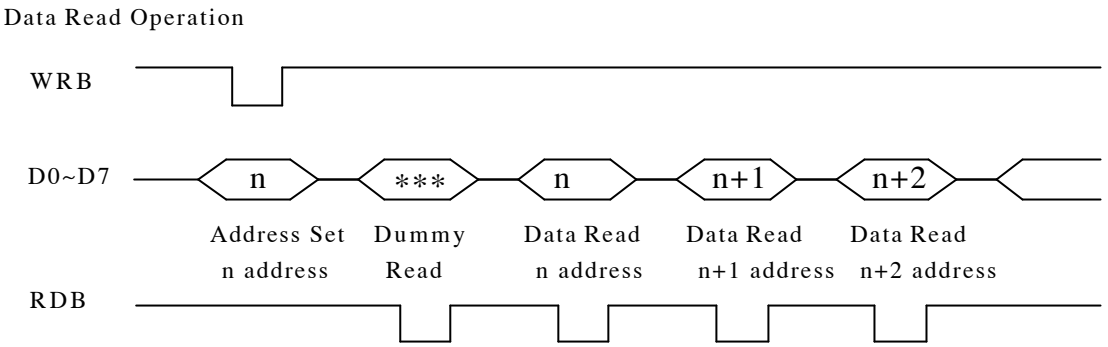
RS="L": Display RAM data

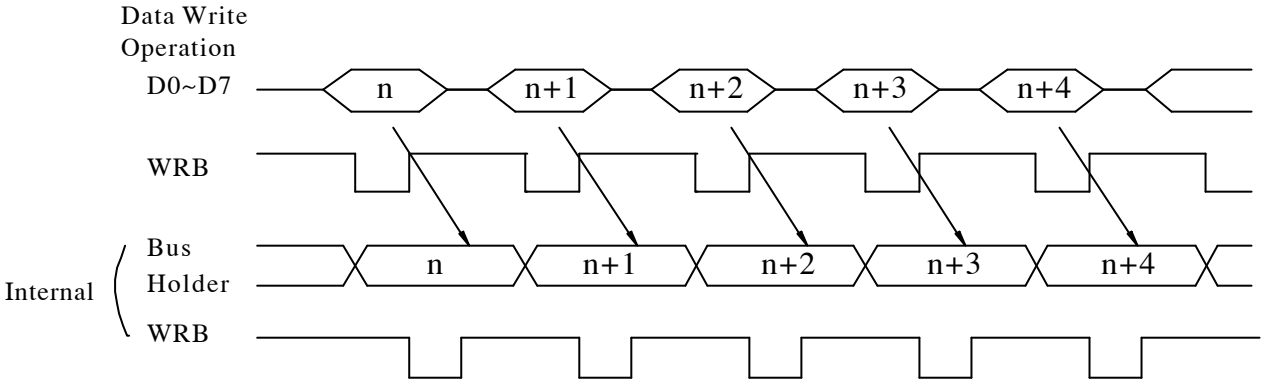
RS="H":Internal command register

The data of 8-bit data bus D0~D7 are written by write operation after address setting through MPU. The timing of Write is at the rising of WRB for 80 family MPU and at the falling of E for 68 family MPU respectively.

Write is is internally processed by placing intermediately the bus holder in the internal data bus .In case of writing data from MPU, the data are temporally held in the bus holder before they are written by the time of

the next cycle. Since the Read sequence of Display RAM data is limited, note that when Address Set is made, the designated address data are not output to Read Comman immediately after the Address Set, but are output when the second data Read, resulting in requiring dummy Read one time. Dummy Read is always requlred one time after Address Set

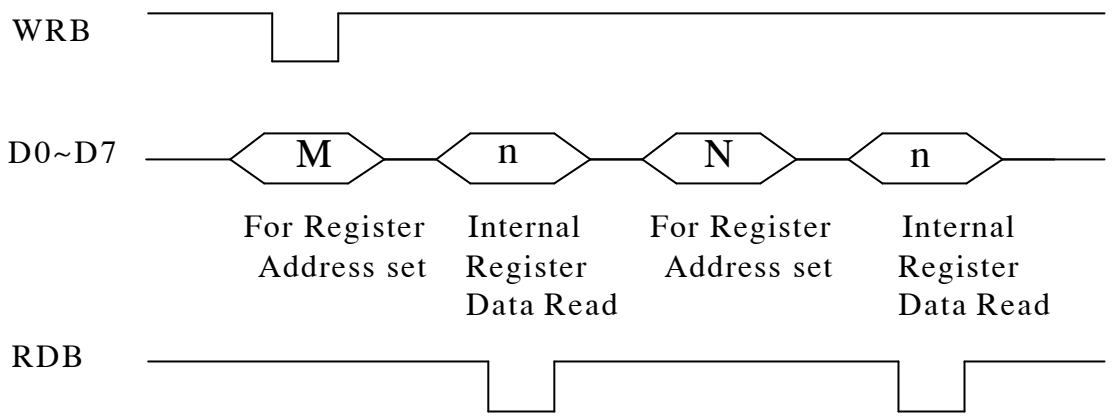




2.5.3 Read of internal Register

The LH155BA reads not only Display RAM, but also the internal registers.

Addresses for Read (0.2~E[hex])are allotted to each internal register. In reading the internal registers, the addresses of internal registers allotted to read are written in the register Read and then are read.



2.5.4 Display Mode

The LH155BA have 3 Display modes.

One is for Graphic Display mode and one is for Segment display mode and the other is for icon Display. 3 mode are independent of each other, so each mode can function alone. That can drive a minimum circuit each display mode. A suitable mode for lower current consumption is selectable.

2.5.4-1 Graphic Display Mode

This mode enable 64x128 Buit - in SRAM and 64 command x 128 segment output terminal.

Graphic Display's Memory map is below.

When Stand-by mode and Sleep mode, power supply circuit is stopped and output terminal is specified VSS level.

The Memory for Graphic Display is accessed by 8 bits at one time.

X address is from 00H to 0FH and Y address is from 00H to 3FH. (See table A)

2.5.5 Display Starting Line Register

This register is for determining display start line (usually the most upper line)

Corresponding to COM0 in case of display the Display data RAM.

The register is also used in picture-scrolling.

The 6-bit display starting address is set in this register by display starting-line setting command.

The register are preset every timing of FLM signal variation in the display line counter. The line counter counts up being synchronized with LP input and generates line addressed which read out sequentially 128-bit data from Display RAM to LCD driver circuit.

2.5.6 Addressing of Display RAM

Display RAM consists of 128 x 64 bit memory, and makes access in 8 bit unit to an address specified by X address and Y address from MPU.

The address, X and Y are possible to be set up so that can increment automatically with the address control register. The increment is made every time Display RAM is read or written from MPU.

Thought the X direction side is selected by X address while the Y direction side by Y address, 10H-FFH in the X address are inhibited and do not have the X address set in these addresses.

In the Y direction side, the 128-bit display data are internally read the display data latch circuit at the rising of LP every one line cycle, and are output from the display data latch circuit at the falling of LP.

43H-FFH in the Y address are inhibited and do mot have the Y address set in these addresses.

When FLM signals being output in one frame cycle are at "H", the value in the display starting line register are perset in the line counter and the line counter counts up at the falling of LP signals.

The display line address countr is aynchronized with each timing signal of the LCD system to operate and is independent of address counters, X and Y.

2.5.7 Display RAM Data and LCD

One bit of Display RAM data corresponds to one dot of LCD. Normal display and reverse display by REV register are set up as follows.

- Normal display (REV=0) : RAM data=”0” not lighted
  RAM data=”1” lighted
- Reverse display (REV=1) : RAM data=”0” lighted
  RAM data=”1” not lighted

2.5.8 Segment Display Output Order/Reverse Set Up

The order of display outputs, SEG0~SEG127 can be reversed by reversing access to Display RAM from MPU by using REF register, lessen the limitation in placing IC when assembling a LCD panel module.

REP																																
	=1	X=0FH								X=0EH								…			X=00H											
	=0	X=00F								X=01H								…			X=0FH											
SWAP	=1	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0			D7	D6	D5	D4	D3	D2	D1	D0	LINE				
	=0	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7			D0	D1	D2	D3	D4	D5	D6	D7	address				
00H																												00H				
01H																												01H				
02H																												02H				
03H																												03H				
04H																												04H				
05H																												05H				
06H																												06H				
07H																												07H				
08H																												08H				
3AH																												3AH				
3BH																												3BH				
3CH																												3CH				
3DH																												3DH				
3EH																												3EH				
3FH																		…										3FH				
Segment Output		SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SGE7	SEG8	SEG9	SEG10	SEG11	SGE12	SEG13	SEG14	SEG15	…		SEG120	SEG121	SEG122	SEG123	SEG124	SEG125	SEG126	SEG127					

Display start line

Common Output

COM0 COM1 COM2 COM3 COM4 COM5 COM6 COM7 COM8 … COM58 COM59 COM60 COM61 COM62 COM63

2.5.9 Display Timing Generator

The display timing generator generates a timing clock necessary for internal operation and timing pulses (LP, FLM, and M) by inputting the original oscillating clock CK or by the oscillating circuit of OSC1 and OSC0. By setting up Master/Stave mode(M/S), the state of timing pulse pins and the timing generator changes.

2.5.10 Signal Generation to Display Line Counter, and Display Data Latching Circuit

Both the clock to the line counter and latching signals to display data latching circuit from the display clock (LP) are generated.

Synchronized with the display clock, the line addresses of Display RAM are generated and 128-bit display data are latched to display-data latching circuit to output to the LCD driver circuit (SEG output).

2.5.11 Generation of the Alternated Signal (M) and the Synchronous Signal (FLM)

LCD alternated signal (M) and synchronous signal (FLM) are generated by the display clock (LP). The FLM generates alternated drive waveform to the LCD driver circuit. Normally the FLM generates alternated driver drive waveform every frame unit.

(M-signal level is reversed every one frame).

But by setting up data (n-1) in an n-line reverse register and n-line alternated command (NLIN) at “H”, n-line reverse waveform is generated.

When the LH155BA is used in multi-chip, the signals of LP, FLM, and M must be sent from Master side in the Slave operation.

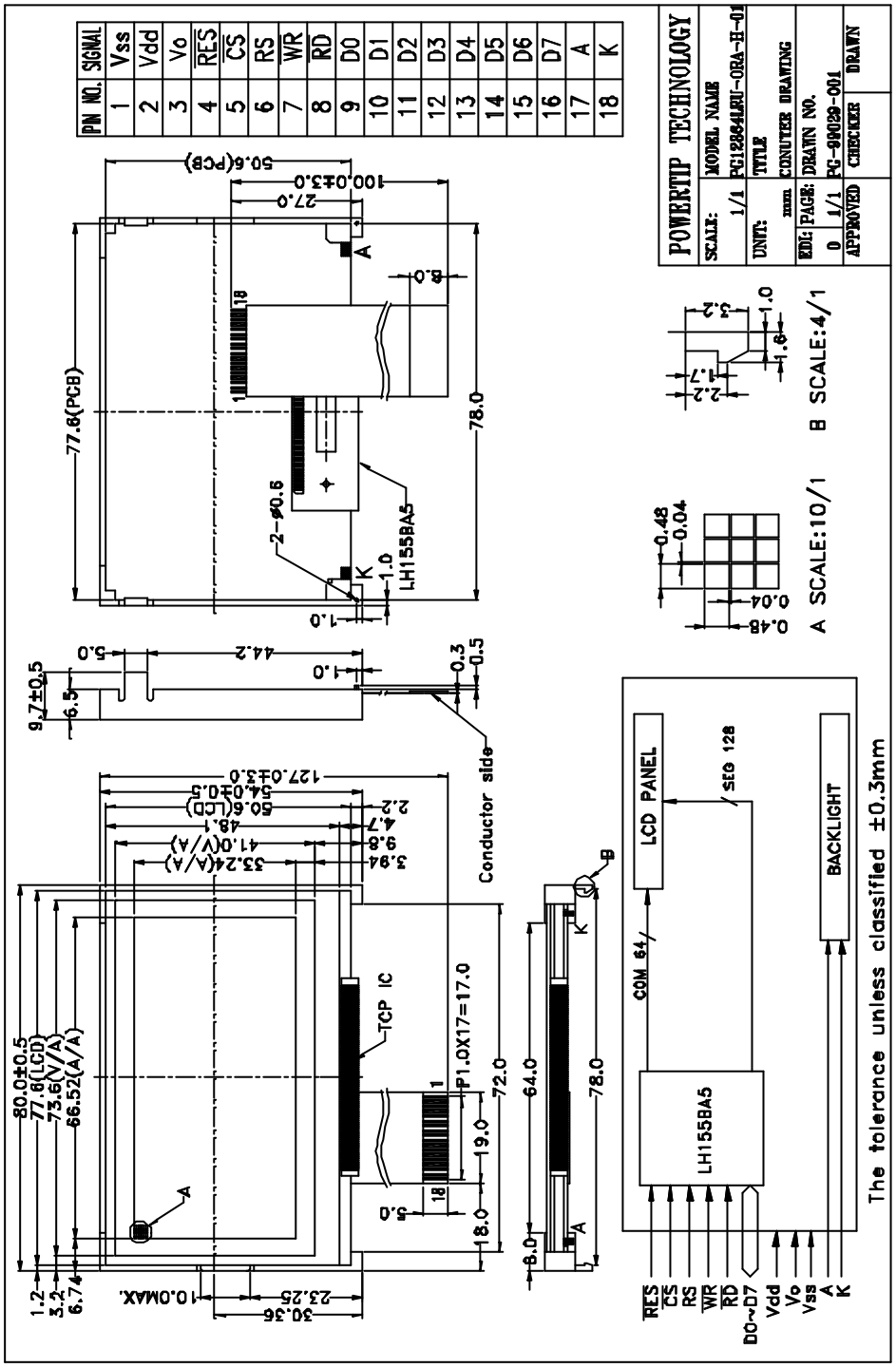
2.5.12 Display Data Latching Circuit

Display Data Latching Circuit temporary latches display data that is output display data to LCD driver circuit from Display RAM every one common period. Normal display /reverse display, display ON/OFF, and display all on command are operated by controlling data in the latch. And no data within Display RAM changes.

3. RELIABILITY

3.1 Content of Reliability Test

Environmental Test			
NO	Test Item	Content of Test	Test Condition
1	High temperature storage	Endurance test applying the high storage temperature for a long time.	70°C 100 hrs
2	Low temperature storage	Endurance test applying the high storage temperature for a long time.	-30°C 100 hrs
3	High temperature operation	Endurance test applying the electric stress (Voltage & Current) and the thermal stress to the element for a long time.	70°C 100 hrs
4	Low temperature operation	Endurance test applying the electric stress under low temperature for a long time.	-20°C 100 hrs
5	High temperature /Humidity Storage	Endurance test applying the high humidity storage for a long time.	70°C,90%RH 50 hrs
6	High temperature /Humidity Operation	Endurance test applying the electric stress (Voltage & Current) and temperature / humidity stress to the element for a long time.	70°C,90%RH 50 hrs
7	Temperature Cycle	Endurance test applying the low and high temperature cycle. -25°C → 25°C → 75°C 30min ← 5min ← 30min 1 cycle	-25°C / 75°C 10 cycle


POWERTIP TECHNOLOGY
MODEL NAME
PG12864LRU-ORA-H-01
TITLE
CONUTER DRAWING
DRAWN NO.
PG-09029-001
CHECKER
DRAWN
SCALE: 1/1
UNIT: mm
EDI: 0
PAGE: 1/1
APPROVED
PIN NO. SIGNAL
1 Vss
2 Vdd
3 Vo
4 RES
5 CS
6 RS
7 WR
8 RD
9 D0
10 D1
11 D2
12 D3
13 D4
14 D5
15 D6
16 D7
17 A
18 K
LCD PANEL
BACKLIGHT
LH155BA5
TCP IC
COM 64
SEG 128
Conductor side
A SCALE:10/1
B SCALE:4/1
The tolerance unless classified ±0.3mm