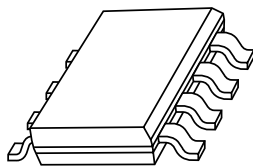


DATA SHEET



PHP222 Dual P-channel enhancement mode MOS transistor

Preliminary specification
Supersedes data of 1998 Mar 24
File under Discrete Semiconductors, SC13

1998 Apr 01

Dual P-channel enhancement mode MOS transistor

PHP222

FEATURES

- Very low on-state resistance
- High-speed switching
- No secondary breakdown
- Low threshold.

APPLICATIONS

- Power management
- DC-DC converters
- General purpose switch.

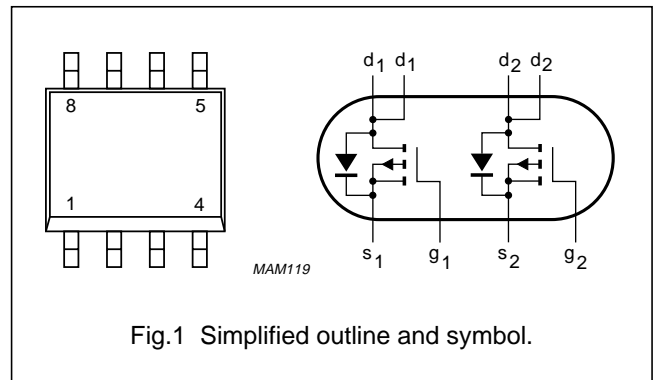
DESCRIPTION

Two P-channel enhancement mode MOS transistors in an 8-pin SOT96-1 (SO8) SMD plastic package.

CAUTION
The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

PINNING - SOT96-1 (SO8)

PIN	SYMBOL	DESCRIPTION
1	s ₁	source 1
2	g ₁	gate 1
3	s ₂	source 2
4	g ₂	gate 2
5	d ₂	drain 2
6	d ₂	drain 2
7	d ₁	drain 1
8	d ₁	drain 1



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{DS}	drain-source voltage (DC)		–	–30	V
V _{SD}	source-drain diode forward voltage	I _S = –1.25 A; V _{GD} = 0	–	–1.3	V
V _{GSO}	gate-source voltage (DC)	open drain	–	±8	V
V _{GSt}	gate-source threshold voltage	I _D = –1 mA; V _{DS} = V _{GS}	–0.4	–	V
I _D	drain current (DC)	T _s = 80 °C	–	–3.2	A
R _{DSon}	drain-source on-state resistance	I _D = –1.6 A; V _{GS} = –2.5 V	–	220	mΩ
P _{tot}	total power dissipation	T _s = 80 °C	–	3.5	W

Dual P-channel enhancement mode MOS transistor

PHP222

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per P-channel					
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{GSO}	gate-source voltage (DC)	open drain	–	±8	V
I_D	drain current (DC)	$T_s = 80\text{ °C}$; note 1	–	–3.2	A
I_{DM}	peak drain current	note 2	–	–12.8	A
P_{tot}	total power dissipation	$T_s = 80\text{ °C}$; note 3	–	3.5	W
		$T_{amb} = 25\text{ °C}$; note 4	–	2.63	W
		$T_{amb} = 25\text{ °C}$; note 5	–	1.14	W
		$T_{amb} = 25\text{ °C}$; note 6	–	1.56	W
T_{stg}	storage temperature		–55	+150	°C
T_j	operating junction temperature		–55	+150	°C
Source-drain diode					
I_S	source current (DC)	$T_s = 80\text{ °C}$	–	–2.7	A
I_{SM}	peak pulsed source current	note 2	–	–10.8	A

Notes

- T_s is the temperature at the soldering point of the drain lead.
- Pulse width and duty cycle limited by maximum junction temperature.
- Maximum permissible dissipation per MOS transistor. Both devices may be loaded up to 3.5 W at the same time.
- Maximum permissible dissipation per MOS transistor. Device mounted on a printed-circuit board with an $R_{th\ a-tp}$ (ambient to tie-point) of 27.5 K/W.
- Maximum permissible dissipation per MOS transistor. Device mounted on a printed-circuit board with an $R_{th\ a-tp}$ (ambient to tie-point) of 90 K/W.
- Maximum permissible dissipation if only one MOS transistor dissipates. Device mounted on a printed-circuit board with an $R_{th\ a-tp}$ (ambient to tie-point) of 90 K/W.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j-s}$	thermal resistance from junction to soldering point	20	K/W

Dual P-channel enhancement mode MOS transistor

PHP222

CHARACTERISTICS

$T_j = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per P-channel						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0; I_D = -10\ \mu\text{A}$	-30	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{GS} = V_{DS}; I_D = -1\ \text{mA}$	-0.4	–	–	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0; V_{DS} = -24\ \text{V}$	–	–	-100	nA
I_{GSS}	gate leakage current	$V_{GS} = \pm 8\ \text{V}; V_{DS} = 0$	–	–	± 100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5\ \text{V}; I_D = -1.6\ \text{A}$	–	–	200	m Ω
		$V_{GS} = -2.5\ \text{V}; I_D = -1.6\ \text{A}$	–	–	220	m Ω
		$V_{GS} = -1.8\ \text{V}; I_D = -0.8\ \text{A}$	–	–	250	m Ω
C_{iss}	input capacitance	$V_{GS} = 0; V_{DS} = -24\ \text{V}; f = 1\ \text{MHz}$	–	696	–	pF
C_{oss}	output capacitance	$V_{GS} = 0; V_{DS} = -24\ \text{V}; f = 1\ \text{MHz}$	–	163	–	pF
C_{rss}	reverse transfer capacitance	$V_{GS} = 0; V_{DS} = -24\ \text{V}; f = 1\ \text{MHz}$	–	73	–	pF
Q_G	total gate charge	$V_{GS} = -4.5\ \text{V}; V_{DD} = -15\ \text{V}; I_D = -1\ \text{A}; T_{amb} = 25\text{ °C}$	–	16	–	nC
Q_{GS}	gate-source charge	$V_{DD} = -15\ \text{V}; I_D = -1\ \text{A}; T_{amb} = 25\text{ °C}$	–	0.7	–	nC
Q_{GD}	gate-drain charge	$V_{DD} = -15\ \text{V}; I_D = -1\ \text{A}; T_{amb} = 25\text{ °C}$	–	4.1	–	nC
Switching times						
$t_{d(on)}$	turn-on delay time	$V_{GS} = 0\ \text{to}\ -8\ \text{V}; V_{DD} = -20\ \text{V}; I_D = -1\ \text{A}; R_{gen} = 6\ \Omega$	–	3.5	–	ns
t_r	rise time		–	4	–	ns
t_{on}	turn-on switching time		–	7.5	–	ns
$t_{d(off)}$	turn-off delay time	$V_{GS} = -8\ \text{to}\ 0\ \text{V}; V_{DD} = -20\ \text{V}; I_D = -1\ \text{A}; R_{gen} = 6\ \Omega$	–	90	–	ns
t_f	fall time		–	35	–	ns
t_{off}	turn-off switching time		–	125	–	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	$V_{GD} = 0; I_S = -1.25\ \text{A}$	–	–	-1.3	V
t_{rr}	reverse recovery time	$I_S = -1.25\ \text{A}; di/dt = 100\ \text{A}/\mu\text{s}$	–	65	–	ns

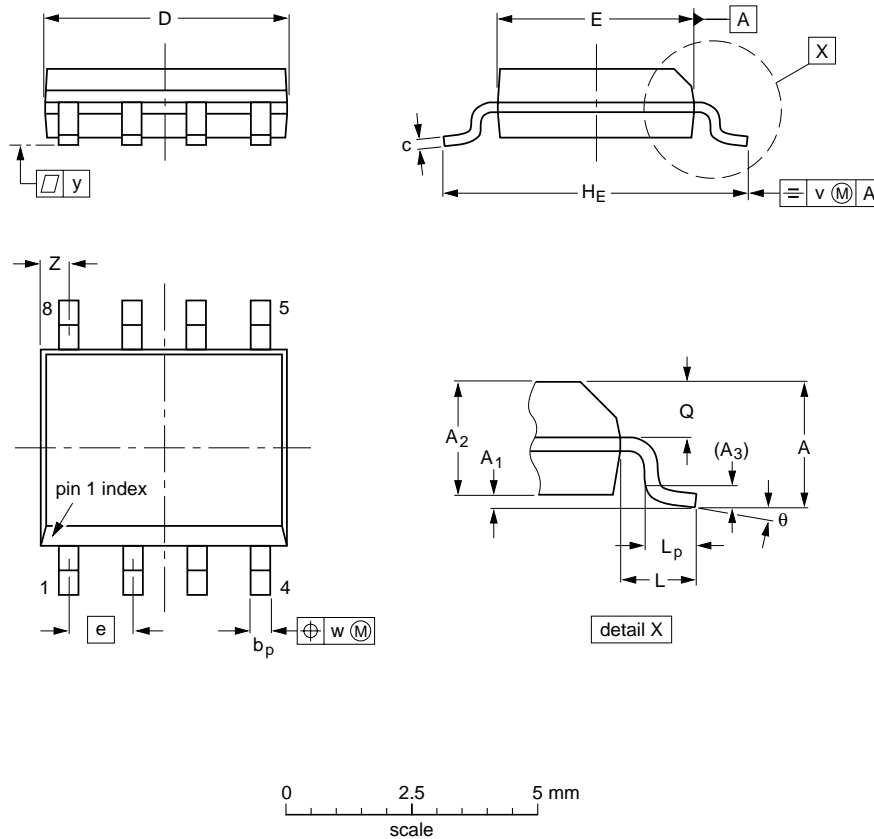
Dual P-channel enhancement mode MOS transistor

PHP222

PACKAGE OUTLINE

S08: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A _{max.}	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				95-02-04 97-05-22

Dual P-channel enhancement mode MOS transistor

PHP222

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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Dual P-channel enhancement
mode MOS transistor

PHP222

NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113, Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010, Fax. +43 160 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6, 220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor, 51 James Bourchier Blvd., 1407 SOFIA, Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS, Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre, 72 Tat Chee Avenue, Kowloon Tong, HONG KONG, Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S, Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO, Tel. +358 9 615800, Fax. +358 9 61580920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex, Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG, Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS, Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor, 254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025, Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division, Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510, Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14, Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053, TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3, 20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108, Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL, Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR, Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905, Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB, Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND, Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO, Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc., 106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI, Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA, Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW, Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762, Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale, 2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000, Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Al. Vicente Pinzon, 173, 6th floor, 04547-130 SÃO PAULO, SP, Brazil, Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA, Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM, Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH, Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1, TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd., 209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260, Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL, Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7, 252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes, MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409, Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD, Tel. +381 11 625 344, Fax. +381 11 635 777

For all other countries apply to: Philips Semiconductors, International Marketing & Sales Communications, Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

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