PI3041A Contact Image Sensor

Preliminary Data Sheet

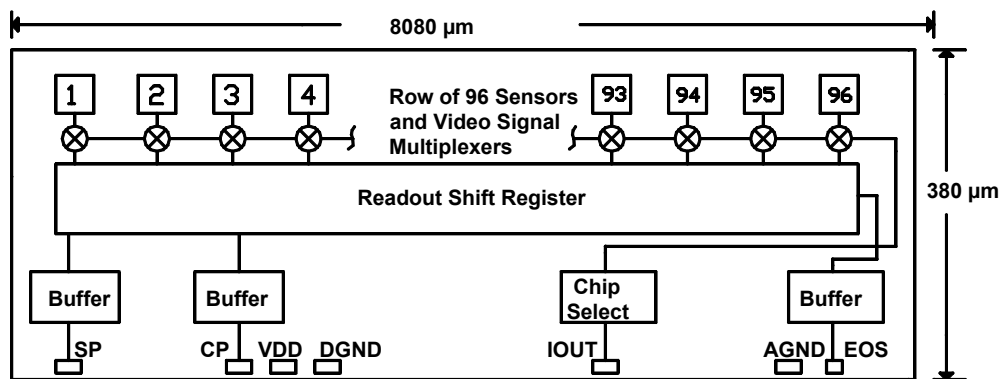## PI3041A
300DPI CIS Sensor Chip
Engineering Data Sheet

Description:

Peripheral Imaging Corporation PI3041A CIS, Contact Image Sensor, chip is a 300 dot per inch resolution, linear array image sensor chip. The sensor chip is processed using a CMOS Image Sensing Technology, a possession of ISPL (Image Sensor Product Line) group within AMIS. Designed for cascading multiple chips in a series, the image sensor chips, uses a chip-on-board process. They are bonded end-to-end on a printed circuit board (PCB). This bonding process allows the CIS module manufacturers to produce variable CIS module lengths in increments of the chip array lengths. Hence, the modules are easily applied in a large number of document scanners, found in today's facsimile market. Examples are wide format maps and architectural drawings scanners down to the narrow width scanners, such as, those found in check readers, lotto tickets, entrance gates tickets, etc. This is not to exclude the many office automation equipments, which require an even more variety in scanning widths, as well as, those with special mechanically configurations.

Figure 1 is a block diagram of the imaging sensor chip. Each sensor chip consists of 96 detector elements, their associated multiplexing switches, buffers, and a chip selector. The detector's element-to-element spacing is approximately 83.3 µm. The size of each chip without scribe lines is 8080 µm by 380 µm. Each sensor chip has 7 bonding pads. The pad symbols and functions are described in Table 1.


Figure 1. PI3041A Block Diagram

SYMBOL	FUNCTION
SP	Start Pulse: Input clock to start the line scan.
CP	Clock Pulse: Input clock to clock of the Shift Register.
VDD	Positive Supply: +5 volt supply connected to substrate.
DGND	Digital Ground: Connection topside common
IOUT	Signal Current Output: Output for video signal current
AGND	Analog Ground: Connection topside common
EOS	End of Scan Pulse: Output from the shift register at end of scan.

Table 1. Pad Symbols and Functions

Bonding Pad Outputs Locations and Die Dimensions

Figure 2 shows image sensor's die dimension and the bonding pad locations for PI3041A Sensor Chip. The location is referenced to the lower left corner of the die.
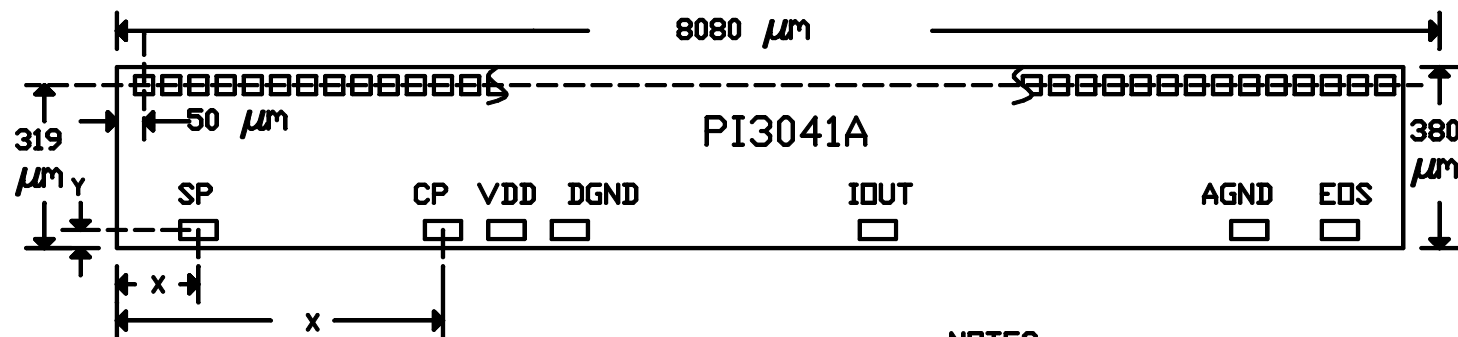
PAD	FUNCTION	Y	X
SP	START INPUT	70	928
CP	CLOCK INPUT	70	3208
VDD	+5 SUPPLY	70	3505
DGND	GROUND	70	3768
IOUT	VIDEO SIGNAL OUT	70	4922
AGND	ANALOG GROUND	70	6462
EOS	SCAN OUTPUT	70	6742

NOTES:
1. THE DRAWING IS NOT TO SCALE.
2. THE DIE LENGTH AND WIDTH ARE GIVEN AS SHOWN.
3. THE PAD LOCATION ARE GIVEN IN THE TABLE
4. THERE ARE TWO EXAMPLES OF THE X AND Y LOCATIONS SHOWN ON THE FIRST TWO PADS. THEY ARE MEASURED TO THE LEFT BOTTOM CORNER OF THE PAD OPENNING
   ALL PAD OPENNING ARE 140 X 80.
5. ALL DIMENSIONS ARE IN μm.
6. THE DOTTED LINE IS THE CENTER LINE OF SENSORS. ALONG WITH ITS VERTICAL LINE, IT LOCATES THE POSITION OFTHE FIRST SENSOR FROM THE DIE EDGE.

Figure 2. Bonding Pad and Chip Layout:

Wafer Scribe Lines Bordering The Die

Figure 3 shows the wafer scribe lines bordering the PI3041A Sensor Chip. The wafer thickness is 350µcrons.

70
μm

Scribe width

380
μm

PI3041A

SENSOR DIE
DIMENSION
PIXEL PITCH = 83.3 μm
WAFER THICKNESS = 350 μm

60
μm

8080
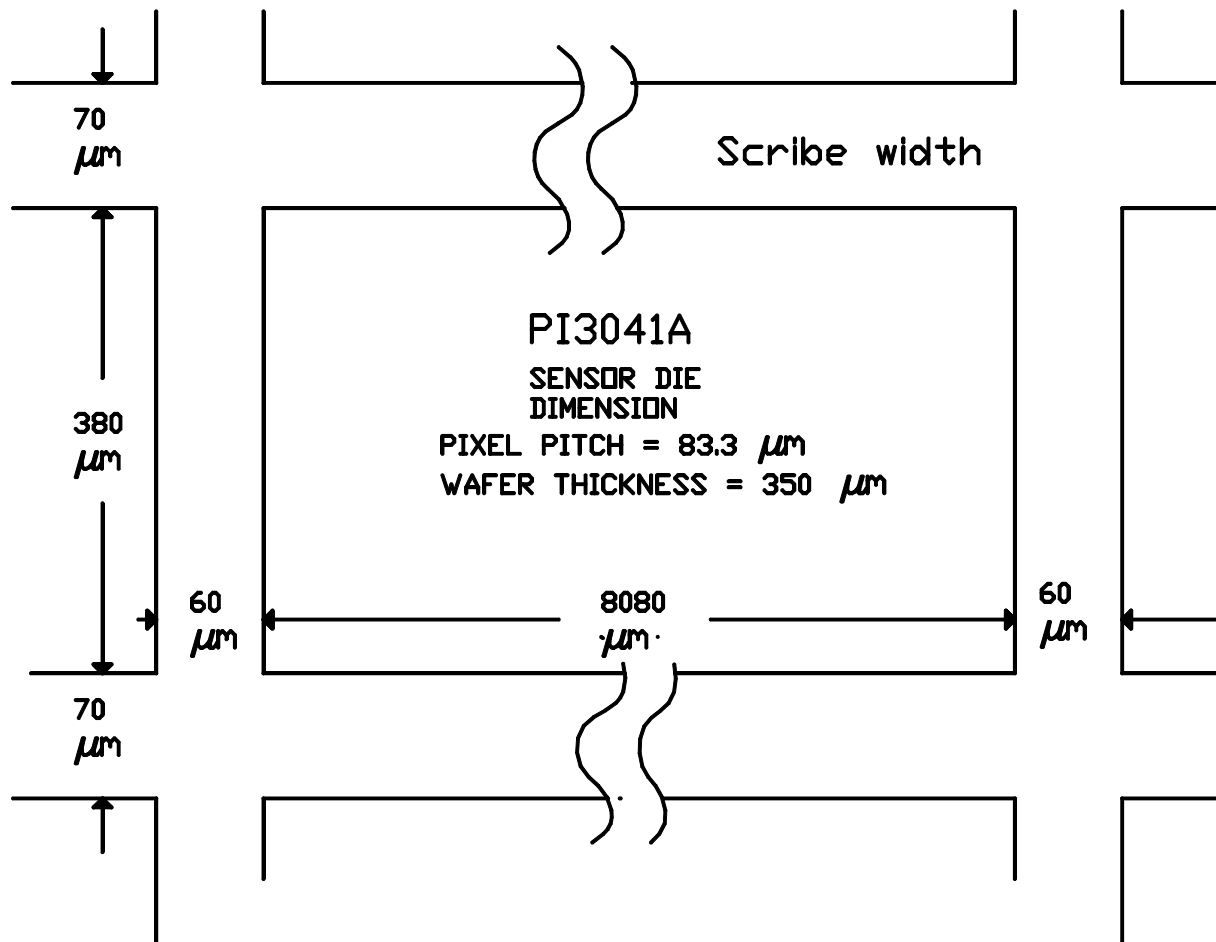μm·

60
μm

70
μm

Figure 3. Wafer Scribe Lines

Output Circuit Of The Image Sensor

The video signal from each photo-site is connected to a common video line on the sensor. Each photo-site is composed of a phototransistor with a series MOS switch connecting its emitter to a common video line. The video line is connected to the pad labeled IOUT. The photo-sites are readout upon the closure of the MOS switch, which is sequentially switched on and off by its internal scanning shift register, see Figure 1, PI3041A Block Diagram. For the clock and timing operation image sensor see Figure 7, Timing Diagram Of The PI3041A Sensor. The photo-sensing element is the base of the phototransistor where it detects and converts the light energy to proportional charges and stores them in its base and collector capacitance. When the MOS switch is activated, the emitter is connected to the video line and acts as source follower, producing an impulse current proportional to the stored charges in the base. This current is a discrete-time analog signal output called the video pixel. The charges in the video pixel are proportional to the light energy impinging in the neighborhood of its photo-sites. Figure 4, Video Pixel Output Structures, show a output structure of four photo-sites out of 128. The multiplexing MOS switch in each photo-site terminates into the output pad, IOUT, through a common video line. As the shift register sequentially accesses each photo-site the charges of the video pixel is sent to the IOUT where they are processed with an external signal conversion circuit. See the follow section, Signal Conversion Circuit.
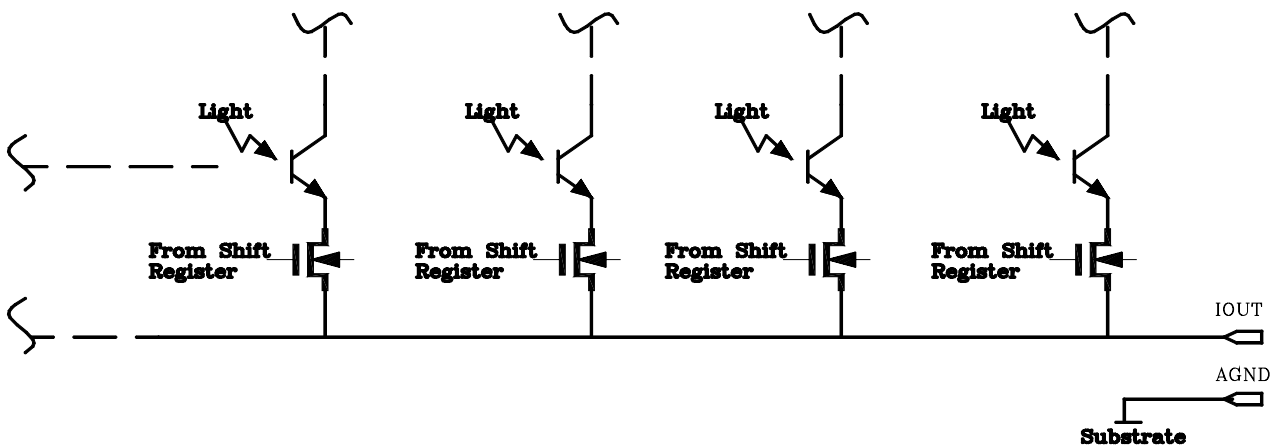

**Figure 4. Video Pixel Output Structures**

Signal Conversion Circuit

Figure 5, Video Output Test and Application Circuit is an example of the charge conversion that is used in the CIS modules. It is usually bonded on the same PCB on which the image sensors are bonded.   In applications where cost is important factor, this simply circuit provides the cleanest technique in processing the video output. It integrates all the currents from each pixel element onto a capacitor, CAP. It, also, sums the switch edge's energy along with the signal current pulses, hence minimizes the switching patterns on the video pixels. The summed charges stored on the CAP, produce a pixel voltage. Its voltage amplitude is proportional to the charge from the current pulse and the value of the CAP.
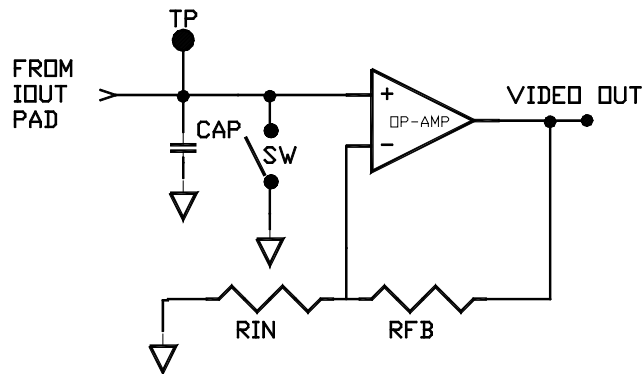
Figure 5. Video Output Test and Application Circuit

Since switching energies are high frequencies components, they tend to integrate to a 0 value and the remainder adds a constant value to offset the dark level. After the pixel is integrated, the CAP is reset to zero volts by activating the shunt switch, SW, that connects the video line to ground prior to accessing the following pixel element. As it is seen, depicting a typical pixel voltage waveform, in Figure 6, Single Pixel Output Voltage, the shunt time is controlled with CP. Simultaneous to SW activation, the pixel element storage is, also, reset to the dark reference level, hence initializing the pixel for its integration process cycle. The signal pixels Vp(n) is referenced to its Dark Level as it is seen in Figure 6.
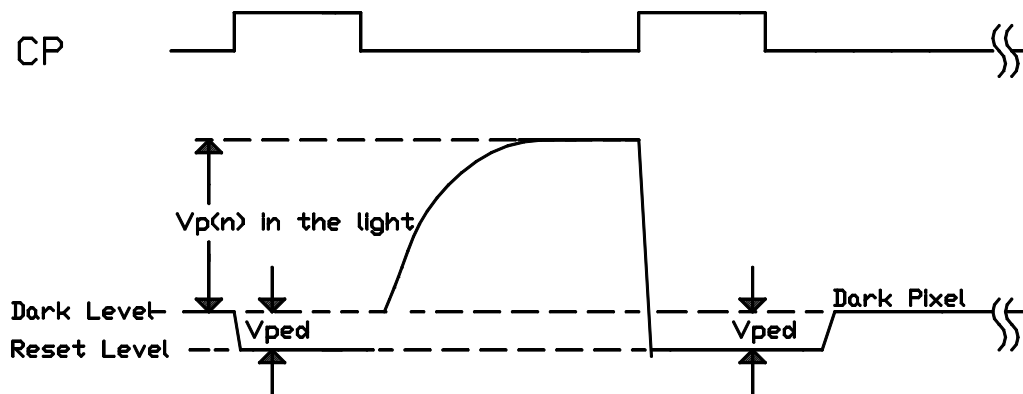
Figure 6. Single Pixel Video Output

Two Test Setups For Specifications And Performance

First Setup: The standard specifications are the image sensor tests that are performed on the wafer probe machine where each device on the wafer is tested in production. However, the data in these measurements are measured with a clock frequency at a fixed 500 KHz. Since the pixel rate is equal to the clock rate, the pixel rate is also at 500KHz. The specification under the section Electro-Optical Characteristics (25º C) is the wafer probe specifications, Table 2.

Second Setup: The CIS modules made with these devices operate in excess of 5.0 MHz. Accordingly the wafer probe specifications are supplemented with high frequency clocking performance using an A6 length module's PCB board.

Electro-Optical Characteristics (25° C)

The electro-optical characteristics of PI3041A imaging sensor chip are listed in Table 2. This is the wafer probe specification used to tests the each die at 25° C.

Parameters	Symbols	Typical	Units	Notes
Number of Photo-elements		128	elements	
Pixel-to-pixel spacing		~83.3	μm	
Line scanning rate	Tint [1]	128/Fclk	μs/line	
Clock frequency	Fclk [2]	500	KHz	See note 2 for higher clock speed. (maximum 5 MHz)
Output voltage	Vpavg [3]	1.85 ± 0.35	V	
Output voltage non-uniformity	Up [4]	± 7.5	%	
Dark output voltage	Vd [5]	<100	mV	
Dark output non-uniformity	Ud [6]	<100	mV	
Adjacent Pixel non-uniformity	Upadj [7]	<6.5	%	
Chip-to-chip non-uniformity	Ucc [8]	± 5	%	

Table 2. Electro-Optical Characteristic

Notes: (1)   Tint stands for the line scanning rate or the integration time. It is determined by the time interval between two start pulses, where the start pulses start the line-scan process, as soon as, CP, module clock, acquires it and shifts it into the internal shift register. The minimum integration time in one line scan of the sensor is number of pixel sites divided by its clock frequency. In a CIS module it is the number of sensors times the number of pixel in the sensor, all over the clock frequency. Tint in the wafer probe is set with the calibration procedure use to set the amplitude of Vpavg, see note (3).

(2)   Fclk is the device's clock, CP, frequency and it is, also, equal to the pixel rate. In the wafer test Fclk is set to 500 KHz. However, PIC (recently acquired by AMIS) has been successfully mass-producing high frequency CIS modules, using only the wafer test to qualify them. Hence, the devices are constantly tested for their standard high-speed performance with each A6 modules in production. These module production tests as proven that the low speed wafer probe tests are sufficient to produce reliable image devices.

(3)   Vpavg = ΣVp(n)/Npixels (average level in one line scan).
Where Vp(n) is the amplitude of nth pixel in the sensor chip and Npixels is the total number of pixels in sensor chip. Vpavg is converted from impulse current video pixel into a voltage output. See Figure 4, <u>Video Pixel Output</u> in section <u>Output Circuit Of The Image Sensor</u> and Figure 5, <u>Video Output Test and Application Circuit</u> in section <u>Signal Conversion Circuit</u> on page 6 and 7. There Is a calibration procedure to calibrate Vpavg using Tint as variable to control the exposure. Hence, Vpavg is calibrated for each image

sensor type to compensate for the probe card variations, as well as, the interfacing circuits to the wafer probe machine.

(4)   Up is the uniformity specification, measured under a uniform exposing light exposure. Up = [Vp(max) - Vpavg] / Vpavg x 100% or [Vpavg - Vp(min)] / Vpavg} x 100%, whichever is greater.

Where   Vp(max) is the maximum pixel output voltage in the light.
Vp(min) is the minimum pixel output voltage in the light.
The pixel Vp(n) is one n^{th} pixel in Npixels in the sensor.

(5)   Vd =   Vp(n)/Npixels. Where Vp(n) is the pixels signal amplitude of the nth pixel of the sensor. Dark is where light is off, leaving the image surface unexposed.

(6)   Ud = Vdmax – Vdmin.

(7)   Upadj = MAX[| (Vp(n) - Vp(n+l) | / Vp(n)) x 100%. Upadj is the nonuniformity in percentage. It is the amplitude difference between two neighboring pixels.

(8)   Ucc is the uniformity specifications, measured among the good die on the wafer. Under uniform light exposure the sensors are measured and calculated with following algorithm: Vpavg of all the good dies on the wafer are averaged and assigned VGpavg. Then the die with maximum Vpavg is assigned Vpavg(max), and the one with minimum Vpavg is assigned Vpavg(min). Then UCC = {[Vpavg(max)-Vpavg(min)]/VGpavg}x100.

Measuring The Device's High Frequency Performances

The PI3041A devices were tested on an A6 length standard CIS module's PCB. Thirteen sensors bonded on the PCB board along with its support circuits, such as, clock buffer circuits, the shunt switch, SW, and its amplifier. The board's video line capacitance, input capacitance of SW and input capacitance of the amplifier become part of the CAP. The A6 PCB was selected because together with the shunt switch, SW, and with its amplifier input, the video line had a typical value of ~100pf including its stray from its PCB copper traces. Another reason for this selection is that when the PI3041A wafer probe are tested, they use similar circuits to those as previously discussed under the section Signal Conversion Circuits.

By removing RIN, the amplifier gain is set to one. Then with the total value of CAP at ~100pf the Video Pixels Voltage amplitude gives a measure of the approximate Pixel charge. Note the amplifier is a 1:1 buffer amplifier that serves to isolate the video line from the measuring instruments. Further note that when the modules are produced, RIN is in the circuit as variable resistor. Then, in production of the CIS modules, the video output amplitude, Vpavg, can be adjusted to the module's specified level. This factory adjust is required because the exposure is fixed (Exposure = Light Power X Time). Example, the module's light power is fixed and integrations time, Tint, is fixed. Note Tint is fixed in accordance to users requirement, or specified for factory adjustment procedure during production. In either case, the light exposure is fixed. Accordingly, to adjust the voltage amplitude to the specified level, RIN is used.

Since the sensor response vary as a function of color, the PI3041A is measured with a Yellow-Green LED light source, as well as, the Red (660 nm) LED light source. The light sources were selected because historically, these LED light bars were used in the CIS industry and accepted in the low-cost CIS markets. Today, the users are turning towards the Light Guides or Light Pipes as the costs have been reducing and the image sensor's technology continually improves. Yet, in low-cost applications

and, especially in mid-size volume production, the LED light bars and the older image sensors persistently continue to be in demand by the scanning industry.

The high frequency performance specifications are graphical curves showing the video output, Vpavg, response to its applied light exposure. Although four exposure response graphs serve as good design reference for the designer who have prior knowledge of the image power that will be exposing the image sensors, this is not always the case, example, in designing and producing a CIS module. So to this end, the A6 PCB board, used to characterize the light exposure to video response specification, is enclosed in its A6 module housing and measured for its standard CIS parameters. These modules were fabricated exactly as their production counter part, except that the gain of the amplifier is set one. The measurements were conducted with two different LED bars, one Yellow-Green and the other Red.

Video Output Response Under Exposure

The four video signal output as function of light exposure are given in Graphs, A, B, C and D. The measurements are conducted in Black Box that enclosed the light source, the PCB and the instrument to measure the light power. The LED source mounted at the top radiated its light energy directly on the image sensor of the A6 PCB that is lying flat at the bottom of box. The video output was measured at the amplifier output of the A6 PCB. The PCB setup condition is described under the section, Measuring The Device's High Frequency Performance. Note the gain of the amplifier is set to one. Also the clock duty cycle is set to 25% for the 2.0 MHz clock frequency and set to 50% for the 5.0 MHz.
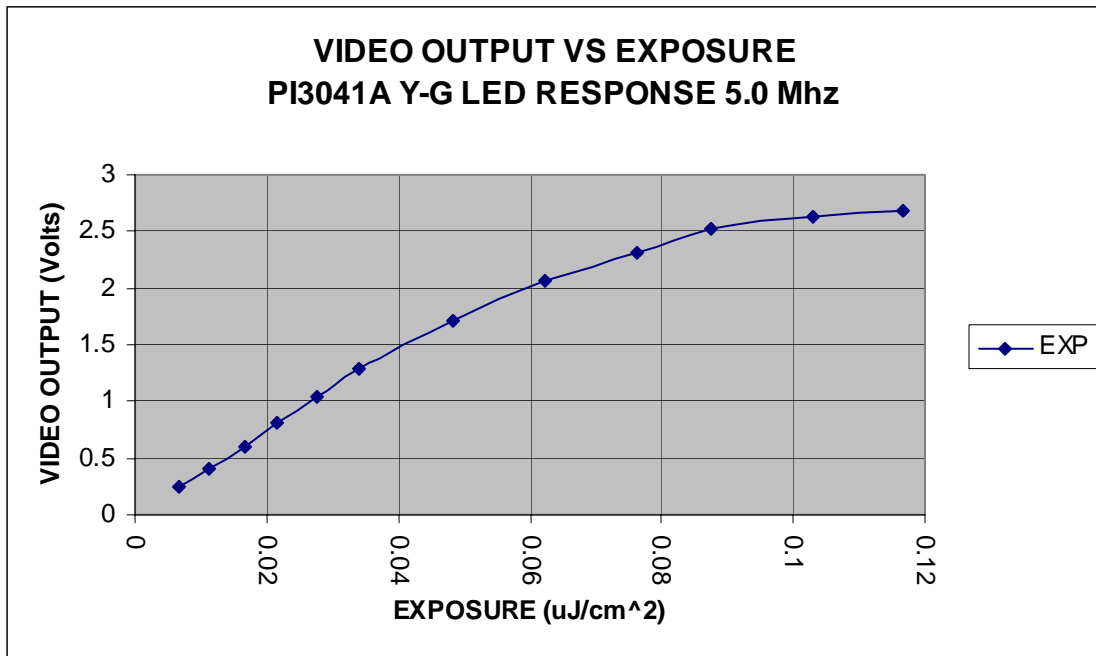

VIDEO OUTPUT VS EXPOSURE
PI3041A RED LED RESPONSE 2.0 Mhz
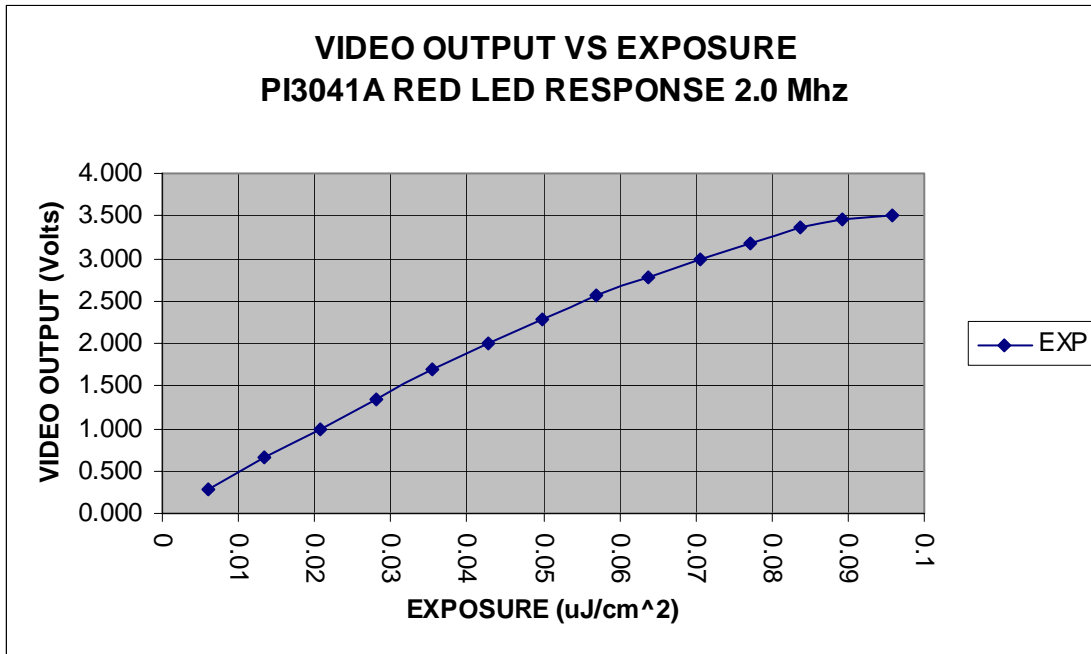
Graph A. A typical Video Output a as function of Light Exposure
Illuminated with a RED 660 nm LED Source with the PI3041A clocked at 2.0 MHz

VIDEO OUTPUT VS EXPOSURE
PI3041A Y-G LED RESPONSE 2.0 Mhz
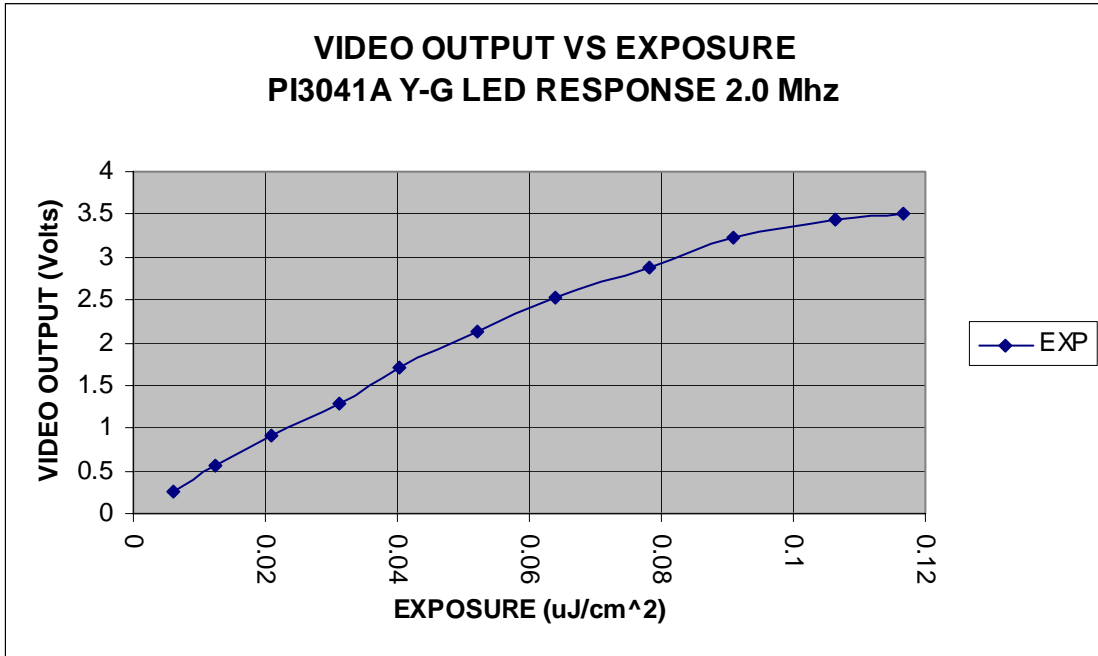
Graph B. A typical Video Output a as function of Light Exposure
Illuminated with a Y-G LED Source with the PI3041A clocked at 2.0 MHz

VIDEO OUTPUT VS EXPOSURE
PI3041A RED LED RESPONSE 5.0 Mhz
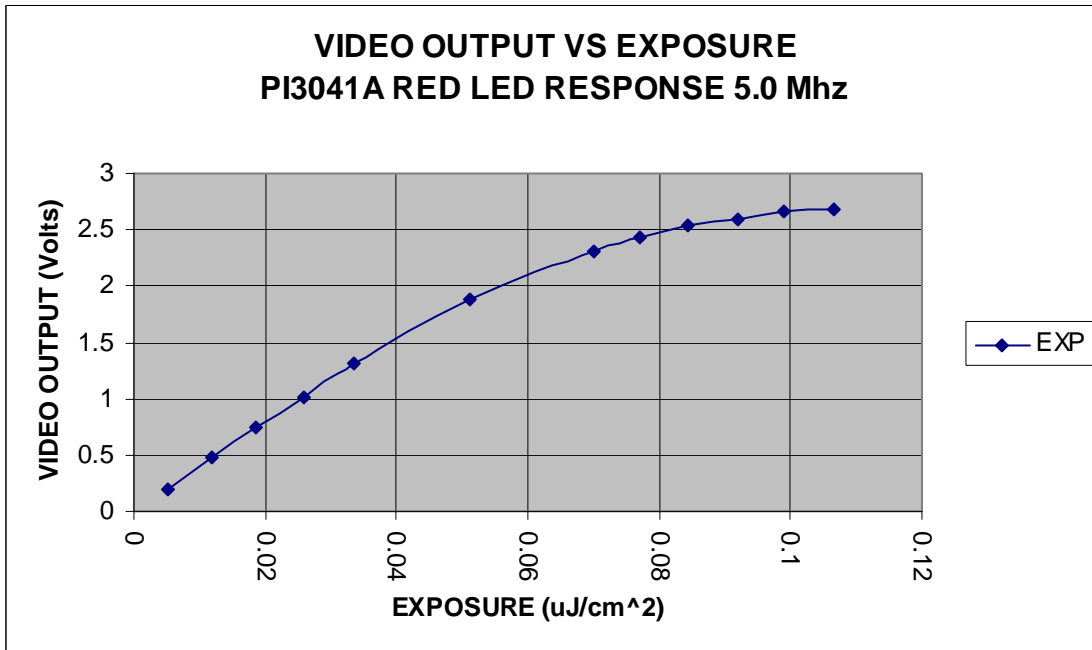
Graph C. A typical Video Output a as function of Light Exposure
Illuminated with a RED 660 nm LED Source with the PI3041A clocked at 5.0 MHz

VIDEO OUTPUT VS EXPOSURE
PI3041A Y-G LED RESPONSE 5.0 Mhz

Graph D. A typical Video Output a as function of Light Exposure
Illuminated with a Y-G LED Source with the PI3041A clocked at 5.0 MHz

A6 Module With PI3041A High Frequency Specifications

RED 660 LED Bar, A6 PCB In A6 Module Housing, At 2.0 MHz CLOCK				
Parameters	Symbols	Typical	Units	Remarks
Line scanning rate	Tint [1]	627	μs/line	13 dies in the scan. see note 1. (Bottom of Table 6)
Clock frequency	Fclk [2]	2	MHz	
Output voltage	Vpavg [3]	1.1	V	Amplifier Gain = 1.0, see note 3
Output voltage non-uniformity	Up [4]	$\pm$ 20	%	LED bar non-uniformity, see note 4.
Dark output voltage	Vd [5]	<25	mV	
Dark output non-uniformity	Ud [6]	<15	mV	
Adjacent Pixel non-uniformity	Upadj [7]	<20	%	
LED Bar Input Voltage	VLED [8]	5.0	V	LED Power Varies greatly. See note 8.
LED Bar Input Current	ILED [8]	90	mA	LED Power Varies greatly. See note 8.

Table 3. Electro-Optical Characteristic At High Frequency

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RED 660 LED Bar, A6 PCB In A6 Module Housing, At 5.0 MHz CLOCK				
Parameters	Symbols	Typical	Units	Remarks
Line scanning rate	Tint [1]	251	μs/line	13 dies in the scan. see note 1. (Bottom of Table 6)
Clock frequency	Fclk [2]	5	MHz	
Output voltage	Vpavg [3]	0.5	V	Amplifier Gain = 1.0, see note 3
Output voltage non-uniformity	Up [4]	$\pm$ 20	%	LED bar non-uniformity, see note 4.
Dark output voltage	Vd [5]	<190	mV	
Dark output non-uniformity	Ud [6]	<80	mV	
Adjacent Pixel non-uniformity	Upadj [7]	<20	%	
LED Bar Input Voltage	VLED [8]	5.0	V	LED Power Varies greatly. See note 8.
LED Bar Input Current	ILED [8]	90	mA	LED Power Varies greatly. See note 8.

Table 4. Electro-Optical Characteristic At High Frequency

Y-G LED Bar, A6 PCB In A6 Module Housing, At 2.0 MHz CLOCK				
Parameters	Symbols	Typical	Units	Remarks
Line scanning rate	Tint [1]	627	μs/line	13 dies in the scan. see note 1. (Bottom of Table 6)
Clock frequency	Fclk [2]	2	MHz	
Output voltage	Vpavg [3]	0.150	V	Amplifier Gain = 1.0, see note 3
Output voltage non-uniformity	Up [4]	$\pm$ 20	%	LED bar non-uniformity, see note 4.
Dark output voltage	Vd [5]	<30	mV	
Dark output non-uniformity	Ud [6]	<15	mV	
Adjacent Pixel non-uniformity	Upadj [7]	<20	%	
LED Bar Input Voltage	VLED [8]	5.0	V	LED Power Varies greatly. See note 8.
LED Bar Input Current	ILED [8]	380	mA	LED Power Varies greatly. See note 8.

Table 5. Electro-Optical Characteristic At High Frequency

Y-G LED Bar, A6 PCB In A6 Module Housing, At 5.0 MHz CLOCK				
Parameters	Symbols	Typical	Units	Remarks
Line scanning rate	Tint [1]	251	μs/line	13 dies in the scan. see note 1. (Bottom of Table 6)
Clock frequency	Fclk [2]	5	MHz	
Output voltage	Vpavg [3]	0.080	V	Amplifier Gain = 1.0, see note 3

Output voltage non-uniformity	Up [4]	25	%	LED bar non-uniformity, see note 4.
Dark output voltage	Vd [5]	<180	mV	
Dark output non-uniformity	Ud [6]	<60	mV	
Adjacent Pixel non-uniformity	Upadj [7]	<20	%	
LED Bar Input Voltage	VLED [8]	5.0	V	LED Power Varies greatly. See note 8.
LED Bar Input Current	ILED [8]	380	mA	LED Power Varies greatly. See note 8.

Table 6. Electro-Optical Characteristic At High Frequency

Notes: (1)   Note 1 under Table 2, <u>Electro-Optical Characteristic</u> is valid definition, except that the A6 modules has 13 sensors sequentially cascaded, hence, Tint = (13X96)/Fclk is the minimum integration time.

(2)   Fclk is the module's clock, CP, frequency and equal to the pixel rate. Also, the clock duty cycle is set to 25% for the 2.0 MHz clock frequency and set to 50% for the 5.0 MHz.

(2) $Vpavg = Vp(n)/Npixels$ (average level in one line scan).
Where $Vp(n)$ is the amplitude of nth pixel in one line scan of the modules. Npixels is the total number of pixels in the module, i.e., 13 die x 96 pixels. The amplitude of Vpavg is adjusted with RIN (which are installed in the production module) on all of CIS modules because of variations caused by the LED light sources. The low-cost production LED's light power are known to vary as much as ± 30%.

(4)   Up is the uniformity specification, measured under a uniform exposing light exposure. $Up = [Vp(max) - Vpavg] / Vpavg$ x 100% or $[Vpavg - Vp(min)] / Vpavg$} x 100%, whichever is greater.
Where $Vp(max)$ is the maximum pixel output voltage in the light.
$Vp(min)$ is the minimum pixel output voltage in the light.
The pixel $Vp(n)$ is one n^{th} pixel in Npixels in the sensor.
In applying the Up definition, Npixels must change. It must include 13 sensors, or 13x96 pixels.
Additionally, because the low-cost LED power variation can be high as ± 30%, the non-uniformities may varies as much as ± 30%. Hence the uniformities are worst because of the LED Bar CIS modules.

(5) $Vd = Vp(n)/Npixels$. Where $Vp(n)$ is the pixels signal amplitude of the nth pixel of the sensor. Dark is where light is off, leaving the image surface unexposed.

(6) $Ud = Vdmax - Vdmin$.

(7) $Upadj = MAX[| (Vp(n) - Vp(n+l) | / Vp(n)) $ x 100%. Upadj is the nonuniformity in percentage. It is the amplitude difference between two neighboring pixels.

(8)   The low-cost LED light powers are widely specified, worst case as high as ± 30%, hense, the requirement for the Vpavg Gain Control and the wide Up specifications.

Sensor's Operational Specifications

Absolute Maximum Ratings:

Parameters	Symbol	Maximum Rating	Units
Power Supply Voltage	VDD	10	Volts
Power Supply Current	IDD	<2.0	ma
Input clock pulse (high level)	Vih	Vdd + 0.5	Volts
Input clock pulse (low level)	Vil	-0.25	Volts
Operating Temperature	Top	0 to 50	^{o}C
Operating Humidity	Hop	10 to 85	RH %
Storage Temperature	Tstg	-25 to 75	^{o}C
Storage Humidity	Hstg	10 to 90	RH %

Table 7. Absolute Maximum Ratings

Recommended Operating Conditions at Room Temperature

Parameters	Symbol	Min.	Typical	Max.	Units
Power Supply	VDD	4.5	5.0	5.5	Volts
Input clock pulses high level	Vih [1]	3.0	5.0	VDD	Volts
Input clock pulse low level	Vil [1]	0	0	0.8	Volts
Operating high level exposed output	IOUT [2]		See note.		
Clock Frequency	Fclk [3]	0.1	2.0	5.0	MHz
Clock pulse duty cycle	Duty [4]		25		%
Clock pulse high durations	tw		0.125		μsec
Integration time	Tint		0.864	10	ms
Operating Temperature	Top		25	50	^{o}C

Table 8. Recommended Operating Condition At Room Temperature

Note   (1)   Applies to both CP and SP.
      (2)   The output is a current that is proportional to the charges, which are integrated on the phototransistor's base via photon-to-electron conversion. For its conversion to voltage pixels see Figure 4, <u>Video Pixel Output Structure</u> in section <u>Output Circuit Of The Image Sensor</u>.
      (3)   Although the clock frequency, Fclk, will operate the device at less than 100KHz, it is recommended that the device be operated above 500KHz to avoid complication of leakage current build-up. In applications using long CIS module length, such as an array of image sensor > 27, increases the readout time, i.e., increases Tint, hence, leakage current build-up occurs.
      (4)   The clock duty cycle typically is normally set to 25 %. However, it can operate with duty cycle as large as 50 %, which will allow more reset time at the expense of video pixel readout time. At clock frequencies approaching 5.0 MHz it is recommended to use 50% duty cycle to allow more time for the signal pixel to integrate and settle.

Switching Characteristics @ 25° C.

The timing relationships of the video output voltage and its two input clocks the start pulse, SP, and the shift register clock, CP, along with the shift register EOS output clock are shown in Figure 7, Timing Diagram Of The PI3041A Sensor. The switch timing specification for the symbols on the timing diagram is given in Table 9, Timing Symbol's Definition below the timing diagram. The digital clocks' levels are +5 Volts CMOS compatible. The video, IOUT, is defined in Figure 4, Video Pixel Output in section Output Circuit Of The Image Sensor.
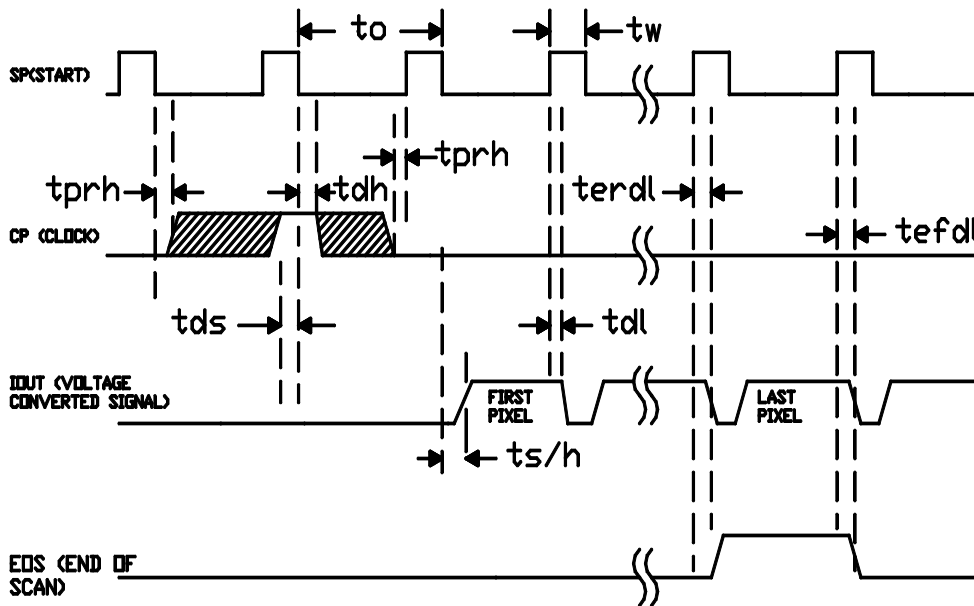
Figure 7. Timing Diagram Of The PI3041A Sensor

Item	Symbol	Minimum	Mean	Maximum	Units
Clock cycle time	to	200		10000	ns
Clock pulse width[1]	tw	50			ns
Clock duty cycle		25	50	75	%
Data setup time	tds	20			ns
Data hold time	tdh	20			ns
Prohibit crossing time[2]	tprh		20		ns
EOS rise delay	terdl		60		ns
EOS fall delay	tefdl		70		ns
Signal delay time[3]	tdl		20		ns
Signal settling time[3]	ts/h		120		ns

Table 9. Timing Symbol's Definition

Notes (1)   The clock pulse width, tw, varies with frequency, as well as, the duty cycle.

(2) Prohibit crossing time is to insure that no two start pulses are locked into the shift register for any single scan time. Since the start pulse is entered into the shift register during its active high level when the CP clock edges falls, the active high of the start pulse is permitted only during one falling, CP, clock edges for any given scan. Otherwise, multiple start pulses will load into the shift register.

(3) Pixel delay times and settling time depend on the output amplifier, which is employed. These values, tdl and ts/h, are measured with the amplifier see in Figure 8. Typical A6 CIS Module Circuit using the PI3041A sensors. Note, the impulse signal current out of the device has pulse width ~ 30 ns. Hence, the faster the amplifier with a faster settling time will yield a signal video pulse with faster rise and settle times.

Typical A6 CIS Module Circuit

See Figure 8. Typical A6 CIS Module Circuit using the PI3041A sensors. The circuit is provided as reference to illustrate the interconnection of the PI3041A for a serially cascaded line of image sensors. It is a typical A6 size CIS module produced by PIC. It provides the first time user with additional insight for designing a CIS module and supplements the circuit descriptions given in the section, Signal Conversion Circuit.

The difference is in the arrangement of the two shunt switches, U3D, and U3A. U3D is a counterpart to SW in Figure 5. Video Output Test and Application Circuit. A DC restoration capacitor, C20, with value of 500pf added between the shunts switch. The first, U3D, clamps the video line to ground to reset the image sensors. Simultaneously the second, U3A, clamps the node between C15 and amplifier input to an output reference bias voltage that is on the node between R4 and R9. These resistors are voltage divider that sets the DC operating level of the amplifier's output by applying same bias voltage to both inputs of the amplifier

(See next page for the Typical A6 CIS Module Circuit.)

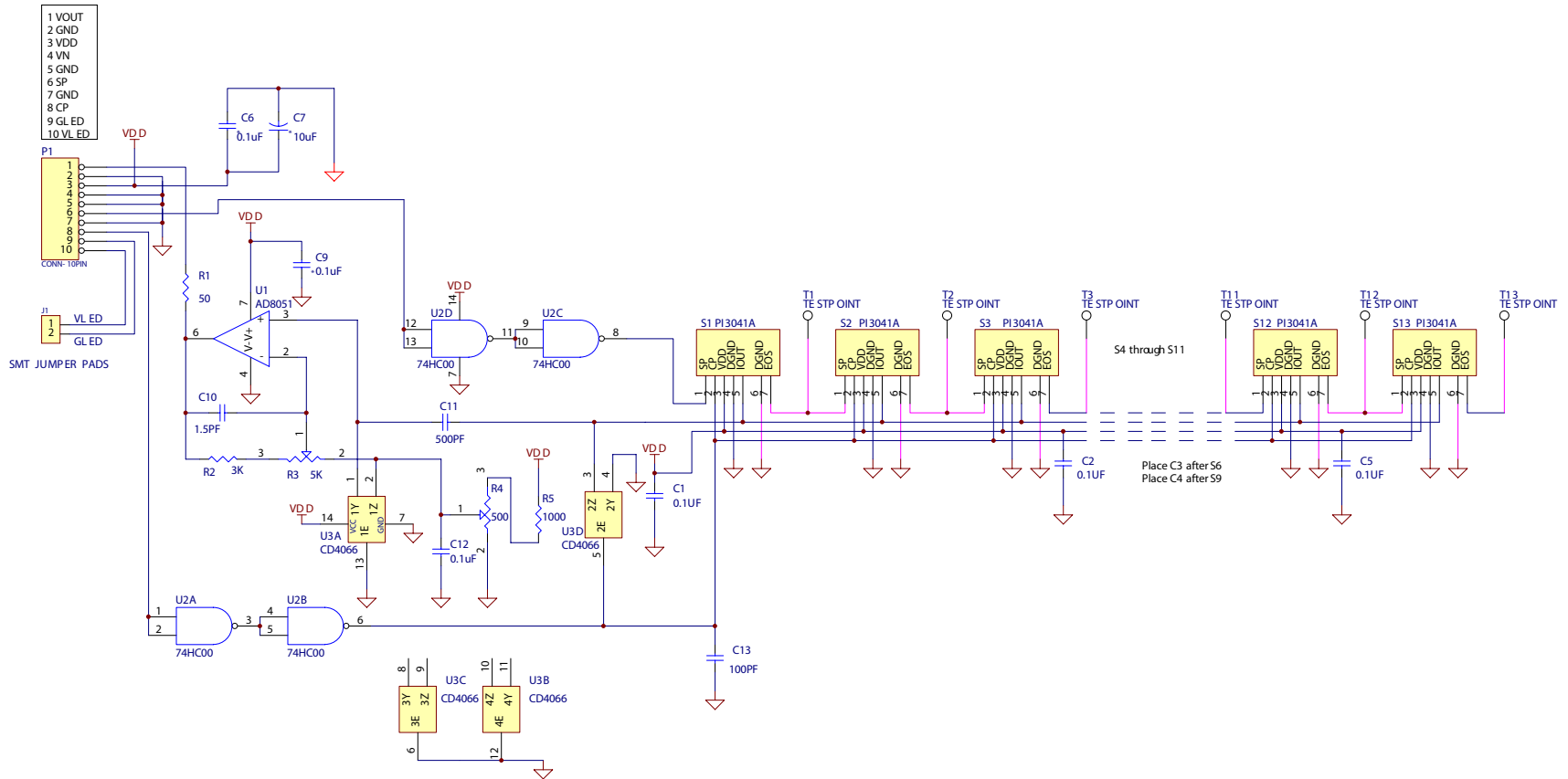Figure 8. Typical A6 CIS Module Circuit