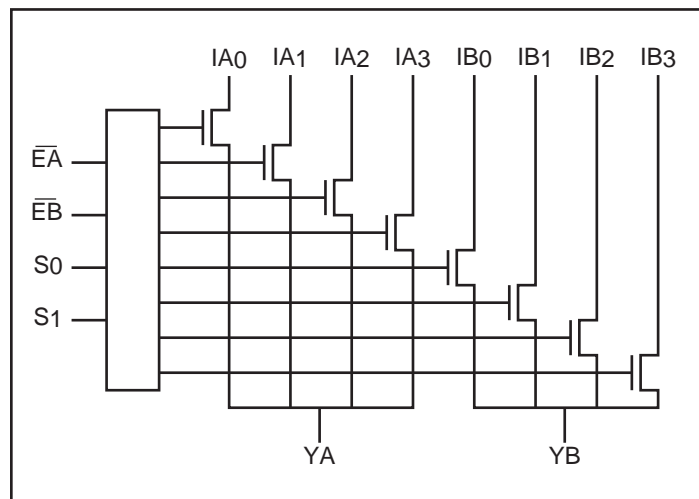
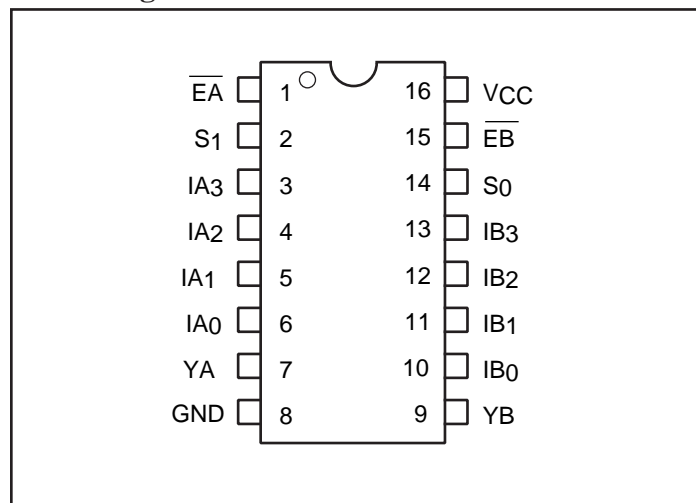


Dual 4:1 Mux/DeMux Bus Switch
Features

- Near-Zero propagation delay
- 5Ω switches connect inputs to outputs
- Direct bus connection when switches are ON
- ESD Protection up to 2kV HBM
- Ultra Low Quiescent Power (0.2μA typical)
 - Ideally suited for notebook applications
- Pin compatible with 74 series 253 logic devices
- Packaging (Pb-free & Green available):
 - 16-pin 150-mil wide plastic QSOP (Q)
 - 16-pin 173-mil wide plastic TSSOP (L)
 - 16-pin 150-mil wide plastic SOIC (W)

Description

Pericom Semiconductor's PI5C3253 is a Dual 4:1 Multiplexer/demultiplexer with three-state outputs that is pinout compatible with the PI74FCT253T, 74F253, and 74ALS/AS/LS 253. Inputs can be connected to outputs with low On-Resistance (5Ω) with no additional ground bounce noise or propagation delay.

Block Diagram

Pin Configuration

Truth Table⁽¹⁾

Enable		Select				
EA	EB	S1	S0	YA	YB	Function
H	X	X	X	Hi-Z	X	Disable A
X	H	X	X	X	Hi-Z	Disable B
L	L	L	L	IA0	IB0	S1-0 = 0
L	L	L	H	IA1	IB1	S1-0 = 1
L	L	H	L	IA2	IB2	S1-0 = 2
L	L	H	H	IA3	IB3	S1-0 = 3

Pin Description

Pin Name	Description
IAn, IBn	Data Inputs
S0-1	Select Inputs
EA, EB	Enable
YA, YB	Data Outputs
GND	Ground
VCC	Power

Note:

1. H = High Voltage Level, L = Low Voltage Level

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & V _{CC} Only)..	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current.....	120mA
Power Dissipation	0.5W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = -40°C to +85°C, V_{CC} = 5V ±5%)

Parameters	Description	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level	2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level	-0.5		0.8	
I _{IH}	Input HIGH Current	V _{CC} = Max., V _{IN} = V _{CC}			±1	μA
I _{IL}	Input LOW Current	V _{CC} = Max., V _{IN} = GND			±1	
I _{OZH}	High Impedance Output Current	0 ≤ I _N , Y _N ≤ V _{CC}			±1	
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18mA		-0.7	-1.2	V
I _{OS}	Short Circuit Current ⁽³⁾	I (Y) = 0V, Y (I) = V _{CC}	100			mA
V _H	Input Hysteresis at Control Pins			150		mV
R _{ON}	Switch On-Resistance ⁽⁴⁾	V _{CC} = Min., V _{IN} = 0.0V, I _{ON} = 48mA		5	7	Ω
		V _{CC} = Min., V _{IN} = 2.4V, I _{ON} = 15mA		10	15	

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, T_A = 25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Measured by the voltage drop between I and Y pin at indicated current through the switch. ON resistance is determined by the lower of the voltages on the two (I,Y) pins.

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters ⁽¹⁾	Description	Test Conditions	Typ.	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V		6	pF
C _{OFF}	I _A /I _B Capacitance, Switch Off			6	
C _{ON}	I _A /I _B Capacitance, Switch On			24	

Notes:

1. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	3.0	μA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4V ⁽³⁾			2.5	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., I and Y Pins Open E _X = GND Control Input Toggling 50% Duty Cycle				0.25	mA/ MHz

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V, control inputs only); I and Y pins do not contribute to I_{CC}.
4. This current applies to the control inputs only and represent the current required to switch internal capacitance at the specified frequency. The I and Y inputs generate no significant AC or DC currents as they transition. This parameter is not tested, but is guaranteed by design.

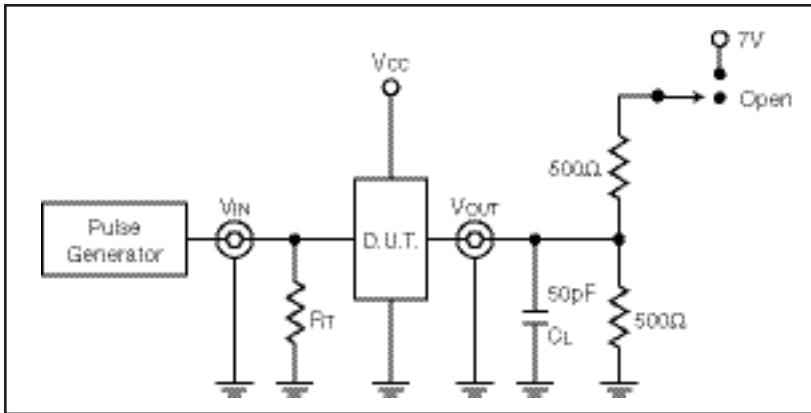
Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	Com.		Units
			Min.	Max.	
t _{IY}	Propagation Delay ^(2,3) In to Yn	C _L = 50pF R _L = 500Ω		0.25	ns
t _{SY}	Bus Select Time, S _n to Y _n		0.5	6.6	
t _{PZH} t _{PZL}	Bus Enable Time, \bar{E}_n to Y _n		0.5	6.0	
t _{PHZ} t _{PLZ}	Bus Disable Time, \bar{E}_n to Y _n		0.5	6.0	

Notes:

1. See test circuit and waveforms.
2. This parameter is guaranteed but not tested on Propagation Delays.
3. The bus switch contributes no propagational delay other than the RC delay of the On-Resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25ns for 50pF load. Since this time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagational delay to the system. Propagational delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

Test Circuit



Switch Position

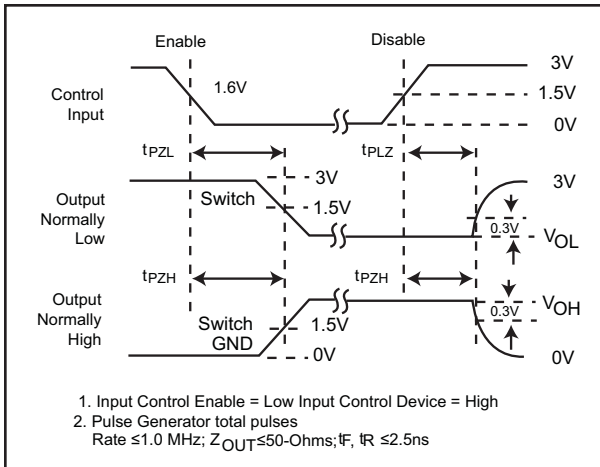
Test	Switch
Disable LOW	Closed
Enable LOW	Closed
t_{PD}	Open

Definitions:

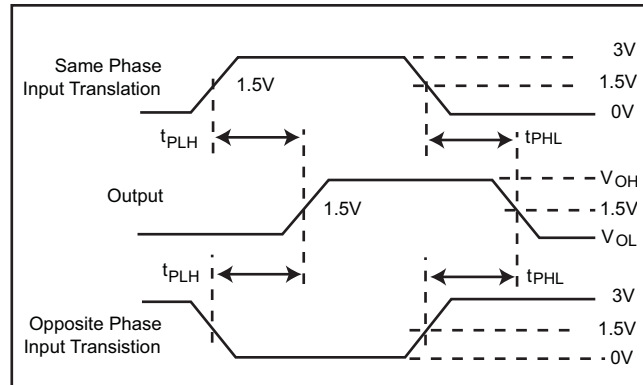
CL = Load Capacitance (includes jig and probe capacitance)

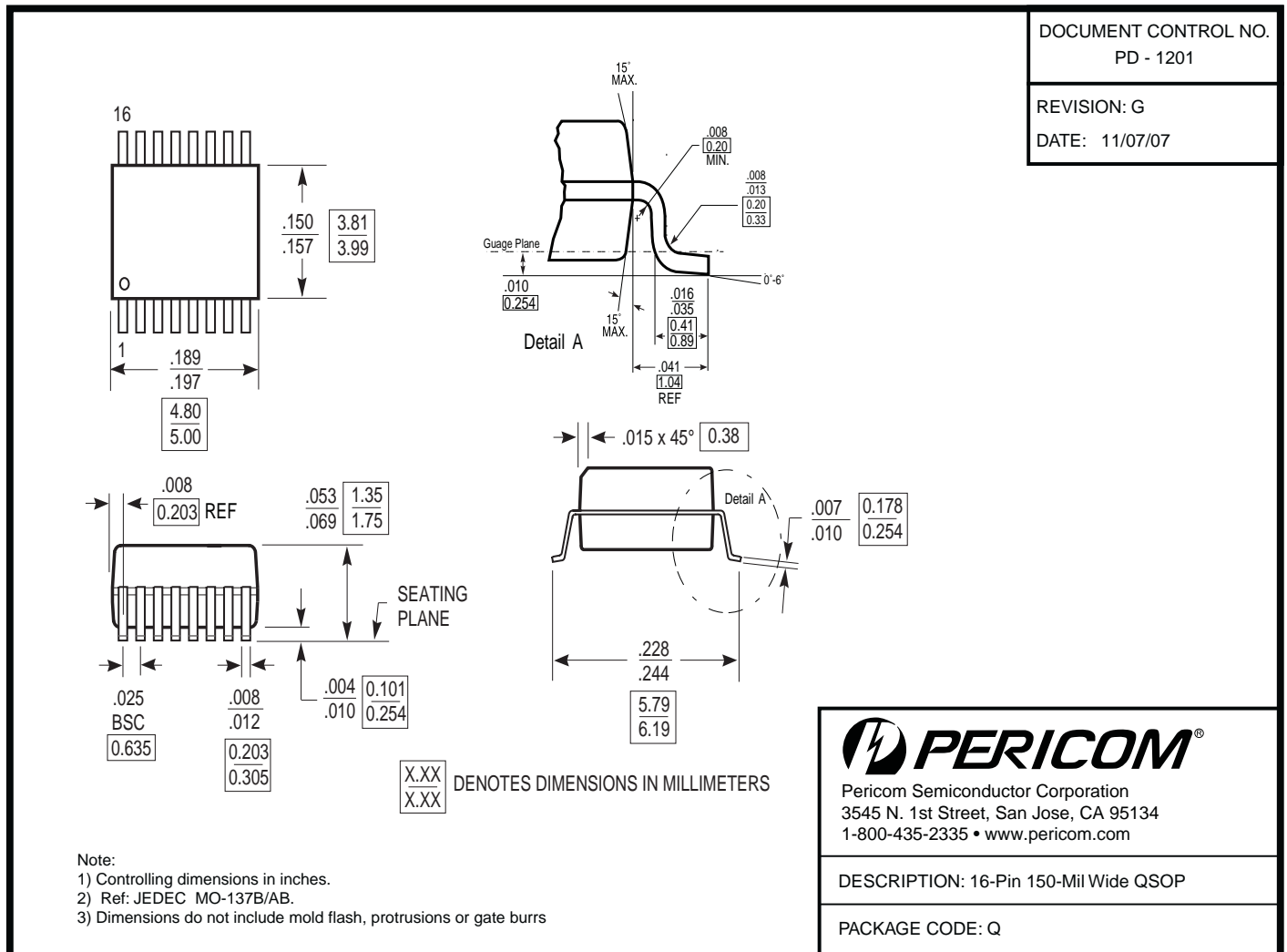
RT = Termination resistance (should be equal to ZOUT of the pulse generator)

Enable and Disable Timing Diagram

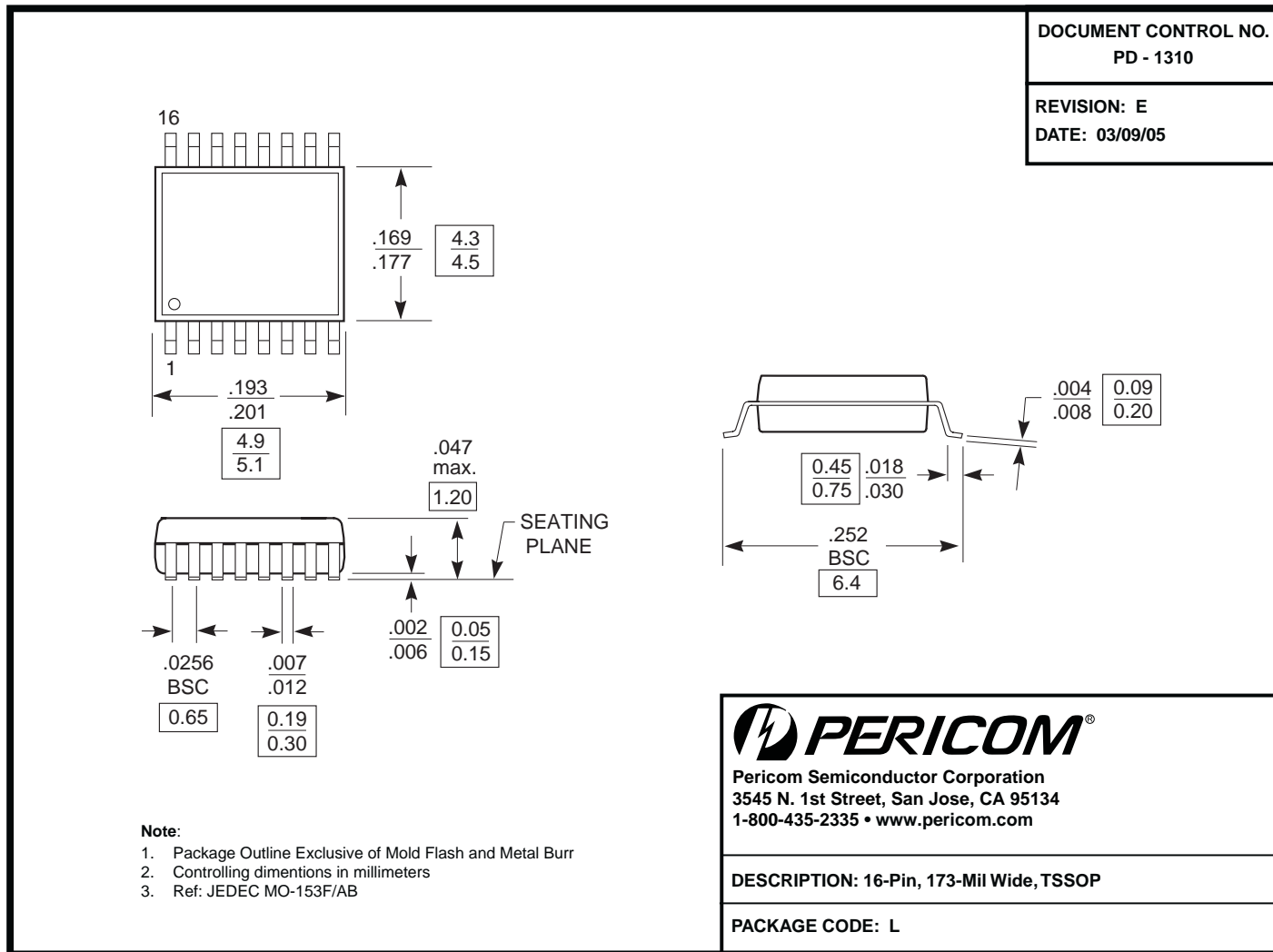


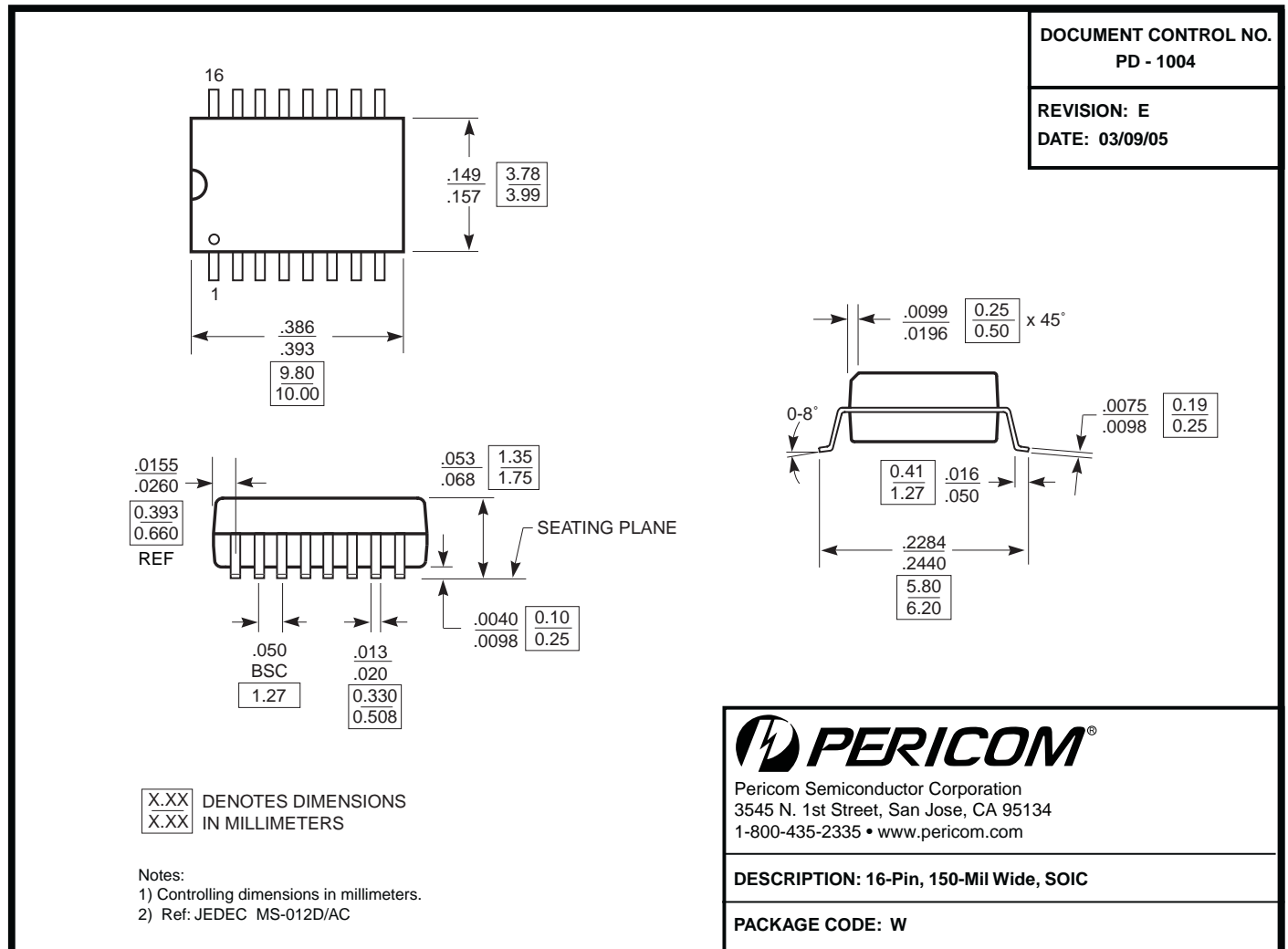
Propagation Delay Diagram



Packaging Mechanical: 16-pin QSOP (Q)


Packaging Mechanical: 16-pin TSSOP (L)



Packaging Mechanical: 16-pin SOIC (W)

Ordering Information

Ordering Code	Package Code	Package Description
PI5C3253QE	Q	Pb-free & Green, 16-pin 150-mil wide QSOP
PI5C3253LE	L	Pb-free & Green, 16-pin 173-mil wide TSSOP
PI5C3253WE	W	Pb-free & Green, 16-pin 150-mil wide SOIC

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- Adding an X suffix = Tape/Reel