

## 12-Bit to 24-Bit Registered Bus Exchanger With 3-STATE Outputs

### Product Features

- PI74ALVCHR16269 is designed for low voltage operation
- $V_{CC} = 2.3V$  to  $3.6V$
- Hysteresis on all inputs
- Typical  $V_{OLP}$  (Output Ground Bounce)  
 $< 0.8V$  at  $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  
 $< 2.0V$  at  $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$
- All output ports have equivalent  $26\Omega$  series resistors, no external resistors are required
- Bus Hold retains last active bus state during 3-STATE, eliminating the need for external pullup resistors
- Industrial operation at  $-40^\circ C$  to  $+85^\circ C$
- Packages available:
  - 56-pin 240 mil wide plastic TSSOP (A)
  - 56-pin 300 mil wide plastic SSOP (V)

### Product Description

Pericom Semiconductor's PI74ALVCHR series of logic circuits are produced in the Company's advanced 0.5 micron CMOS technology, achieving industry leading speed.

The PI74ALVCHR16269 is used in applications in which two separate ports must be multiplexed onto, or demultiplexed from, a single port. It is particularly suitable as an interface between synchronous DRAM's and high-speed microprocessors.

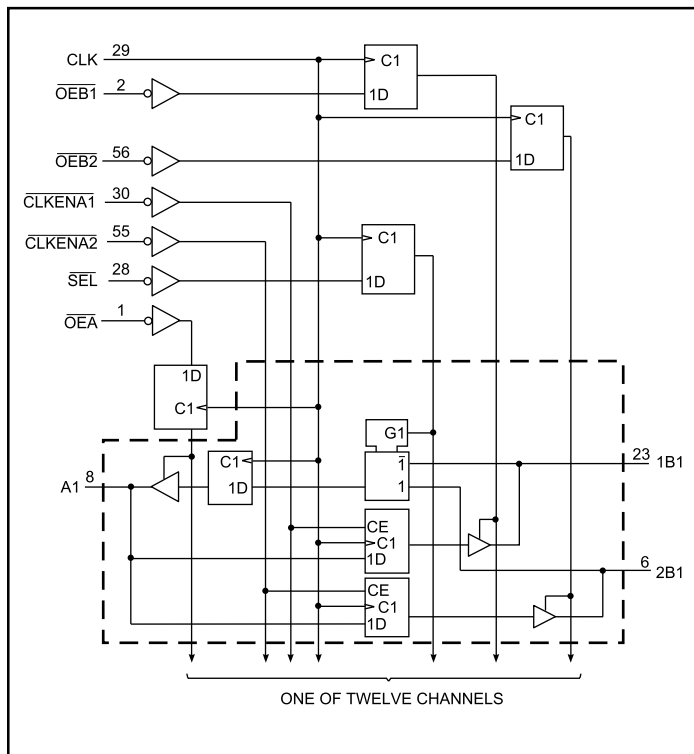
Data is stored on the internal B-port registers on the low-to-high transition of the clock (CLK) input when the appropriate clock-enable ( $\overline{CLKENA}$ ) inputs are low. Proper control of these inputs allows two sequential 12-bit words to be presented as a 24-bit word on the B-port. For data transfer in the B-to-A direction, a single storage register is provided. The select ( $\overline{SEL}$ ) line selects 1B or 2B data for the A outputs. The register on the A output permits the fastest possible data transfer, thus extending the period during which the data is valid on the bus. The control terminals are registered so that all transactions are synchronous with CLK. Data flow is controlled by the active-low output enables ( $\overline{OEA}$ ,  $\overline{OEB1}$ , and  $\overline{OEB2}$ ).

To ensure the high-impedance state during power up or power down, a clock pulse should be applied as soon as possible and  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. Due to  $\overline{OE}$  being routed through a register, the active state of the outputs cannot be determined prior to the arrival of the first clock pulse.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

All outputs are designed to sink up to 12mA and include  $26\Omega$  resistors to reduce overshoot and undershoot.

### Logic Block Diagram



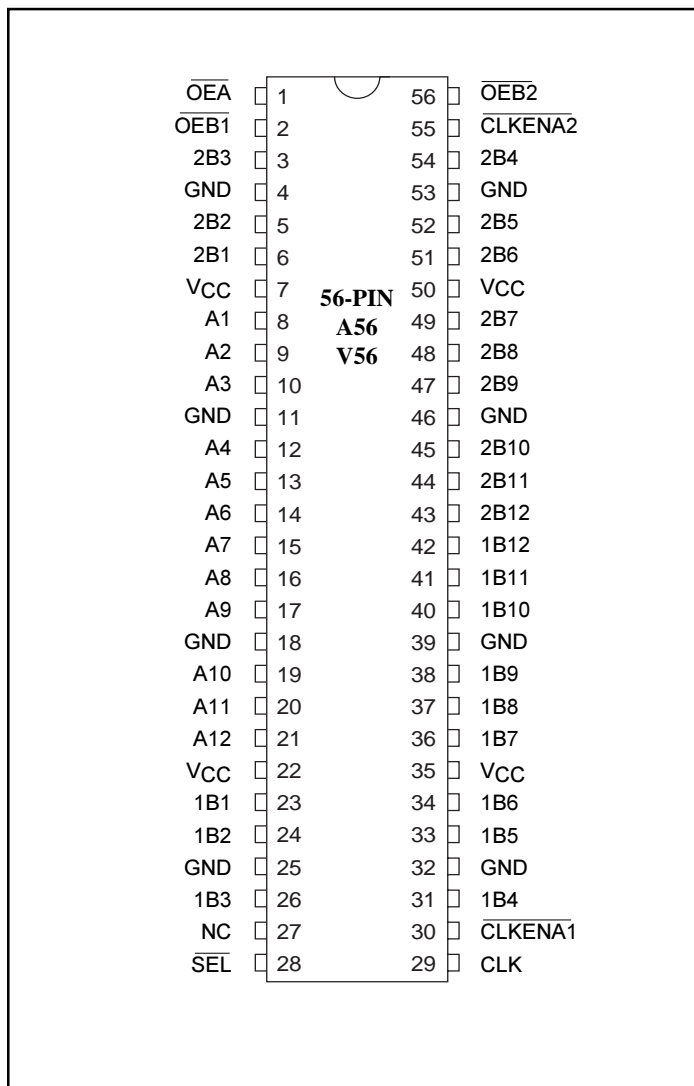
### Product Pin Description

Pin Name	Description
OE	Output Enable Input (Active LOW)
CLK	Clock
SEL	Select (Active Low)
CLKEN	Clock Enable (Active Low)
A,1B,2B	3-State Outputs
GND	Ground
VCC	Power

### Truth Tables<sup>(1)</sup>

Inputs			Outputs	
CLK	OE $\bar{A}$	OE $\bar{B}$	A	1B,2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

### Product Pin Configuration



### A to B STORAGE (OE $\bar{B}$ = L)

INPUTS				OUTPUTS	
CLKENA1	CLKENA2	CLK	A	1B	2B
L	H	↑	L	L	2B <sub>0</sub> <sup>(2)</sup>
L	H	↑	H	H	2B <sub>0</sub> <sup>(2)</sup>
L	L	↑	L	L	L
L	L	↑	H	H	H
H	L	↑	L	1B <sub>0</sub> <sup>(2)</sup>	L
H	L	↑	H	1B <sub>0</sub> <sup>(2)</sup>	H
H	H	X	X	1B <sub>0</sub> <sup>(2)</sup>	2B <sub>0</sub> <sup>(2)</sup>

### B to A STORAGE (OE $\bar{A}$ = L)

Inputs				Outputs A
CLK	SEL	1B	2B	
X	H	X	X	A0 <sup>(2)</sup>
X	L	X	X	A0 <sup>(2)</sup>
↑	H	L	X	L
↑	H	H	X	H
↑	L	X	L	L
↑	L	X	H	H

#### Notes:

- H = High Signal Level  
 L = Low Signal Level  
 X = Irrelevant  
 Z = High Impedance  
 ↑ = Transition, Low to High
- Output level before indicated steady state input conditions established

### Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	-65°C to +150°C
Supply Voltage Range, $V_{CC}$ .....	-0.5V to 4.6V
Input Voltage Range, $V_I$ ; Except	
I/O ports <sup>(1)</sup> .....	-0.5V to 4.6V
I/O ports <sup>(1,2)</sup> .....	-0.5V to $V_{CC} + 0.5V$
Output Voltage Range, $V_O$ <sup>(1,2)</sup> .....	-0.5V to $V_{CC} + 0.5V$
Input Clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	-50mA
Output Clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	-50mA
Continuous Output Current, $I_O$ .....	±50mA
Continuous Current through each $V_{CC}$ or GND .....	±100mA
Maximum Power Dissipation:	
A package .....	1W
V package .....	1.4W

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Notes:**

1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6V maximum.

**DC Electrical Characteristics** (Over the Operating Range,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 3.3V \pm 10\%$ )

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
$V_{CC}$	Supply Voltage		2.3		3.6	
$V_{IH}^{(1)}$	Input HIGH Voltage	$V_{CC} = 2.3V$ to $2.7V$	1.7			V
		$V_{CC} = 2.7V$ to $3.6V$	2.0			
$V_{IL}^{(1)}$	Input LOW Voltage	$V_{CC} = 2.3V$ to $2.7V$			0.7	
		$V_{CC} = 2.7V$ to $3.6V$			0.8	
$V_{IN}^{(1)}$	Input Voltage		0		$V_{CC}$	
$V_{OUT}^{(1)}$	Output Voltage		0		$V_{CC}$	
$I_{OH}^{(1)}$	HIGH-level Output Current	$V_{CC} = 2.3V$			-6	mA
		$V_{CC} = 2.7V$			8	
		$V_{CC} = 3.0V$			-12	
$I_{OL}^{(1)}$	LOW-level Output Current	$V_{CC} = 2.3V$			6	
		$V_{CC} = 2.7V$			8	
		$V_{CC} = 3.0V$			12	
$T_A$	Operating Free-Air Temperature		-40		85	°C
$At/\Delta v$	Input Transition Rise or Fall Rate				10	ns/V

**Note:**

1. Unused control inputs must be held HIGH or LOW to prevent them from floating.

**DC Electrical Characteristics-Continued** (Over the Operating Range,  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 3.3\text{V} \pm 10\%$ )

Parameters	Test Conditions	$V_{CC}^{(1)}$	Min.	Typ. <sup>(2)</sup>	Max.	Units
$V_{OH}$	$I_{OH} = -100\mu\text{A}$	Min. to Max.	$V_{CC} - 0.2$			V
	$I_{OH} = -4\text{mA}$	$V_{IH} = 1.7\text{V}$	2.3V	1.9		
		$V_{IH} = 2.0\text{V}$	2.7V	2.2		
	$I_{OH} = -6\text{mA}$	$V_{IH} = 1.7\text{V}$	2.3V	1.7		
		$V_{IH} = 2.0\text{V}$	3.0V	2.4		
	$I_{OH} = -8\text{mA}$	$V_{IH} = 2.0\text{V}$	2.7V	2.0		
$I_{OH} = -12\text{mA}$	$V_{IH} = 2.0\text{V}$	3.0V	2.0			
$V_{OL}$	$I_{OL} = 100\mu\text{A}$	Min. to Max.			0.2	V
	$I_{OL} = 4\text{mA}$	$V_{IL} = 0.7\text{V}$	2.3V		0.4	
		$V_{IL} = 0.8\text{V}$	2.7V		0.4	
	$I_{OL} = 6\text{mA}$	$V_{IL} = 0.7\text{V}$	2.3V		0.55	
		$V_{IL} = 0.8\text{V}$	3.0V		0.55	
	$I_{OL} = 8\text{mA}$	$V_{IL} = 0.8\text{V}$	2.7V		0.6	
$I_{OL} = 12\text{mA}$	$V_{IL} = 0.8\text{V}$	3.0V		0.8		
$I_I$	$V_I = V_{CC}$ or GND		3.6V		$\pm 5$	$\mu\text{A}$
$I_I$ (Hold) <sup>(3)</sup>	$V_I = 0.7\text{V}$		2.3V	45		
	$V_I = 1.7\text{V}$			-45		
	$V_I = 0.8\text{V}$		3.0V	75		
	$V_I = 2.0\text{V}$			-75		
	$V_I = 0$ to 3.6V		3.6V		$\pm 500$	
$I_{OZ}^{(4)}$	$V_O = V_{CC}$ or GND		3.6V		$\pm 10$	
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$		3.6V		40	
$\Delta I_{CC}$	One input at $V_{CC} - 0.6\text{V}$ , Other inputs at $V_{CC}$ or GND		3V to 3.6V		750	
$C_I$ Control Inputs	$V_I = V_{CC}$ or GND		3.3V		3.5	pF
$C_{IO}$ A or B Ports	$V_O = V_{CC}$ or GND		3.3V		8.5	

**Notes:**

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at  $V_{CC} = 3.3\text{V}$ ,  $+25^{\circ}\text{C}$  ambient and maximum loading.
3. Bus hold maximum dynamic current required to switch the input from one state to another
4. For I/O ports, the  $I_{OZ}$  includes the input leakage current.

### Timing Requirements over Operating Range

Parameters	Description	V <sub>CC</sub> = 2.5V ± 0.2V		V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 3.3V ± 0.3V		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
f <sub>CLOCK</sub>	Clock frequency		95		115		135	MHz
t <sub>w</sub>	Pulse duration, CLK High or Low	5.2		4.3		3.3		ns
t <sub>SU</sub>	Setup time	A data before CLK ↑	1.4		1.4		1	
		B data before CLK ↑	1.6		1.5		1.1	
		$\overline{\text{SEL}}$ before CLK ↑	0.8		1.1		1.3	
		$\overline{\text{CLKENA1}}$ or $\overline{\text{CLKENA2}}$ before CLK ↑	0.8		1		0.8	
		$\overline{\text{OE}}$ data before CLK ↑	1.7		1.6		1.2	
t <sub>H</sub>	Hold time	A data after CLK ↑	0.9		0.9		1.2	
		B data after CLK ↑	0.8		0.6		1	
		$\overline{\text{SEL}}$ after CLK ↑	1.1		0.8		1.7	
		$\overline{\text{CLKENA1}}$ or $\overline{\text{CLKENA2}}$ after CLK ↑	1.4		1		1.6	
		$\overline{\text{OE}}$ after CLK ↑	0.9		0.8		1.2	

### Switching Characteristics over Operating Range<sup>(1)</sup>

Parameters	From (INPUT)	To (OUTPUT)	V <sub>CC</sub> = 2.5V ± 0.2V		V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 3.3V ± 0.3V		Units
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
f <sub>MAX</sub>			95		115		135		ns
t <sub>PD</sub>	CLK	B	2.3	7.7		6.9	2.2	5.8	
		A	1.9	6.4		5.8	2	5.2	
t <sub>EN</sub>	CLK	B	2.5	7.7		6.9	2.3	5.8	
		A	2.2	6.7		6	2.1	5.3	
t <sub>DIS</sub>	CLK	B	3.3	8.1		6.7	2.4	6	
		A	2.7	8		6.2	2.1	6	

**Notes:**

- Unused control inputs must be held HIGH or LOW to prevent them from floating.
- Minimum limits are guaranteed but not tested on Propagation Delays.

### Operating Characteristics, T<sub>A</sub> = 25°C

Parameter		Test Conditions	V <sub>CC</sub> = 2.5V ± 0.2V	V <sub>CC</sub> = 3.3V ± 0.3V	Units
			Typical		
C <sub>PD</sub> Power Dissipation Capacitance per Exchanger	Outputs Enabled	C <sub>L</sub> = 0pF, F = 10 MHz	142	172	pF
	Outputs Disabled		115	129	