Fast CMOS 18-Bit Registered Transceivers

Product Features

- Functionally compatible with FCT3, LVT, and 74 series 16501 families of products
- Tri-State outputs
- 5V Tolerant inputs and outputs
- 2.0V-3.6V V_{CC} supply operation
- Balanced sink and source output drives (24 mA)
- Low ground bounce outputs
- Supports live insertion
- ESD Protection exceeds 2000V, Human Body Model
  200V, Machine Model
- Packages available:
  – 56-pin 240-mil wide plastic TSSOP (A)
  – 56-pin 300-mil wide plastic SSOP (V)

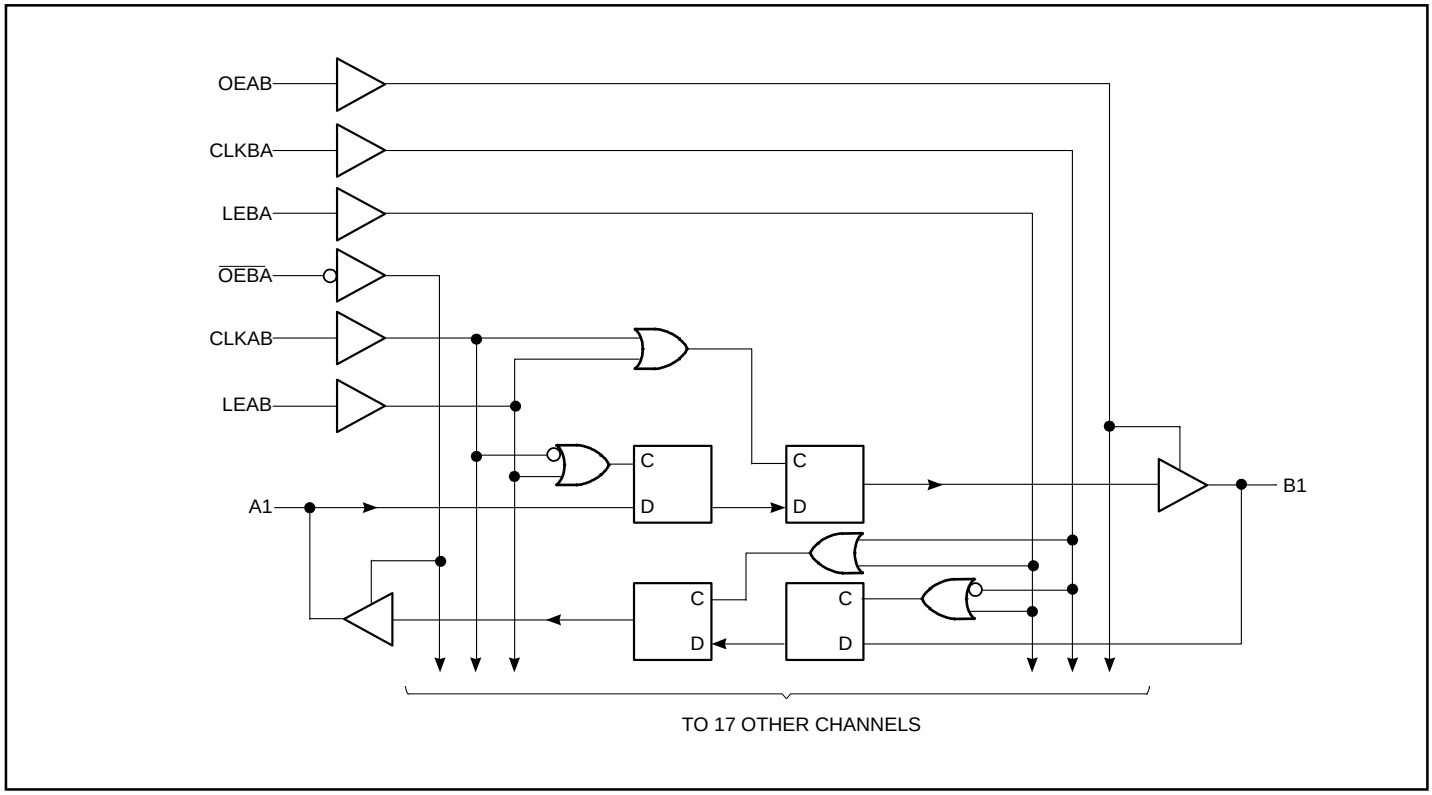
Product Description

Pericom Semiconductor's PI74LCX series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The PI74LCX16501 is an 18-bit registered bus transceiver designed with D-type latches and flip-flops to allow data flow in transparent, latched, and clocked modes. The Output Enable ($\overline{OEAB}$ and OEBA, Latch Enable (LEAB and LEBA) and Clock (CLKAB and CLKBA) inputs control the data flow in each direction. When LEAB is HIGH, the device operates in transparent mode for A-to-B data flow. When LEAB is LOW, the A data is latched if CLKAB is held at a HIGH or LOW logic level. The A bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of CLKAB, if LEAB is LOW. OEAB performs the output enable function on the B port. Data flow from B port to A port is similar using $\overline{OEBA}$, LEBA and CLKBA. This high-speed, low-power device offers a flow-through organization for ease of board layout.

The PI74LCX16501 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3V/5.0V system.

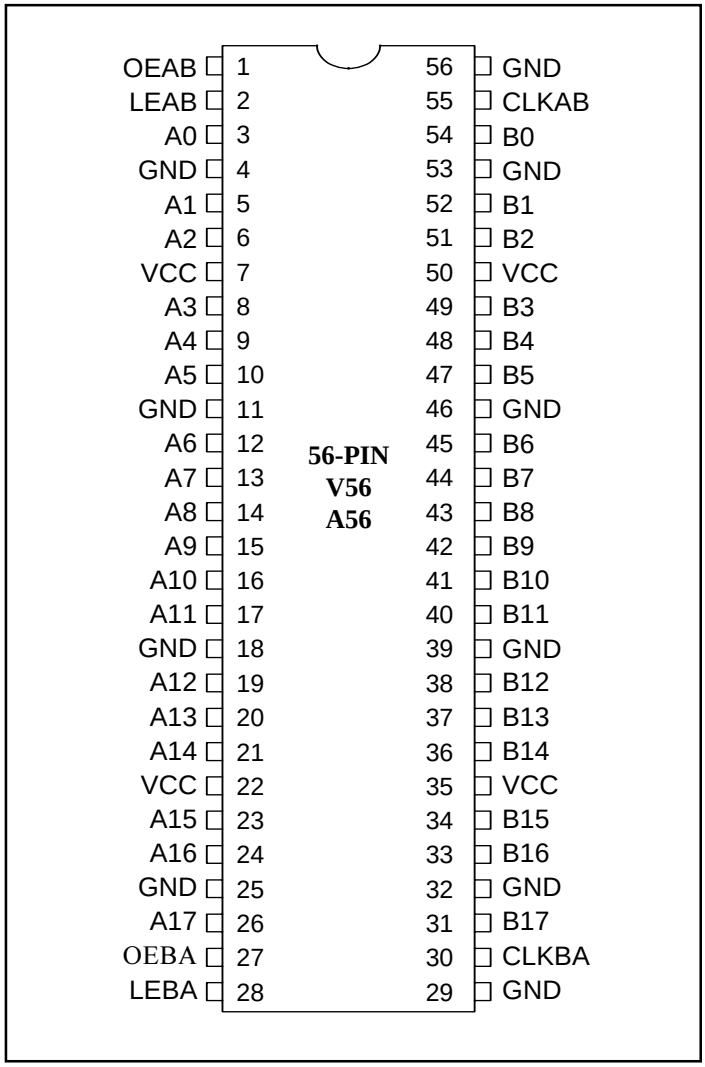
Logic Block Diagram



Product Pin Description

Pin Name	Description
OEAB	A-to-B Output Enable Input
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
Ax	A-to-B Data Inputs or B-to-A 3-State Outputs
Bx	B-to-A Data Inputs or A-to-B 3-State Outputs
GND	Ground
VCC	Power

Product Pin Configuration



Truth Table[1]

Inputs				Outputs
OEAB	LEAB	CLKAB	Ax	Bx
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	H	X	B[2]
H	L	L	X	B[3]

Notes:

1. A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{OEBA}$, LEBA, and CLKBA.
2. Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.
3. Output level before the indicated steady-state input conditions were established.
4. H = High Voltage Level
   L = Low Voltage Level
   Z = High Impedance
   ↑ = LOW-to-HIGH Transition

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Symbol	Parameter		Min.	Max.	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	
		TRI-State	0	5.5	
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V-3.6V	—	±24	mA
		V_{CC} = 2.7V	—	±12	
T_A	Free-Air Operating Temperature		–40	+85	°C
$\Delta t/\Delta V$	Input Edge Rate	V = 0.8V-2.0V, V_{CC} = 3.0V	0	10	ns/V

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 2.7V to 3.6V)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0	—	—	V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level		—	—	0.8	
V_{OH}	Output HIGH Voltage	V_{CC} = 2.7-3.6	I_{OH} = –0.1mA	V_{CC}-0.2	—	—	
		V_{CC} = 2.7	I_{OH} = –12mA	2.2	—	—	
		V_{CC} = 3.0	I_{OH} = –18mA	2.4	—	—	
			I_{OH} = –24mA	2.2	—	—	
V_{OL}	Output LOW Voltage	V_{CC} = 2.7-3.6	I_{OL} = 0.1mA	—	—	0.2	
		V_{CC} = 2.7	I_{OL} = 12mA	—	—	0.4	
		V_{CC} = 3.0	I_{OL} = 16mA	—	—	0.4	
			I_{OL} = 24mA	—	—	0.55	
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18mA		—	–0.7	–1.2	
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	Vcc = 2.7-3.6	—	—	±5	µA
I_{OZ}	Tri-State Output Leakage	0 ≤ V_O ≤ 5.5V V_I = V_{IH} or V_{IL}	V_{CC} = 2.7-3.6	—	—	±5	
I_{OFF}	Power Down Disable	V_{CC} = 0V, V_{IN} or V_{OUT} ≤ 5.5V		—	—	10	
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = GND or V_{CC}	—	0.1	10	
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max.	V_{IN} = V_{CC} – 0.6V[3]	—	—	500	

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Per TTL driven input; all other inputs at V_{CC} or GND.

Capacitance

Parameters	Description	Test Conditions	Typ.	Units
C_{IN}	Input Capacitance	V_{CC} = Open, V_I = 0V or V_{CC}	7	pF
C_{OUT}	Output Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}	8	
C_{PD}	Power Dissipation Capacitance	V_{CC} = 3.3V, V_I = 0V or V_{CC}, F = 10 MHz	20	

Switching Characteristics over Operating Range

Parameters	Description	Conditions	V_{CC} = 3.3V ± 0.3V		V_{CC} = 2.7V		Units
			Min.	Max.	Min.	Max.	
fmax	Maximum Clock Frequency	C_L = 50 pF R_L = 500Ω	170	—	—	—	MHz
t_{PHL} t_{PLH}	Propagation Delay Bus to Bus		1.5	6.0	1.5	7.0	ns
t_{PHL} t_{PLH}	Propagation Delay Clock to Bus		1.5	6.5	1.5	7.5	
t_{PHL} t_{PLH}	Propagation Delay LE to Bus		1.5	6.5	1.5	7.5	
t_{PZL} t_{PZH}	Output Enable Time		1.5	7.5	1.5	8.5	
t_{PLZ} t_{PHZ}	Output Disable Time		1.5	6.0	1.5	7.0	
t_S	Setup Time		2.5	—	2.5	—	
t_H	Hold Time		1.5	—	1.5	—	
t_W	Pulse Width		3.0	—	3.0	—	
$t_{SK(O)}$	Output to Output Skew[1]		—	1.0	—	—	

Note:
1. Skew between any two outputs, of the same package, switching in the same direction.

Dynamic Switching Characteristics (T_A = +25°C)

Parameters	Description	Test Conditions[1]	Typ.	Units
V_{OLP}	Dynamic LOW Peak Voltage	V_{CC} = 3.3V, C_L = 50pF V_{IH} = 3.3V, V_{IL} = 0V	0.8	V
V_{OLV}	Dynamic LOW Valley Voltage	V_{CC} = 3.3V, C_L = 50pF V_{IH} = 3.3V, V_{IL} = 0V		

Note:
1. Measured with n–1 outputs switching from High-to-Low or Low-to-High. The remaining output is measured in the LOW state.