

EPROM-Based 8-Bit CMOS Microcontroller Series

Devices Included in this Data Sheet:

- PIC16LV54A
- PIC16LV58A

High-Performance RISC CPU:

- Only 33 single word instructions to learn
- All instructions are single cycle (2 μ s) except for program branches which are two-cycle
- Operating speed: DC - 2 MHz clock input
DC - 2 μ s instruction cycle

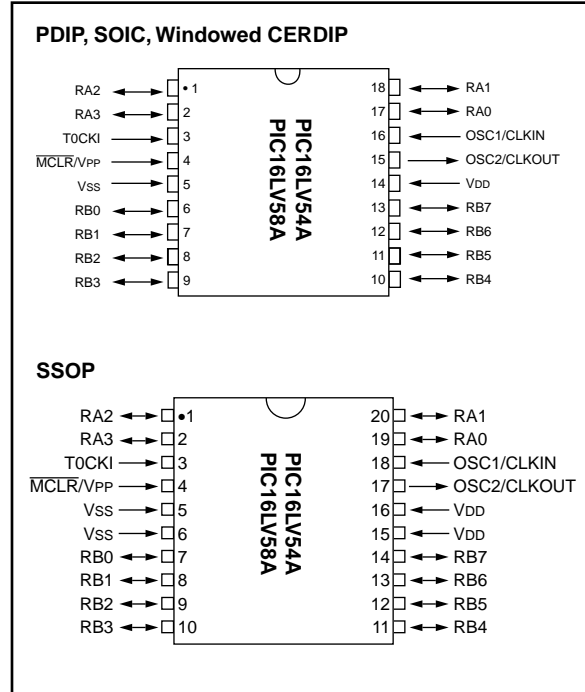
Device	Pins	I/O	EPROM	RAM
PIC16LV54A	18	12	512	25
PIC16LV58A	18	12	2K	73

- 12-bit wide instructions
- 8-bit wide data path
- Seven special function hardware registers
- Two-level deep hardware stack
- Direct, indirect and relative addressing modes for data and instructions

Peripheral Features:

- 8-bit real time clock/counter (TMR0) with 8-bit programmable prescaler
- Power-On Reset (POR)
- Device Reset Timer (DRT)
- Watchdog Timer (WDT) with its own on-chip RC oscillator for reliable operation
- Programmable code-protection
- Power saving SLEEP mode
- Selectable oscillator options:
 - RC: Low-cost RC oscillator
 - XT: Standard crystal/resonator
 - LP: Power saving, low frequency crystal

Pin Configurations



CMOS Technology:

- Low-power, high-speed CMOS EPROM technology
- Fully static design
- Wide-operating voltage range:
 - EPROM Commercial/Industrial 2.0V to 3.8V
- Low-power consumption
 - < 1 mA typical @ 3V, 2 MHz
 - 10 μ A typical @ 2V, 32 kHz
 - < 0.6 μ A typical standby current (with WDT disabled) @ 3V, 0°C to 70°C

Enhanced PIC16LV5X

1.0 GENERAL DESCRIPTION

The Enhanced PIC16LV5X from Microchip Technology is a family of low-cost, high performance, 8-bit, fully static, EPROM-based CMOS microcontrollers. This family is pin and software compatible with the PIC16LV5X family of devices in a new enhanced process technology. It employs a RISC architecture with only 33 single word/single cycle instructions. All instructions are single cycle (2 μ s) except for program branches which take two cycles. The Enhanced PIC16LV5X delivers performance an order of magnitude higher than its competitors in the same price category. The 12-bit wide instructions are highly symmetrical resulting in 2:1 code compression over other 8-bit microcontrollers in its class. The easy to use and easy to remember instruction set reduces development time significantly.

The Enhanced PIC16LV5X products are equipped with special features that reduce system cost and power requirements. The Power-On Reset (POR) and Device Reset Timer (DRT) eliminate the need for external reset circuitry. There are three oscillator configurations to choose from, including the power-saving LP (Low Power) oscillator and cost saving RC oscillator. Power saving SLEEP mode, Watchdog Timer and code protection features improve system cost, power and reliability.

The UV erasable CERDIP packaged versions are ideal for code development, while the cost-effective One-Time-Programmable (OTP) versions are suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in OTP microcontrollers while benefiting from the OTP's flexibility.

The Enhanced PIC16LV5X products are supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a 'C' compiler, fuzzy logic support tools, a low-cost development programmer, and a full featured programmer. All the tools are supported on IBM[®] PC and compatible machines.

1.1 Applications

The Enhanced PIC16LV5X series fits perfectly in applications such as low-power remote transmitters/receivers and pointing devices. The EPROM technology makes customizing application programs (transmitter codes, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages, for through hole or surface mounting, make this microcontroller series perfect for applications with space limitations. Low-cost, low-power, high performance, ease of use and I/O flexibility make the Enhanced PIC16LV5X series very versatile even in areas where no microcontroller use has been considered before (e.g., timer functions, replacement of "glue" logic in larger systems, coprocessor applications).

Enhanced PIC16LV5X

TABLE 1-1: ENHANCED PIC16LV5X FAMILY OF DEVICES

	Maximum Frequency of Operation (MHz)		EPROM Program Memory (words)		RAM Data Memory (bytes)		Clock	Memory	Peripherals	Features	
							Timer Module(s)	I/O Pins	Voltage Range (Volts)	Number of Instructions	Packages
PIC16LV54A	20	512	25	TMR0	12	2.0-3.8	33	18-pin DIP, SOIC; 20-pin SSOP			
PIC16LV58A	20	2K	73	TMR0	12	2.0-3.8	33	18-pin DIP, SOIC; 20-pin SSOP			

Legend: All PIC16/17 Family devices have Power-On Reset, selectable Watchdog Timer, selectable code protect and high I/O current capability.

Enhanced PIC16LV5X

2.0 ENHANCED PIC16LV5X DEVICE VARIETIES

A variety of frequency ranges and packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in this section. When placing orders, please use the Enhanced PIC16LV5X Product Identification System at the back of this data sheet to specify the correct part number.

For the Enhanced PIC16LV5X family of devices, there is one device type, as indicated in the device number:

1. **LV**, as in PIC16LV54A. These devices have EPROM program memory and operate over the standard voltage range of 2.0 to 3.8 volts.

2.1 UV Erasable Devices

The UV erasable versions, offered in CERDIP packages, are optimal for prototype development and pilot programs

UV erasable devices can be programmed for any of the four oscillator configurations. Microchip's PICSTART[®] and PRO MATE[™] programmers both support programming of the Enhanced PIC16LV5X. Third party programmers also are available; refer to the Third Party Guide for a list of sources.

2.2 One-Time-Programmable (OTP) Devices

The availability of OTP devices is especially useful for customers expecting frequent code changes and updates.

The OTP devices, packaged in plastic packages, permit the user to program them once. In addition to the program memory, the configuration bits must be programmed.

2.3 Quick-Turnaround-Production (QTP) Devices

Microchip offers a QTP Programming Service for factory production orders. This service is made available for users who choose not to program a medium to high quantity of units and whose code patterns have stabilized. The devices are identical to the OTP devices but with all EPROM locations and configuration bit options already programmed by the factory. Certain code and prototype verification procedures apply before production shipments are available. Please contact your Microchip Technology sales office for more details.

2.4 Serialized Quick-Turnaround-Production (SQTPSM) Devices

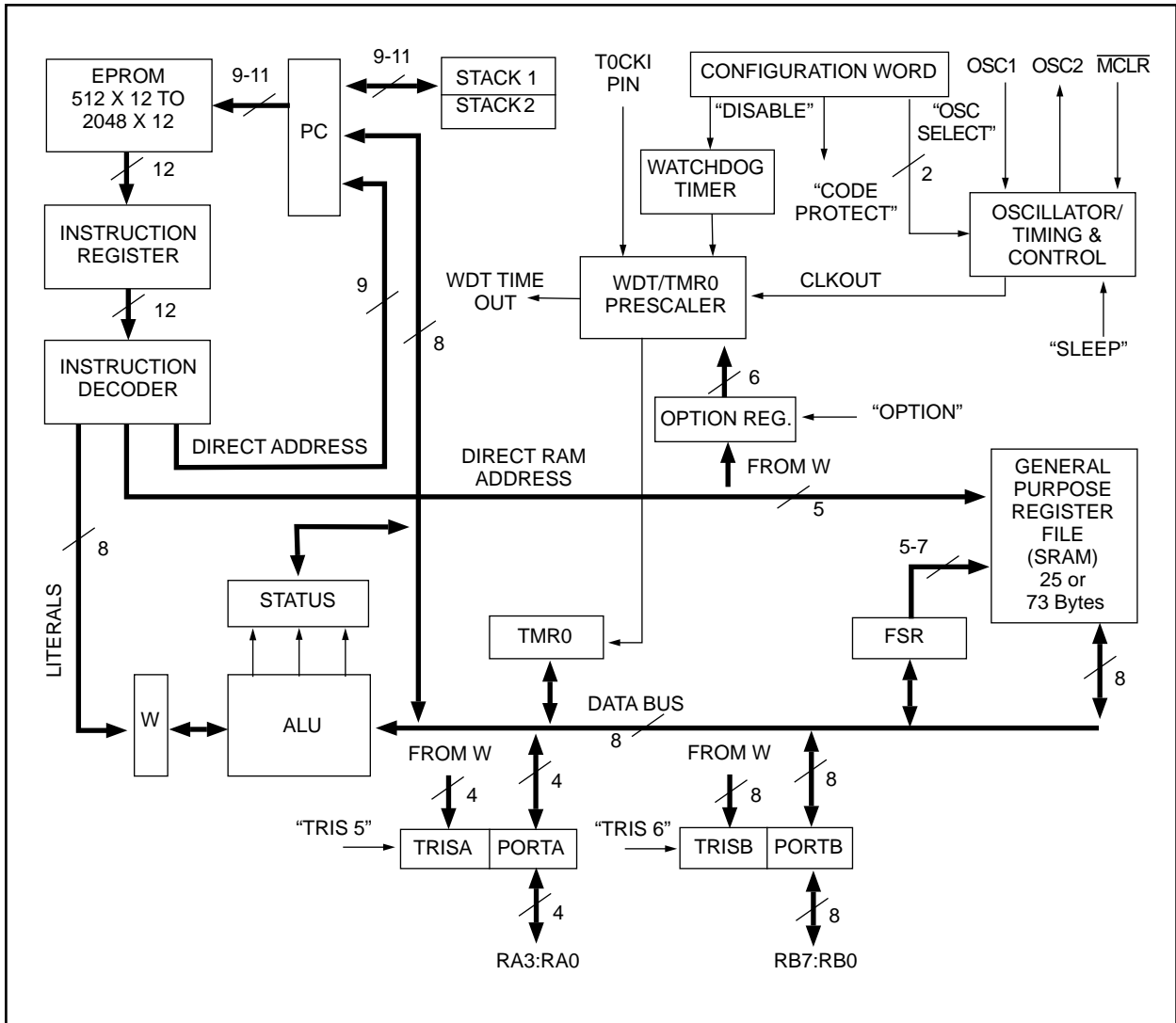
Microchip offers the unique programming service where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number which can serve as an entry code, password or ID number.

3.0 ARCHITECTURAL OVERVIEW

This section provides information on the architecture of the Enhanced PIC16LV5X. For information on operation of the peripherals, electrical specifications, etc., please refer to the Enhanced PIC16C5X data sheet.

FIGURE 3-1: ENHANCED PIC16LV5X SERIES BLOCK DIAGRAM



Enhanced PIC16LV5X

TABLE 3-1: PINOUT DESCRIPTION - PIC16LV54A, PIC16LV58A

Name	DIP, SOIC No.	SSOP No.	I/O/P Type	Input Levels	Description
RA0	17	19	I/O	TTL	Bi-directional I/O port
RA1	18	20	I/O	TTL	
RA2	1	1	I/O	TTL	
RA3	2	2	I/O	TTL	
RB0	6	7	I/O	TTL	Bi-directional I/O port
RB1	7	8	I/O	TTL	
RB2	8	9	I/O	TTL	
RB3	9	10	I/O	TTL	
RB4	10	11	I/O	TTL	
RB5	11	12	I/O	TTL	
RB6	12	13	I/O	TTL	
RB7	13	14	I/O	TTL	
T0CKI	3	3	I	ST	Clock input to Timer0. Must be tied to Vss or VDD, if not in use, to reduce current consumption.
$\overline{\text{MCLR/VPP}}$	4	4	I	ST	Master clear (reset) input/programming voltage input. This pin is an active low reset to the device. Voltage on the $\overline{\text{MCLR/VPP}}$ pin must not exceed VDD to avoid unintended entering of programming mode.
OSC1/CLKIN	16	18	I	ST	Oscillator crystal input/external clock source input.
OSC2/CLKOUT	15	17	O	—	Oscillator crystal output. Connects to crystal or resonator in crystal oscillator mode. In RC mode, OSC2 pin outputs CLKOUT which has 1/4 the frequency of OSC1, and denotes the instruction cycle rate.
VDD	14	15,16	P	—	Positive supply for logic and I/O pins.
Vss	5	5,6	P	—	Ground reference for logic and I/O pins.

Legend: I = input, O = output, I/O = input/output,
 P = power, — = Not Used, TTL = TTL input,
 ST = Schmitt Trigger input

4.0 MEMORY ORGANIZATION

FIGURE 4-1: PIC16LV54A PROGRAM MEMORY MAP AND STACK

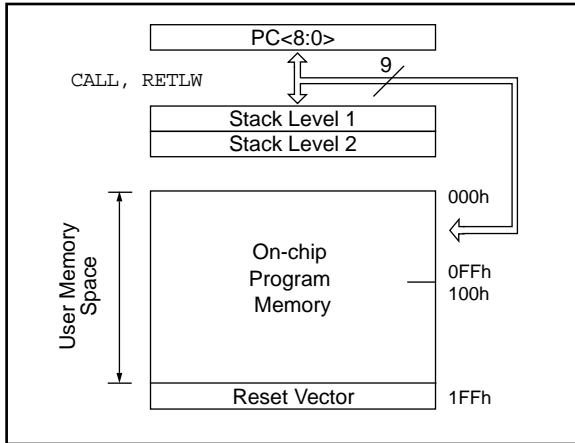


FIGURE 4-2: PIC16LV58A PROGRAM MEMORY MAP AND STACK

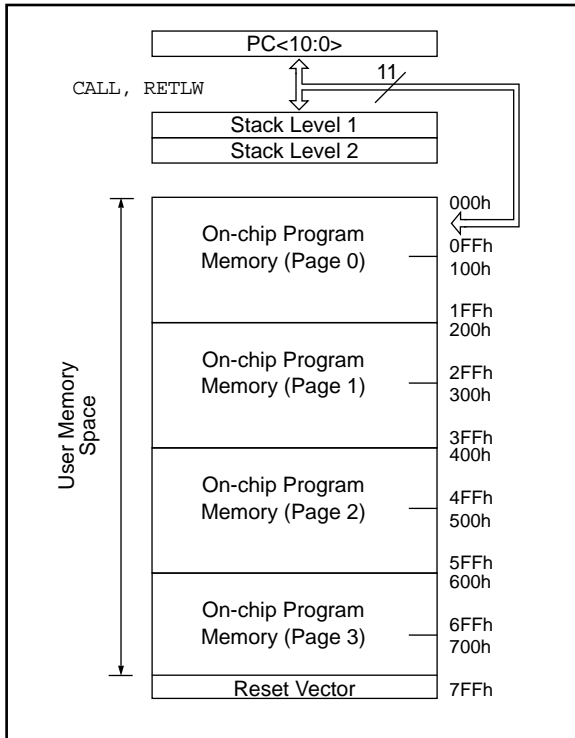
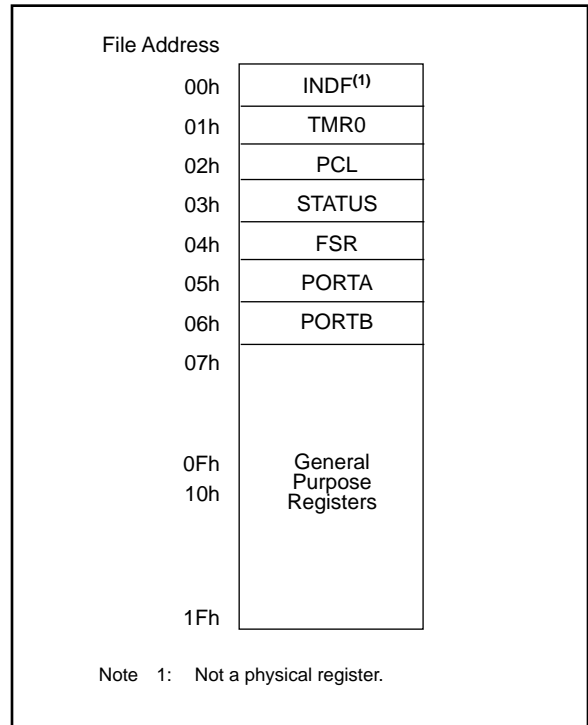


FIGURE 4-3: PIC16LV54A REGISTER FILE MAP



Enhanced PIC16LV5X

FIGURE 4-4: PIC16LV58A REGISTER FILE MAP

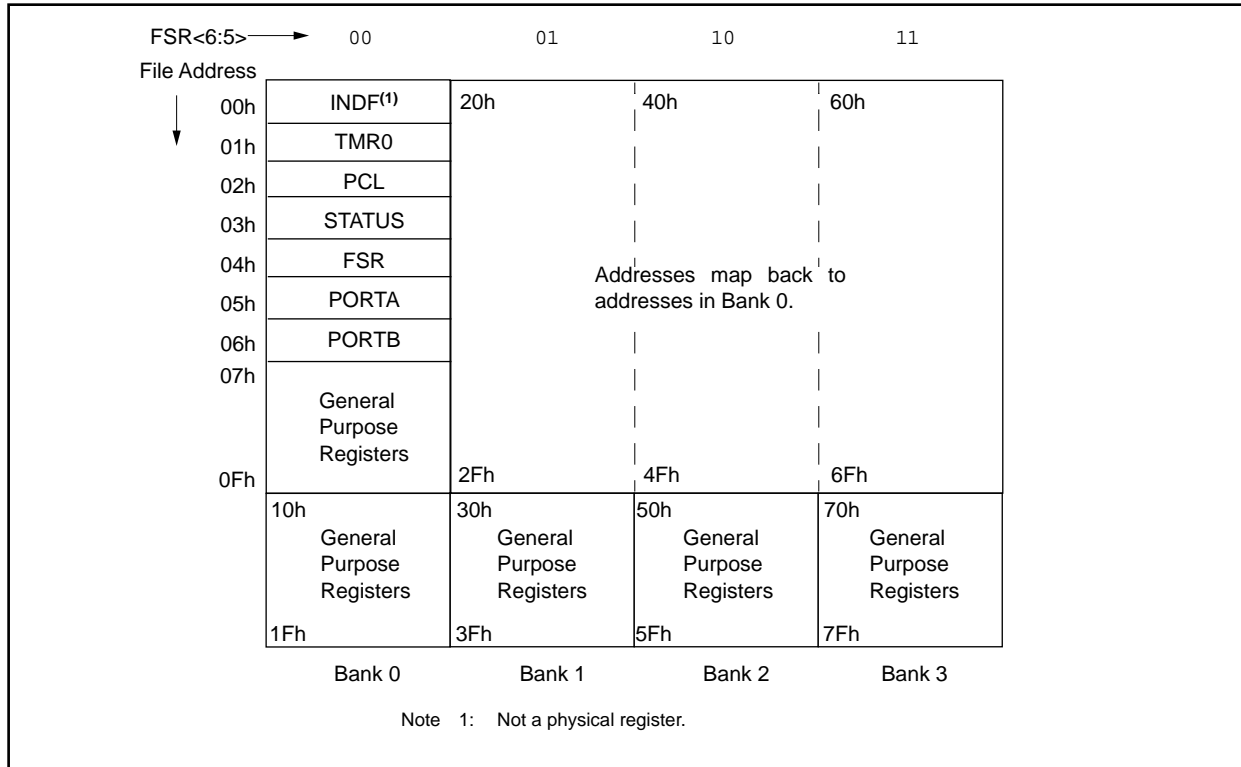


TABLE 4-1: SPECIAL FUNCTION REGISTER SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on Power-On Reset	Value on MCLR and WDT Reset
N/A	TRIS	I/O control registers (TRISA, TRISB, TRISC)								1111 1111	1111 1111
N/A	OPTION	Contains control bits to configure Timer0 and Timer0/WDT prescaler								--11 1111	--11 1111
00h	INDF	Uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
01h	TMR0	8-bit real-time clock/counter								xxxx xxxx	uuuu uuuu
02h ⁽¹⁾	PCL	Low order 8 bits of PC								1111 1111	1111 1111
03h	STATUS	PA2	PA1	PA0	\overline{TO}	\overline{PD}	Z	DC	C	0001 1xxx	000q quuu
04h	FSR	Indirect data memory address pointer								1xxx xxxx	1uuu uuuu
05h	PORTA	—	—	—	—	RA3	RA2	RA1	RA0	---- xxxx	---- uuuu
06h	PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu

Legend: Shaded boxes = unimplemented or unused, — = unimplemented, read as '0' (if applicable)
 x = unknown, u = unchanged, q = value depends on condition.

Note 1: The upper byte of the Program Counter is not directly accessible. See Section 4.5 of the Enhanced PIC16C5X data sheet (DS30236B) for an explanation of how to access these bits.

2: File address 07h is a general purpose register on the PIC16LV54A and PIC16LV58A.

5.0 ELECTRICAL CHARACTERISTICS - PIC16LV5XA

Absolute Maximum Ratings[†]

Ambient temperature under bias	-20°C to +85°C
Storage temperature	- 65°C to +150°C
Voltage on V _{DD} with respect to V _{SS}	0 to +7.5V
Voltage on $\overline{\text{MCLR}}$ with respect to V _{SS} ⁽²⁾	0 to +14V
Voltage on all other pins with respect to V _{SS}	-0.6V to (V _{DD} + 0.6V)
Total power dissipation ⁽¹⁾	800 mW
Max. current out of V _{SS} pin	150 mA
Max. current into V _{DD} pin	100 mA
Max. current into an input pin (TOCKI only)	±500 μ A
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{DD})	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{DD})	±20 mA
Max. output current sunk by any I/O pin	25 mA
Max. output current sourced by any I/O pin	20 mA
Max. output current sourced by a single I/O port (PORTA or B)	40 mA
Max. output current sunk by a single I/O port (PORTA or B)	50 mA

Note 1: Power dissipation is calculated as follows: $P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$

Note 2: Voltage spikes below V_{SS} at the $\overline{\text{MCLR}}$ pin, inducing currents greater than 80mA, may cause latch-up. Thus, a series resistor of 50-100 Ω should be used when applying a "low" level to the $\overline{\text{MCLR}}$ pin rather than pulling this pin directly to V_{SS}

[†] NOTICE: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Enhanced PIC16LV5X

5.1 DC Characteristics: PIC16LV5XA-02 (Commercial) PIC16LV5XA-02 (Industrial)

DC Characteristics Power Supply Pins		Standard Operating Conditions (unless otherwise specified) Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) -20°C ≤ TA ≤ +85°C (industrial)				
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions
Supply Voltage XT, RC and LP options	VDD	2.0		3.8	V	
RAM Data Retention Voltage⁽²⁾	VDR		1.5*		V	Device in SLEEP mode
VDD start voltage to ensure Power-On Reset	VPOR		VSS		V	See section on Power-On Reset for details
VDD rise rate to ensure Power-On Reset	SVDD	0.05*			V/ms	See section on Power-On Reset for details
Supply Current⁽³⁾ XT and RC ⁽⁴⁾ options LP option, Commercial LP option, Industrial	IDD		0.5 11 14	27 35	mA μA μA	FOSC = 2.0 MHz, VDD = 3.0V FOSC = 32 kHz, VDD = 2.5V, WDT disabled FOSC = 32 kHz, VDD = 2.5V, WDT disabled
Power Down Current⁽⁵⁾⁽⁶⁾ Commercial Industrial	IPD		2.5 0.25 3.5 0.3	12 4.0 14 5.0	μA μA μA μA	VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled VDD = 2.5V, WDT enabled VDD = 2.5V, WDT disabled

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- 2: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.
- 3: The supply current is mainly a function of the operating voltage and frequency. Other factors such as bus loading, oscillator type, bus rate, internal code execution pattern, and temperature also have an impact on the current consumption.
 - a) The test conditions for all IDD measurements in active operation mode are:
OSC1 = external square wave, from rail-to-rail; all I/O pins tristated, pulled to VSS, T0CKI = VDD, MCLR = VDD; WDT enabled/disabled as specified.
 - b) For standby current measurements, the conditions are the same, except that the device is in SLEEP mode.
- 4: Does not include current through Rext. The current through the resistor can be estimated by the formula: IR = VDD/2Rext (mA) with Rext in kΩ.
- 5: The power down current in SLEEP mode does not depend on the oscillator type. Power down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD and VSS.
- 6: The oscillator start-up time can be as much as 8 seconds for XT and LP oscillator selection, if the SLEEP mode is entered or during initial power-up.

Enhanced PIC16LV5X

5.2 DC Characteristics: PIC16LV5XA-02 (Commercial) PIC16LV5XA-02 (Industrial)

DC Characteristics All Pins Except Power Supply Pins		Standard Operating Conditions (unless otherwise specified)				
		Operating Temperature 0°C ≤ TA ≤ +70°C (commercial) -20°C ≤ TA ≤ +85°C (industrial) Operating Voltage VDD range is described in Section 10.1, Section 10.2 and Section 10.3 of the Enhanced PIC16C5X data sheet (DS30236B).				
Characteristic	Sym	Min	Typ ⁽¹⁾	Max	Units	Conditions
Input Low Voltage I/O ports $\overline{\text{MCLR}}$ (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	V _{IL}	V _{SS} V _{SS} V _{SS} V _{SS} V _{SS}		0.2 V _{DD} 0.15 V _{DD} 0.15 V _{DD} 0.15 V _{DD} 0.3 V _{DD}	V V V V V	Pin at hi-impedance RC option only ⁽⁴⁾ XT and LP options
Input High Voltage I/O ports $\overline{\text{MCLR}}$ (Schmitt Trigger) T0CKI (Schmitt Trigger) OSC1 (Schmitt Trigger) OSC1	V _{IH}	0.2 V _{DD} +1V 0.85 V _{DD} 0.85 V _{DD} 0.85 V _{DD} 0.7 V _{DD}		V _{DD} V _{DD} V _{DD} V _{DD} V _{DD}	V V V V V	For all V _{DD} ⁽⁵⁾ RC option only ⁽⁴⁾ XT and LP options
Hysteresis of Schmitt Trigger inputs	V _{HYS}	0.15V _{DD} *			V	
Input Leakage Current⁽³⁾ I/O ports $\overline{\text{MCLR}}$ T0CKI OSC1	I _{IL}	-1.0 -5.0 -3.0 -3.0	0.5 0.5 0.5 0.5	+1.0 +5.0 +3.0 +3.0	μA μA μA μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , Pin at hi-impedance V _{PIN} = V _{SS} +0.25V ⁽²⁾ V _{PIN} = V _{DD} ⁽²⁾ V _{SS} ≤ V _{PIN} ≤ V _{DD} V _{SS} ≤ V _{PIN} ≤ V _{DD} , XT and LP options
Output Low Voltage I/O ports OSC2/CLKOUT	V _{OL}			0.6 0.6	V V	I _{OL} = 8.7 mA, V _{DD} = 3.8V I _{OL} = 1.6 mA, V _{DD} = 3.8V, RC option only
Output High Voltage I/O ports ⁽³⁾ OSC2/CLKOUT	V _{OH}	V _{DD} -0.7 V _{DD} -0.7			V V	I _{OH} = -5.4 mA, V _{DD} = 3.8V I _{OH} = -1.0 mA, V _{DD} = 3.8V, RC option only

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is based on characterization results at 25°C. This data is for design guidance only and is not tested.

- 2: The leakage current on the $\overline{\text{MCLR}}$ /V_{PP} pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltage.
- 3: Negative current is defined as coming out of the pin.
- 4: For the RC option, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16LV5X be driven with external clock in RC mode.
- 5: The user may use the better of the two specifications.

Enhanced PIC16LV5X

5.3 Timing Parameter Symbology and Load Conditions

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS
2. TppS

T			
F	Frequency	T	Time

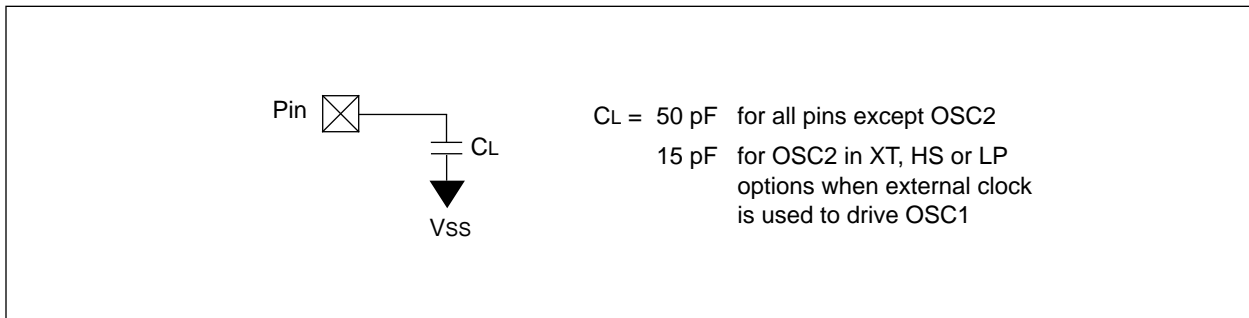
Lowercase subscripts (pp) and their meanings:

pp			
2	to	mc	$\overline{\text{MCLR}}$
ck	CLKOUT	osc	oscillator
cy	cycle time	os	OSC1
drt	device reset timer	t0	T0CKI
io	I/O port	wdt	watchdog timer

Uppercase letters and their meanings:

S			
F	Fall	P	Period
H	High	R	Rise
I	Invalid (Hi-impedance)	V	Valid
L	Low	Z	Hi-impedance

FIGURE 5-1: LOAD CONDITIONS - PIC16LV5XA



5.4 Timing Diagrams and Specifications

FIGURE 5-2: EXTERNAL CLOCK TIMING - PIC16LV5XA

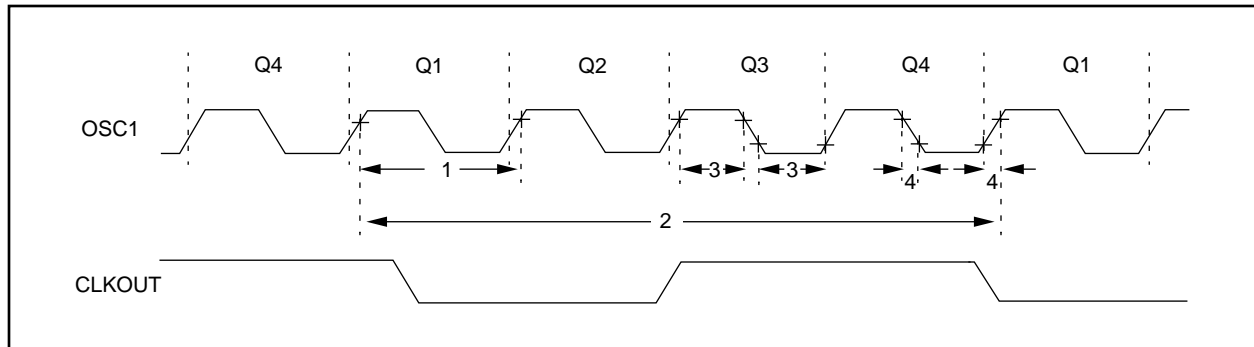


TABLE 5-1: EXTERNAL CLOCK TIMING REQUIREMENTS - PIC16LV5XA

AC Characteristics		Standard Operating Conditions (unless otherwise specified)					
		Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial), $-20^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial)					
		Operating Voltage V_{DD} range is described in Section 10.1, Section 10.2 and Section 10.3 of the Enhanced PIC16C5X data sheet (DS30236B).					
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
	FOSC	External CLKIN Frequency ⁽²⁾	DC	—	2.0	MHz	RC osc mode
			DC	—	2.0	MHz	XT osc mode
			DC	—	200	kHz	LP osc mode
		Oscillator Frequency ⁽²⁾	DC	—	2.0	MHz	RC osc mode
			0.1	—	2.0	MHz	XT osc mode
			5	—	200	kHz	LP osc mode
1	TOSC	External CLKIN Period ⁽²⁾	500	—	—	ns	RC osc mode
			500	—	—	ns	XT osc mode
			5.0	—	—	μs	LP osc mode
		Oscillator Period ⁽²⁾	500	—	—	ns	RC osc mode
			500	—	10,000	ns	XT osc mode
			5.0	—	200	μs	LP osc mode
2	TCY	Instruction Cycle Time ⁽³⁾	—	4/FOSC	—	—	
3	TosL, TosH	Clock in (OSC1) Low or High Time	50*	—	—	ns	XT oscillator
			2.0*	—	—	μs	LP oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT oscillator
			—	—	50*	ns	LP oscillator

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 3.8V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption.

When an external clock input is used, the "max" cycle time limit is "DC" (no clock) for all devices.

3: Instruction cycle period (TCY) equals four times the input oscillator time base period.

Enhanced PIC16LV5X

FIGURE 5-3: CLKOUT AND I/O TIMING - PIC16LV5XA

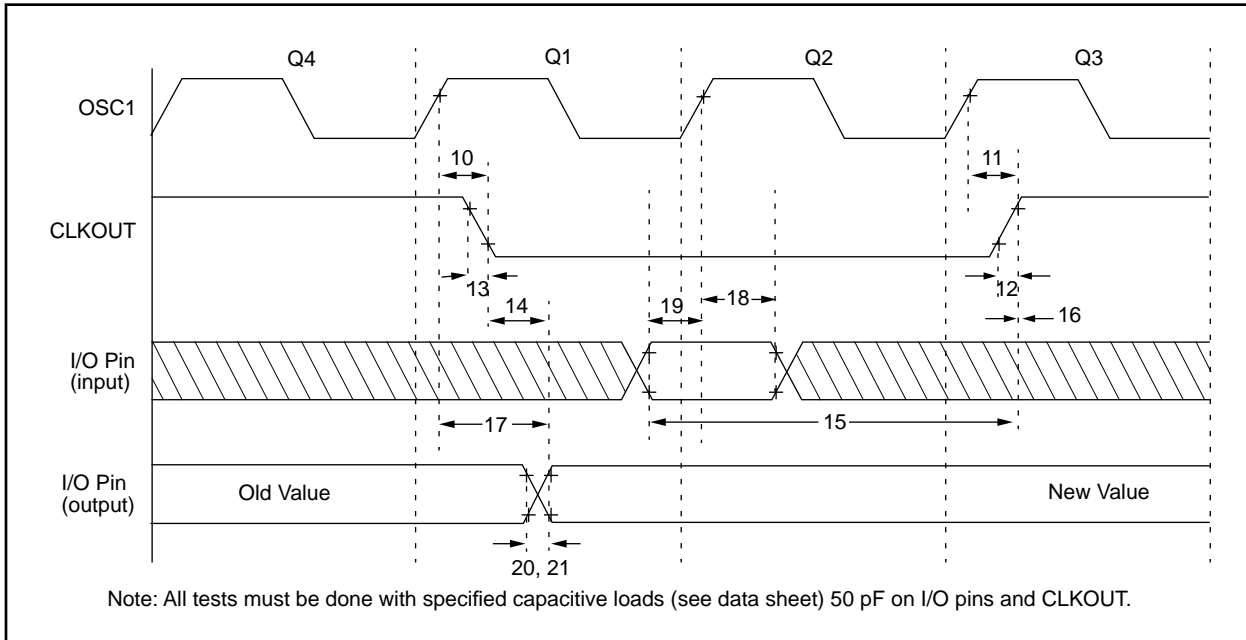


TABLE 5-2: CLKOUT AND I/O TIMING REQUIREMENTS - PIC16LV5XA

AC Characteristics		Standard Operating Conditions (unless otherwise specified)				
		Operating Temperature 0°C ≤ TA ≤ +70°C (commercial), -20°C ≤ TA ≤ +85°C (industrial)				
		Operating Voltage VDD range is described in Section 10.1, Section 10.2 and Section 10.3 of the Enhanced PIC16C5X data sheet (DS30236B).				
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units
10	TosH2ckL	OSC1↑ to CLKOUT↓ ⁽²⁾	—	15	30**	ns
11	TosH2ckH	OSC1↑ to CLKOUT↑ ⁽²⁾	—	15	30**	ns
12	TckR	CLKOUT rise time ⁽²⁾	—	5.0	15**	ns
13	TckF	CLKOUT fall time ⁽²⁾	—	5.0	15**	ns
14	TckL2ioV	CLKOUT↓ to Port out valid ⁽²⁾	—	—	40**	ns
15	TioV2ckH	Port in valid before CLKOUT↑ ⁽²⁾	0.25 Tcy+30*	—	—	ns
16	TckH2iol	Port in hold after CLKOUT↑ ⁽²⁾	0*	—	—	ns
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid ⁽³⁾	—	—	100*	ns
18	TosH2iol	OSC1↑ (Q2 cycle) to Port input invalid (I/O in hold time)	TBD	—	—	ns
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	TBD	—	—	ns
20	TioR	Port output rise time ⁽³⁾	—	10	25**	ns
21	TioF	Port output fall time ⁽³⁾	—	10	25**	ns

* These parameters are characterized but not tested.

** These parameters are design targets and are not tested. No characterization data available at this time.

Note 1: Data in the Typical ("Typ") column is at 3.8V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: Measurements are taken in RC Mode where CLKOUT output is 4 x TOSC.

3: See Figure 5-1 for loading conditions.

FIGURE 5-4: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER TIMING - PIC16LV5XA

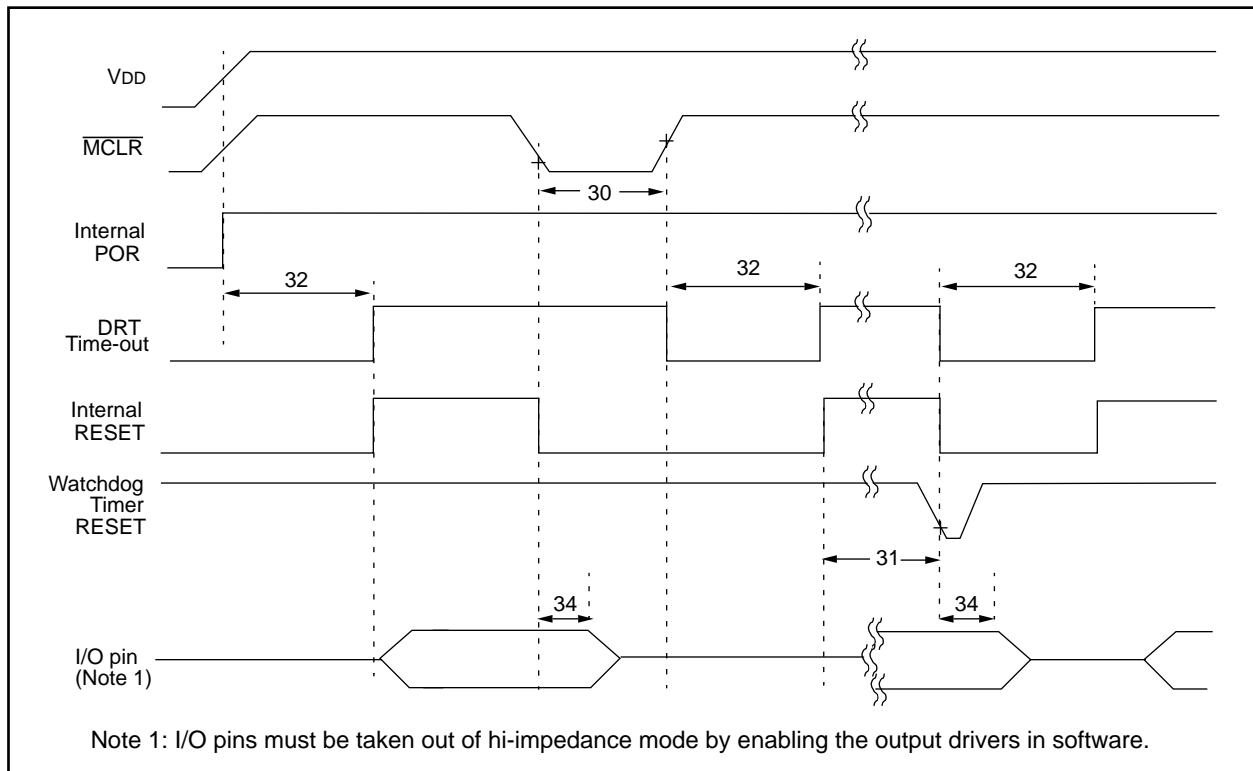


TABLE 5-3: RESET, WATCHDOG TIMER, AND DEVICE RESET TIMER - PIC16LV5XA

AC Characteristics Standard Operating Conditions (unless otherwise specified)							
Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial), $-20^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial)							
Operating Voltage V_{DD} range is described in Section 10.1, Section 10.2 and Section 10.3 of the Enhanced PIC16C5X data sheet (DS30236B).							
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
30	Tmcl	MCLR Pulse Width (low)	100*	—	—	ns	$V_{DD} = 3.8\text{V}$
31	Twdt	Watchdog Timer Time-out Period (No Prescaler)	9.0*	18*	40*	ms	$V_{DD} = 3.8\text{V}$ (Commercial)
32	TDRT	Device Reset Timer Period	9.0*	18*	30*	ms	$V_{DD} = 3.8\text{V}$ (Commercial)
34	Tioz	I/O Hi-impedance from MCLR Low	—	—	100*	ns	

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 3.8V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Enhanced PIC16LV5X

FIGURE 5-5: TIMER0 CLOCK TIMINGS - PIC16LV5XA

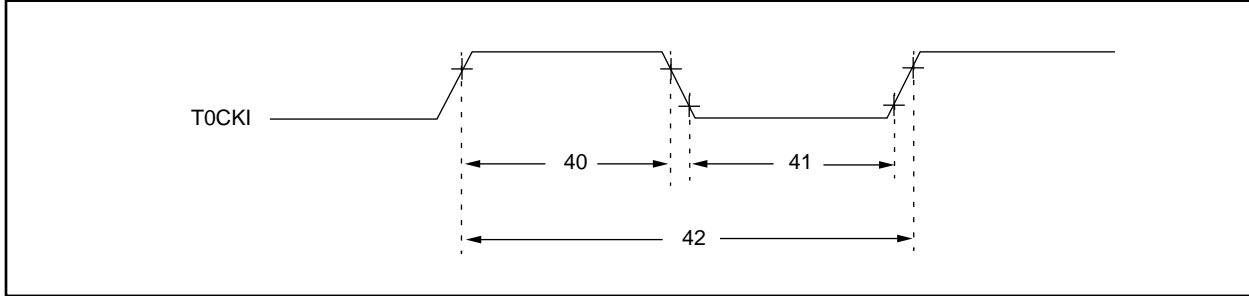


TABLE 5-4: TIMER0 CLOCK REQUIREMENTS - PIC16LV5XA

AC Characteristics		Standard Operating Conditions (unless otherwise specified)					
		Operating Temperature $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$ (commercial), $-20^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ (industrial)					
		Operating Voltage V_{DD} range is described in the Section 10.1, Section 10.2 and Section 10.3 of the Enhanced PIC16C5X data sheet (DS30236B).					
Parameter No.	Sym	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width - No Prescaler	$0.5 T_{CY} + 20^*$	—	—	ns	
		- With Prescaler	10^*	—	—	ns	
41	Tt0L	T0CKI Low Pulse Width - No Prescaler	$0.5 T_{CY} + 20^*$	—	—	ns	
		- With Prescaler	10^*	—	—	ns	
42	Tt0P	T0CKI Period	20 or $\frac{T_{CY} + 40^*}{N}$	—	—	ns	Whichever is greater. N = Prescale Value (1, 2, 4, ..., 256)

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 3.8V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

6.0 DC AND AC CHARACTERISTICS - ENHANCED PIC16LV5X

The graphs and tables provided in this section are for design guidance and are not tested or guaranteed. In some graphs or tables the data presented are outside specified operating range (e.g., outside specified VDD range). This is for information only and devices will operate properly only within the specified range.

The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3 σ) and (mean - 3 σ) respectively, where σ is standard deviation.

Not available at this time.

Enhanced PIC16LV5X

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The following connect procedure applies in most locations:

1. Set your modem to 8-bit, No parity, and One stop (8N1). This is not the normal CompuServe setting which is 7E1.
2. Dial your local CompuServe access number.
3. Depress **<ENTER>** and a garbage string will appear because CompuServe is expecting a 7E1 setting.
4. Type **+**, depress **<ENTER>** and Host Name: will appear.
5. Type **MCHIPBBS**, depress **< ENTER>** and you will be connected to the Microchip BBS.

In the United States, to find CompuServe's phone number closest to you, set your modem to 7E1 and dial (800) 848-4480 for 300-2400 baud or (800) 331-7166 for 9600-14400 baud connection. After the system responds with Host Name:

Type, **NETWORK**, depress **< ENTER>** and follow CompuServe's directions.

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Device: **Enhanced PIC16LV5X** Literature Number: **DS40121A**

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Enhanced PIC16LV5X

ENHANCED PIC16LV5X PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>-XX</u>	<u>X</u>	<u>/XX</u>	<u>XXX</u>	
Device	Frequency Range	Temperature Range	Package	Pattern	
Device	PIC16LV5XA, PIC16LV5XAT ⁽²⁾				
Frequency Range	02	= 2 MHz			
Temperature Range	b ⁽¹⁾	= 0°C to +70°C (Commercial)			
	I	= -20°C to +85°C (Industrial)			
Package	P	= PDIP			
	SO	= SOIC (Gull Wing, 300 mil body)			
	SS	= SSOP (209 mil body)			
Pattern	3-digit Pattern Code for QTP (blank otherwise)				

Examples:

a) PIC16LV54A -02/P 301 = Commercial temp., PDIP package, 2MHz, normal VDD limits, QTP pattern #301.

b) PIC16LV58A - 02I/SO = Industrial temp., SOIC package, 2 MHz, Extended VDD limits.

Note 1: b = blank
2: T = in tape and reel - SOIC, SSOP packages only.

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Products supported by a preliminary Data Sheet may possibly have an errata sheet describing minor operational differences and recommended workarounds. To determine if an errata sheet exists for a particular device, please contact one of the following:

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2. The Microchip Corporate Literature Center U.S. FAX: (602) 786-7277
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Please specify which device, revision of silicon and Data Sheet (include Literature #) you are using.

For latest version information and upgrade kits for Microchip Development Tools, please call 1-800-755-2345 or 1-602-786-7302.

NOTES:

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