PIC18F87J50 FAMILY

PIC18F87J50 Family
Silicon Errata and Data Sheet Clarification

The PIC18F87J50 family devices that you have received conform functionally to the current Device Data Sheet (DS39775**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC18F87J50 family silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A4**).

Data Sheet clarifications and corrections start on page 5, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/ debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC18F87J50 family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)		
		A2	A3	A4
PIC18F65J50	410Xh	2h	3h	3h
PIC18F66J50	414Xh			
PIC18F66J55	416Xh			
PIC18F67J50	418Xh			
PIC18F85J50	41AXh			
PIC18F86J50	41EXh			
PIC18F86J55	420Xh			
PIC18F87J50	422Xh			

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC18F6XJXX/8XJXX Family Flash Microcontroller Programming Specification"* (DS39644) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)		
				A2	A3	A4
MSSP	I^2C™ Slave	1.	With I^2C slave reception, need to read data promptly	X	X	X
MSSP	I^2C Master	2.	With I^2C Master mode, narrow clock width upon slave clock stretch	X	X	X
EUSART	Interrupts	3.	If interrupts are enabled, 2 TCY delay needed after re-enabling the module	X	X	X
MSSP	SPI Master mode	4.	SPI master, write collision for FOSC/64 and Timer2/2	X	X	X
PORTH	RH0, RH1	5.	In certain cases, PMP can override RH0 and RH1	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A4**).

1. Module: MSSP (I^2C™ Slave)

When configured for I^2C™ slave reception, the MSSP module may not receive the correct data, in extremely rare cases. This occurs only if the Serial Receive/Transmit Buffer Register (SSPBUF) is not read after the SSPIF interrupt (PIR1<3>) has occurred, but before the first rising clock edge of the next byte being received.

Work around

The issue can be resolved in either of these ways:

- Prior to the I^2C slave reception, enable the clock stretching feature.

  This is done by setting the SEN bit (SSPCON2<0>).
- Each time the SSPIF is set, read the SSPBUF before the first rising clock edge of the next byte being received.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

2. Module: MSSP (I^2C™ Master)

When in I^2C Master mode, if the slave performs clock stretching, the first clock pulse after the slave releases the SCL line may be narrower than the configured clock width. This may result in the slave missing the first clock in the next transmission/ reception.

Work around

The clock pulse will be the normal width if the slave does not perform clock stretching.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

3. Module: Enhanced Universal Synchronous Asynchronous Receiver Transmitter (EUSART)

In rare situations, when interrupts are enabled, unexpected results may occur if:

- The EUSART is disabled (SPEN bit (RCSTAx<7>) = 0)
- The EUSART is re-enabled (RCSTAx<7> = 1)
- A two-cycle instruction is executed immediately after enabling the module (setting SPEN, CREN or TXEN = 1)

Work around

Add a 2 TCY delay after any instruction that re-enables the EUSART module (ex: sets SPEN = 1). See Example 1.

EXAMPLE 1: RE-ENABLING A EUSART MODULE

```
;Initial conditions: SPEN = 0 (module disabled)
;To re-enable the module:
;Re-Initialize TXSTAx, BAUDCONx, SPBRGx, SPBRGHx registers (if needed)
;Re-Initialize RCSTAx register (if needed), but do not set SPEN = 1 yet

;Now enable the module, but add a 2-Tcy delay before executing any two-cycle
;instructions
bsf    RCSTA1, SPEN ;or RCSTA2 if EUSART2
nop    ;1 Tcy delay
nop    ;1 Tcy delay (two total)

;CPU may now execute 2 cycle instructions
```

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

4. Module: MSSP

With MSSP1 or MSSP2 in SPI Master mode, the FOSC/64 or Timer2/2 clock rate enabled and CKE = 0, a write collision may occur if SSPBUF is loaded immediately after the transfer is complete. A delay may be required before writing SSPBUF, after the MSSP Interrupt Flag bit (SSPIF) is set or the Buffer Full bit (BF) is set. If the delay is insufficiently short, a write collision may occur as indicated by the WCOL bit being set.

Work around

Add a software delay of one SCK period after detecting the completed transfer and prior to updating the SSPBUF contents.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

5. Module: I/O (PORTH)

When the Parallel Master Port (PMP) module is enabled (PMCONH<7> = 1) and the PMPMX bit is clear (CONFIG3L<2> = 0), the PMP module can, under certain conditions, override firmware control over the RH0 and RH1 general purpose I/O (GPIO) pins.

The RH0 and RH1 pins will function normally and can still be used as standard GPIO if the PMP is disabled or the PMPMX Configuration bit is set.

This issue only applies to the 80-pin devices (PIC18F85J50, PIC18F86J50, PIC18F86J55 and PIC18F87J50).

Work around

None.

Affected Silicon Revisions

A2	A3	A4					
X	X	X					

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS39775**B**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Table 28-1: Memory Programming Requirements

On page 430, parameter D132B is renamed, and the minimum and maximum voltage levels and conditions column of the Self-Timed Erase or Write for VDD and VDDCORE for are included. The TWE parameter number and conditions column are changed.

The changed content is indicated in bold text in Table 28-1:

TABLE 28-1: MEMORY PROGRAMMING REQUIREMENTS

DC CHARACTERISTICS			**Standard Operating Conditions (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for industrial				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ†**	**Max**	**Units**	**Conditions**
		Program Flash Memory					
D130	EP	Cell Endurance	10K	—	—	E/W	-40°C to +85°C
D131	VPR	VDDCORE for Read	VMIN	—	3.6	V	VMIN = Minimum operating voltage
D132	VPEW	**Voltage for Self-Timed Erase or Write**					
		VDD	**2.35**	—	**3.6**	V	**ENVREG tied to VDD**
		VDDCORE	**2.25**	—	**2.7**	V	**ENVREG tied to VSS**
D133A	TIW	Self-Timed Write Cycle Time	—	2.8	—	ms	
D133B	TIE	Self-Timed Page Erase Cycle Time	—	33.0	—	ms	
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated
D135	IDDP	Supply Current during Programming	—	10	—	mA	
D140	TWE	Writes per Erase Cycle	—	—	1	—	**For each physical address**

† Data in “Typ” column is at 3.3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2. Module: Table 28-2: Comparator Specifications

On page 431, the maximum Input Offset Voltage (parameter D300) is changed to ±25 mV.

The parameter numbers for TRESP and TMC2OV are changed to D303 and D304, respectively.

A new parameter number, D305, for VIRV is added.

The changed/appended content is indicated in bold text in Table 28-2.

3. Module: Table 28-4: Internal Voltage Regulator Specifications

On page 431, additional comments are provided to help guide selection of an external capacitor.

The changed/appended content is indicated in bold text in Table 28-4.

TABLE 28-2: COMPARATOR SPECIFICATIONS

Operating Conditions: 3.0V < VDD < 3.6V, -40°C < TA < +85°C (unless otherwise stated)							
Param No.	**Sym**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
D300	VIOFF	Input Offset Voltage	—	±5.0	**±25**	mV	
D301	VICM	Input Common Mode Voltage	0	—	AVDD – 1.5	V	
D302	CMRR	Common Mode Rejection Ratio	55	—	—	dB	
D303	TRESP	Response Time**(1)**	—	150	400	ns	
D304	TMC2OV	Comparator Mode Change to Output Valid	—	—	10	μs	
D305	**VIRV**	**Internal Reference Voltage**	**—**	**1.2**	**—**	**V**	

Note 1: Response time measured with one comparator input at (VDD – 1.5)/2, while the other input transitions from VSS to VDD.

TABLE 28-4: INTERNAL VOLTAGE REGULATOR SPECIFICATIONS

Operating Conditions: -40°C < TA < +85°C (unless otherwise stated)							
Param No.	**Sym**	**Characteristics**	**Min**	**Typ**	**Max**	**Units**	**Comments**
	VRGOUT	Regulator Output Voltage	2.45	2.5	—	V	VDD, ENVREG = 3.0V
	CEFC	External Filter Capacitor Value**(1)**	4.7**(2)**	10	—	μF	**Capacitor must be low series resistance (<5Ω)**

Note 1: CEFC applies when the internal regulator is enabled (ENVREG = VDD). When the regulator is disabled (ENVREG = VSS), there is no minimum or maximum capacitance, but good supply rail bypassing should still be practiced.

2: If the regulator is enabled and the VDD supply rail has moderate ripple voltage, it is recommended that more than the minimum CEFC be used.

4. Module: Section 28.3 "DC Characteristics: PIC18F87J50 family (Industrial)"

On page 428, the characteristics and conditions of the Input Leakage Current are updated for the Analog (D060) and included for the Digital (D060A) I/O ports.

The changed content is indicated in bold text in the "DC CHARACTERISTICS" table.

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial			
Param No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**	**Conditions**
	VIL	**Input Low Voltage**				
		All I/O ports:				
D030		with TTL buffer	VSS	0.15 VDD	V	VDD < 3.3V
D030A			—	0.8	V	3.3V ≤ VDD ≤ 3.6V
D031		with Schmitt Trigger buffer	VSS	0.2 VDD	V	
D032		$\overline{MCLR}$	VSS	0.2 VDD	V	
D033		OSC1	VSS	0.3 VDD	V	HS, HSPLL modes
D033A		OSC1	VSS	0.2 VDD	V	EC, ECPLL modes
D034		T1CKI	VSS	0.3	V	
	VIH	**Input High Voltage**				
		I/O ports with non 5.5V tolerance:(2)				
D040		with TTL buffer	0.25 VDD + 0.8V	VDD	V	VDD < 3.3V
D040A			2.0	VDD	V	3.3V ≤ VDD ≤ 3.6V
D041		with Schmitt Trigger buffer	0.8 VDD	VDD	V	
		I/O ports with 5.5V tolerance:(2)				
Dxxx		with TTL buffer	0.25 VDD + 0.8V	5.5	V	VDD < 3.3V
DxxxA			2.0	5.5	V	3.3V ≤ VDD ≤ 3.6V
Dxxx		with Schmitt Trigger buffer	0.8 VDD	5.5	V	
D042		$\overline{MCLR}$	0.8 VDD	VDD	V	
D043		OSC1	0.7 VDD	VDD	V	HS, HSPLL modes
D043A		OSC1	0.8 VDD	VDD	V	EC, ECPLL modes
D044		T1CKI	1.6	VDD	V	
	IIL	**Input Leakage Current(1)**				
D060		**I/O ports with non 5.5V tolerance:(2)**	—	±1	μA	VSS ≤ VPIN ≤ VDD, Pin at high-impedance
D060A		**I/O ports with 5.5V tolerance:(2)**	**—**	**±1**	**μA**	**VSS ≤ VPIN ≤ 5.5V, Pin at high-impedance**
D061		$\overline{MCLR}$	—	±1	μA	Vss ≤ VPIN ≤ VDD
D063		OSC1	—	±5	μA	Vss ≤ VPIN ≤ VDD

Note 1: Negative current is defined as current sourced by the pin.

2: Refer to Table 10-1 for the pins that have corresponding tolerance limits.

5. Module: Section 19.3 “SPI Mode” and Section 19.4 “I²C™ Mode”

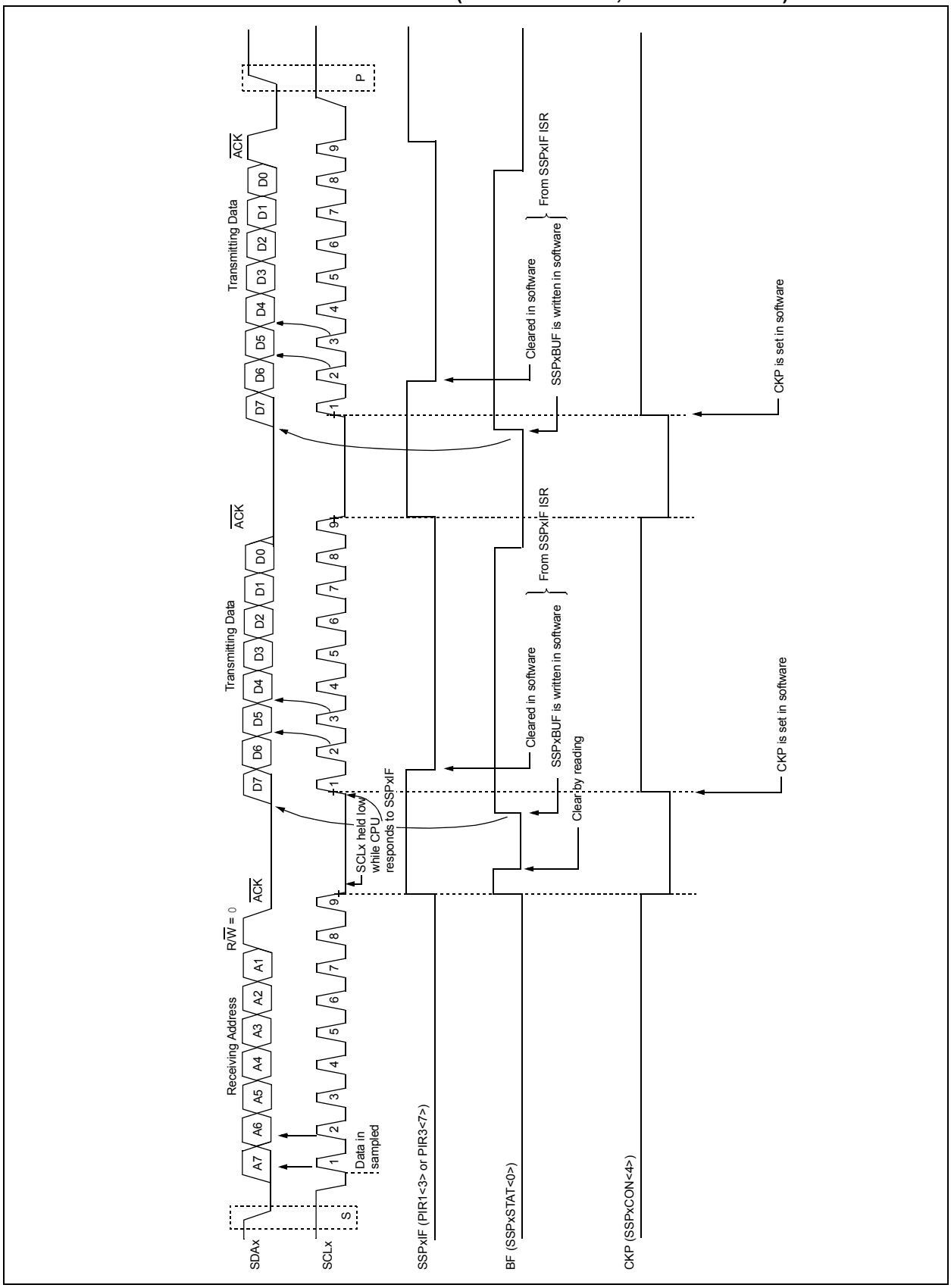
In **Section 19.3 “SPI Mode”** on page 231 and **Section 19.4 “I²C™ Mode”** on page 241, the following note is added to describe the procedure to disable the MSSP module:

Note:	Disabling the MSSP module by clearing the SSPEN bit (SSPxCON1<5>) may not reset the module. It is recommended to clear the SSPxSTAT, SSPxCON1 and SSPxCON2 registers and select the mode prior to setting the SSPEN bit to enable the MSSP module.

6. Module: Figure 19-10: I²C™ Slave Mode Timing (Transmission, 7-Bit Address)

On page 252, the figure is replaced with the new timing diagram provided in Figure 19-10.

FIGURE 19-10: I²C™ SLAVE MODE TIMING (TRANSMISSION, 7-BIT ADDRESS)

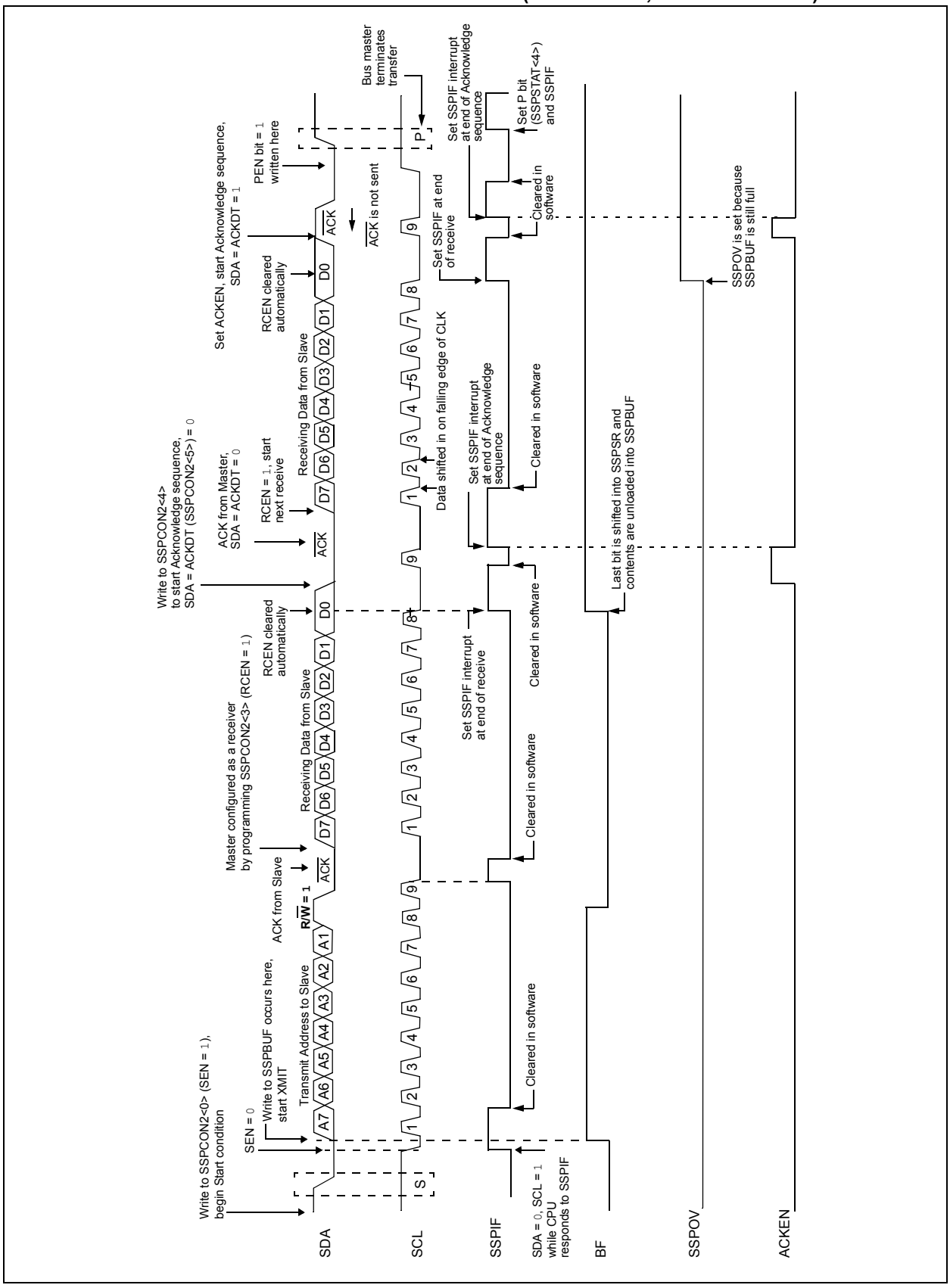


7. Module: Figure 19-24: I²C™ Master Mode Waveform (Reception, 7-Bit Address)

On page 269, the condition, R/$\overline{W}$, when the Acknowledge signal (ACK) is received from the slave, after transmitting the address to the slave, is changed to '1'.

The changed value is indicated in bold text in Figure 19-24.

FIGURE 19-24: I²C™ MASTER MODE WAVEFORM (RECEPTION, 7-BIT ADDRESS)



8. Module: MSSP (SPI Master)

In **Section 19.3.6, "Master Mode,"** the following content is added:

When used in Timer2 Output/2 mode, the SPI bit rate can be configured using the PR2 Period register and the Timer2 prescaler.

To operate in this mode, firmware must first initialize and enable the Timer2 module before it can be used with the MSSP. Once enabled, the Timer2 module is free running and mostly independent of the MSSP module.

Writing to the SSPxBUF register will not clear the current TMR2 value in hardware. This can result in an unpredictable SPI transmit MSb bit width, depending on how close the TMR2 register was to the PR2 match condition at the moment that the firmware wrote to SSPxBUF.

To avoid the unpredictable MSb bit width, initialize the TMR2 register to a known value when writing to SSPxBUF. An example procedure, which provides predictable bit widths (only needed in the Timer2/2 mode), is given in Example 2. The example procedure demonstrates operation with MSSP1, but the concepts apply equally to MSSP2.

EXAMPLE 2: LOADING SSPxBUF WITH THE TIMER2/2 CLOCK MODE

```
TransmitSPI:
BCF     PIR1, SSP1IF    ;Make sure interrupt flag is clear (may have been set from previous
                        ;transmission)
MOVF    SSP1BUF, W      ;Perform read, even if the data in SSPBUF is not important
MOVWF   RXDATA          ;Save previously received byte in user RAM, if the data is meaningful
BCF     T2CON, TMR2ON   ;Turn off timer when loading SSPBUF
CLRF    TMR2            ;Set timer to a known state
MOVF    TXDATA, W       ;WREG = Contents of TXDATA (user data to send)
MOVWF   SSP1BUF         ;Load data to send into transmit buffer
BSF     T2CON, TMR2ON   ;Start timer to begin transmission

WaitComplete:           ;Loop until data has finished transmitting
BTFSS   PIR1, SSP1IF    ;Interrupt flag set when transmit is complete
BRA     WaitComplete
```

9. Module: OSCTUNE Register

The second paragraph of **Section 2.2.5.1 "OSCTUNE Register"** is modified as indicated:

When the OSCTUNE register is modified, the INTOSC frequency begins shifting to the new value. The INTOSC clock stabilizes within 1 ms.

Code execution continues during this shift. There is no indication that the shift has occurred.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (9/2009)

Initial release of the combined, silicon errata/data sheet clarification document. New silicon issues 4 (MSSP) and 5 (I/O – PORTH). New data sheet clarifications 8 (MSSP – SPI Master) and 9 (OSCTUNE Register).

This document replaces these errata documents:

- DS80321B, *"PIC18F87J50 Family Rev. A2 Silicon Errata"*
- DS80415A, *"PIC18F87J50 Family Rev. A3 Silicon Errata"*
- DS80409B, *"PIC18F87J50 Family Data Sheet Errata"*

NOTES:

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