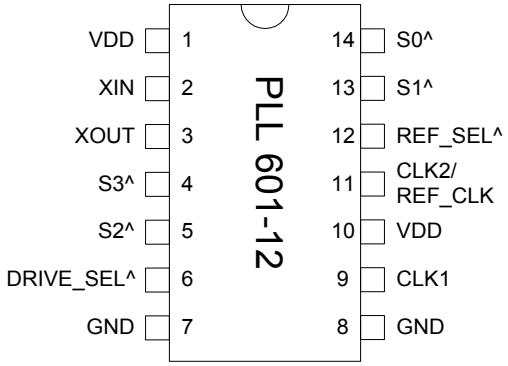
PLL601-12

Dual Output PLL Clock with Selectable Odd Multiplier

FEATURES

- Selectable multipliers (x2.5, x2.75, x3, x4.25, x5, x5.5, x5.75, x6, x6.25, x10, x11, x11.5, x12, x12.5).
- Crystal input range, 13MHz to 31MHz (see Selection Table for detailed acceptable input ranges).
- Maximum output frequency: 312.5MHz
- 2 CMOS outputs.
- Selectable output drive (Standard or High-Drive).
- Selectable REF_CLK output.
- 3.3V operation.
- Available in 14-Pin SOIC.

PIN CONFIGURATION
(Top View)

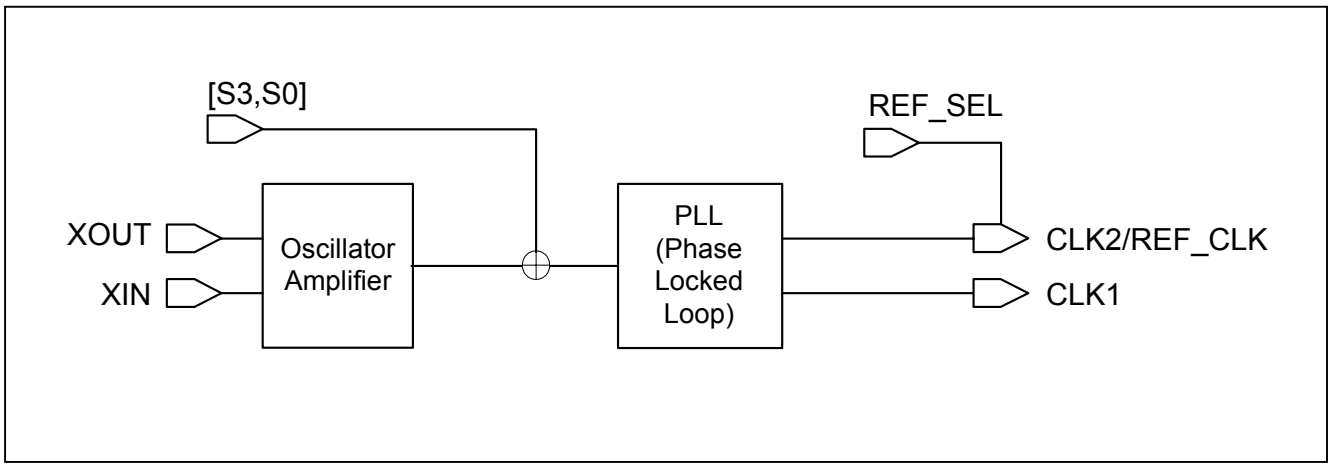


^: Internal pull-up.

DESCRIPTION

The PLL601-12 is a highly flexible XO with selectable multipliers and two CMOS outputs (one of which can be selected to be REF_CLK). Thanks to PhaseLink's advanced Phase Locked Loop technology, it allows a wide choice of selectable multipliers that permits the user to achieve useful frequencies from standard low cost crystals. It accepts fundamental parallel resonant mode crystals from 13 to 31MHz, and is ideal to generate 156.25MHz from a standard 25MHz crystal.

BLOCK DIAGRAM



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FREQUENCY SELECTION TABLE

S3	S2	S1	S0	Xtal Min	Xtal Max	Multiplier
0	0	0	0			Reserved
0	0	0	1			Reserved
0	0	1	0	19	36	X 4.25
0	0	1	1	15	28	X 11
0	1	0	0	14	26	X 12
0	1	0	1	13	25	X 12.5
0	1	1	0	14	27	X 5.75
0	1	1	1	14	26	X 3
1	0	0	0	14	27	X 11.5
1	0	0	1	15	28	X 5.5
1	0	1	0	15	28	X 2.75
1	0	1	1	16	31	X 5
1	1	0	0	16	31	X 2.5
1	1	0	1	16	31	X 10
1	1	1	0	14	26	X 6
1	1	1	1	13	25	X 6.25

Note: Internal pull-ups default S3, S2, S1, and S0 to '1' when not connected

PIN DESCRIPTIONS

Name	Pin #	Type	Description
VDD	1,11	P	Power Supply.
XIN	2	I	Crystal input.
XOUT	3	I	Crystal output.
S3	4	I	Multiplier selector pins. These pins have an internal pull-up that will default SEL to '1' when not connected to GND.
S2	5	I	
DRIVE_SEL	6	I	Selector pin. If DRIVE_SEL is '0', outputs are at high drive. If '1' or not connected, outputs are standard drive (internal pull-up).
GND	7,8	P	Ground.
CLK1	9	O	CLK1 output is the output of the reference frequency (crystal) after multiplication through the Phase Locked Loop.
CLK2/REF_CLK	10	O	CLK2 or REF_CLK output (depending on REF_SEL). CLK2 is in phase and at the same frequency as CLK1. REF_CLK provides the same output as the crystal reference.
REF_SEL	12	I	Selector pin. This pin if set to '0' selects REF_CLK on pin 10. If not connected, it defaults to '1' (pin 10 = CLK2). Internal pull-up.
S1	13	I	Multiplier selector pins. These pins have an internal pull-up that will default SEL to '1' when not connected to GND.
S0	14	I	

ELECTRICAL SPECIFICATIONS

1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	V_{DD}		4.6	V
Input Voltage, dc	V_I	-0.5	V_{DD}+0.5	V
Output Voltage, dc	V_O	-0.5	V_{DD}+0.5	V
Storage Temperature	T_S	-65	150	°C
Ambient Operating Temperature*	T_A	-40	85	°C
Junction Temperature	T_J		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

* **Note**: Operating Temperature is guaranteed by design for all parts (COMMERCIAL and INDUSTRIAL), but tested for COMMERCIAL grade only.

2. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	F_{XIN}	Parallel Fundamental Mode (see Selection Table)	13		31	MHz
Crystal Loading Rating	$C_{L\ (xtal)}$	At VCON = 1.65V		16		pF
Recommended ESR	R_E	AT cut			30	Ω

3. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
Supply Current, Dynamic (with Loaded Outputs)	I_{DD}	15 pF load	Fout<30MHz			15	mA
			30MHz<Fout<100MHz			30	
			Fout >100MHz			40	
Operating Voltage	V_{DD}			2.97		3.63	V
Short Circuit Current					±50		mA

4. AC Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Clock Rise Time		0.8V ~ 2.0V with 10 pF load			1.5	ns
		0.3V ~ 3.0V with 15 pF load		3.7	5	
Output Clock Fall Time		2.0V ~ 0.8V with 10 pF load			1.5	
		3.0V ~ 0.3V with 15pF load		3.7	5	
Output Clock Duty Cycle		Measured @ 1.4V	45	50	55	%

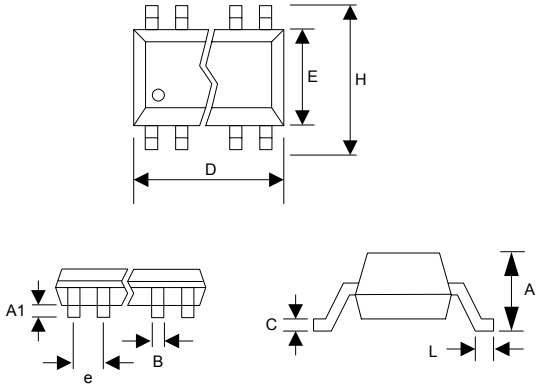
5. Jitter Specifications

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Max. Absolute Jitter, peak-to-peak	Short term		60	100	ps
Max. Jitter, cycle to cycle				60	ps
Phase Noise, relative to carrier, 125Mhz(x5)	100 Hz offset		105		dBc/Hz
Phase Noise, relative to carrier, 125Mhz(x5)	1kHz offset		125		dBc/Hz
Phase Noise, relative to carrier, 125Mhz(x5)	10kHz offset		130		dBc/Hz
Phase Noise, relative to carrier, 125Mhz(x5)	100kHz offset		125		dBc/Hz

PACKAGE INFORMATION

14 PIN Narrow SOIC (mm)

	SOIC	
Symbol	Min.	Max.
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	8.58	8.69
E	3.85	3.97
H	5.80	6.20
L	0.40	1.27
e	1.27 BSC	



ORDERING INFORMATION

For part ordering, please contact our Sales Department:
47745 Fremont Blvd., Fremont, CA 94538, USA
Tel: (510) 492-0990 Fax: (510) 492-0991

PART NUMBER
The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range

PLL601-12 S C

PART NUMBER

TEMPERATURE
C=COMMERCIAL
I=INDUSTRAL

PACKAGE TYPE
S=SOIC

Order Number	Marking	Package Option
PLL601-12SC	P601-12SC	16-Pin SOIC (Tube)
PLL601-12SC-R	P601-12SC	16-Pin SOIC (Tape & Reel)