Programmable logic array (22 × 42 × 10)

PLS173

DESCRIPTION

The PLS173 is a two-level logic element consisting of 42 AND gates and 10 OR gates with fusible link connections for programming I/O polarity and direction.

All AND gates are linked to 12 inputs (I) and 10 bidirectional I/O lines (B). These yield variable I/O gate configurations via 10 direction control gates (D), ranging from 22 inputs to 10 outputs.

On-chip T/C buffers couple either True (I, B) or Complement ($\overline{I}$, $\overline{B}$) input polarities to all AND gates, whose outputs can be optionally linked to all OR gates. Their output polarity, in turn, is individually programmable through a set of EX-OR gates for implementing AND/OR or AND/NOR logic functions.

The PLS173 is field programmable, enabling the user to quickly generate custom patterns using standard programming equipment.

Order codes for this device are listed below.

FEATURES

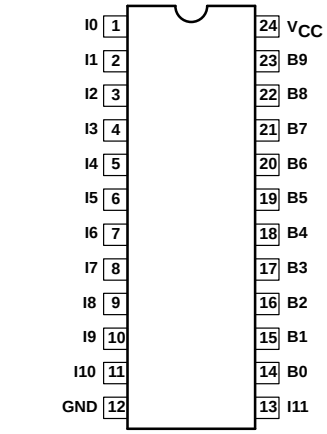
- I/O propagation delay: 30ns (max.)
- 12 inputs
- 42 AND gates
- 10 OR gates
- 10 bidirectional I/O lines
- Active-High or -Low outputs
- 42 product terms:
  - 32 logic terms
  - 10 control terms
- Ni-Cr programmable links
- Input loading: –100μA (max.)
- Power dissipation: 750mW (typ.)
- 3-State outputs
- TTL compatible

APPLICATIONS

- Random logic
- Code converters
- Fault detectors
- Function generators
- Address mapping
- Multiplexing

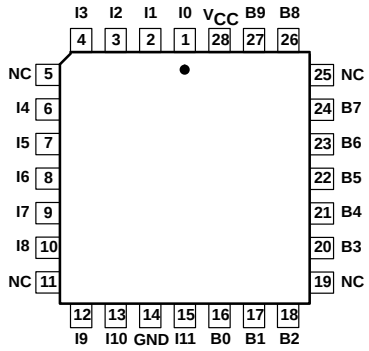
PIN CONFIGURATIONS

N Package



N = Plastic DIP (300mil-wide)

A Package



A = Plastic Leaded Chip Carrier

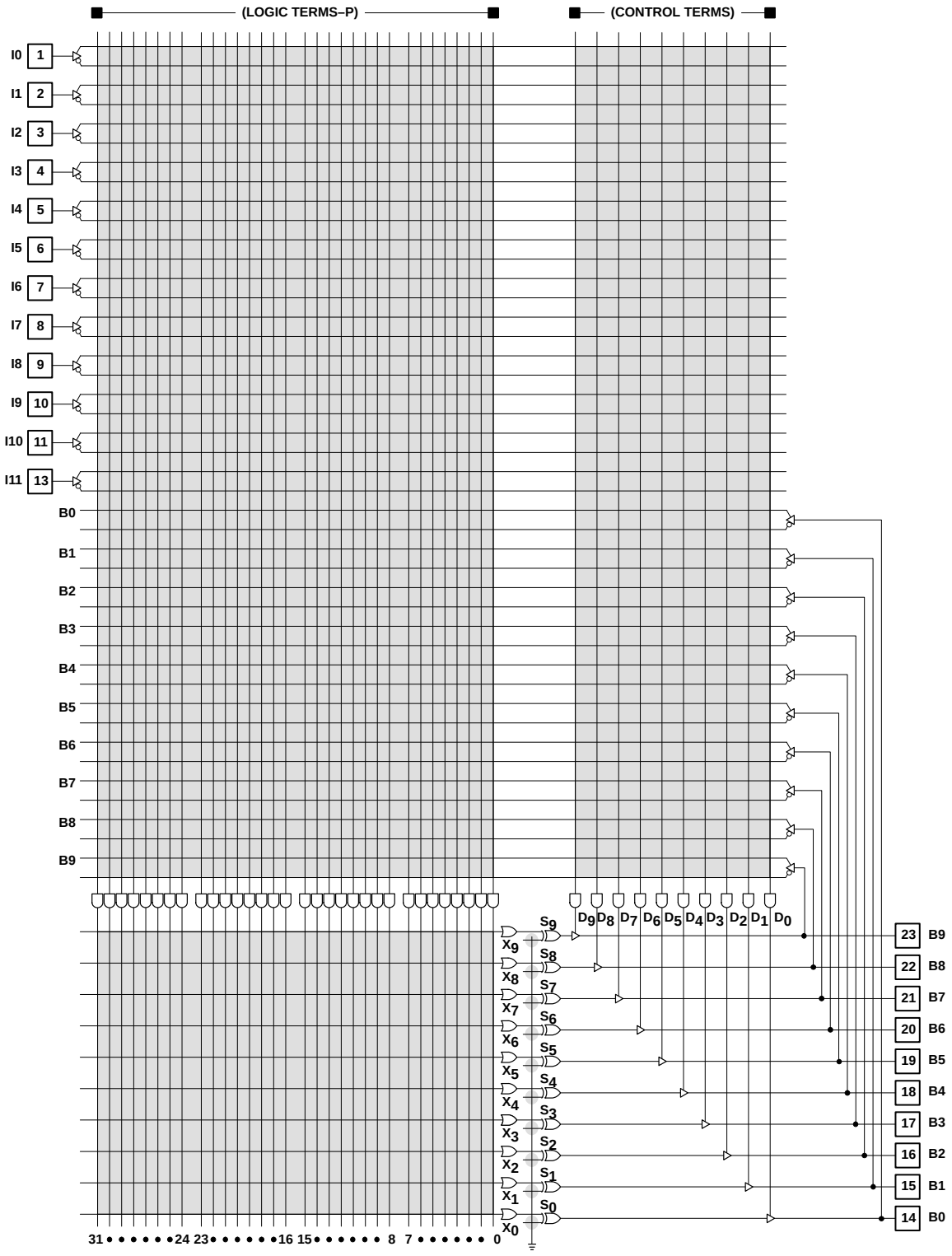
ORDERING INFORMATION

DESCRIPTION	ORDER CODE	DRAWING NUMBER
24-Pin Plastic Dual-In-Line 300mil-wide	PLS173N	0410D
28-Pin Plastic Leaded Chip Carrier	PLS173A	0401F

Programmable logic array ($22 \times 42 \times 10$)

PLS173

LOGIC DIAGRAM

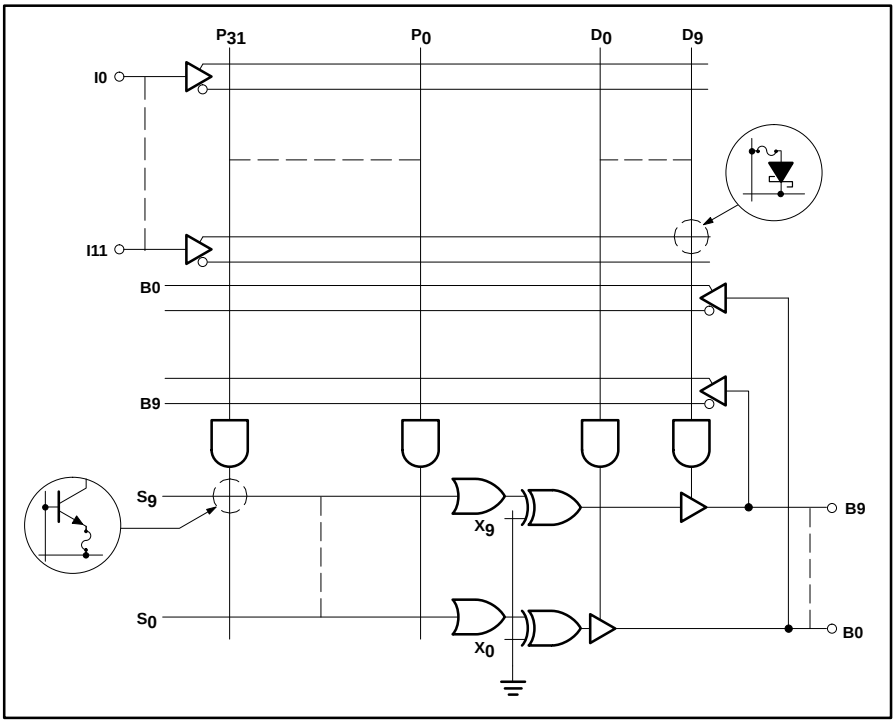


NOTES:
1. All programmed 'AND' gate locations are pulled to logic "1".
2. All programmed 'OR' gate locations are pulled to logic "0".
3. ● Programmable connection.

Programmable logic array ($22 \times 42 \times 10$)

PLS173

FUNCTIONAL DIAGRAM



LOGIC FUNCTION

TYPICAL PRODUCT TERM:

$Pn = A \cdot \overline{B} \cdot C \cdot D \cdot \ldots$

TYPICAL LOGIC FUNCTION:

AT OUTPUT POLARITY = H

$Z = P0 + P1 + P2 \ldots$

AT OUTPUT POLARITY + L

$Z = \overline{P0 + P1 + P2 + \ldots}$

$Z = \overline{P0} \cdot \overline{P1} \cdot \overline{P2} \cdot \ldots$

NOTES:

1. For each of the 10 outputs, either function Z (Active-High) or $\overline{Z}$ (Active-Low) is available, but not both. The desired output polarity is programmed via the EX-OR gates.
2. ZX, A, B, C, etc. are user defined connections to fixed inputs (I), and bidirectional pins (B).

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATING		UNIT
		Min	Max	
V_{CC}	Supply voltage		+7	V_{DC}
V_{IN}	Input voltage		+5.5	V_{DC}
V_{OUT}	Output voltage		+5.5	V_{DC}
I_{IN}	Input currents	–30	+30	mA
I_{OUT}	Output currents		+100	mA
T_{amb}	Operating free-air temperature range	0	+75	°C
T_{stg}	Storage temperature range	–65	+150	°C

NOTES:

1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

TEMPERATURE	
Maximum junction	150°C
Maximum ambient	75°C
Allowable thermal rise ambient to junction	75°C

The PLS173 is also processed to military requirements for operation over the military temperature range. For specifications and ordering information, consult the Philips Semiconductors Military Data Handbook.

DC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75 \le V_{CC} \le 5.25V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP[1]	MAX	
Input voltage[2]						
V_{IL}	Low	V_{CC} = MIN			0.8	V
V_{IH}	High	V_{CC} = MAX	2.0			V
V_{IC}	Clamp[3]	V_{CC} = MIN, I_{IN} = –12mA		–0.8	–1.2	V
Output voltage[2]						
		V_{CC} = MIN				
V_{OL}	Low[4]	I_{OL} = 15mA			0.5	V
V_{OH}	High[5]	I_{OH} = –2mA	2.4			V
Input current[9]						
		V_{CC} = MAX				
I_{IL}	Low	V_{IN} = 0.45V			–100	µA
I_{IH}	High	V_{IN} = V_{CC}			40	µA
Output current						
		V_{CC} = MAX				
$I_{O(OFF)}$	Hi-Z state[8]	V_{OUT} = 5.5V			80	µA
		V_{OUT} = 0.45V			–140	
I_{OS}	Short circuit[3, 5, 6]	V_{OUT} = 0V	–15		–70	mA
I_{CC}	V_{CC} supply current[7]	V_{CC} = MAX		150	170	mA
Capacitance						
		V_{CC} = 5V				
I_{IN}	Input	V_{IN} = 2.0V		8		pF
C_B	I/O	V_B = 2.0V		15		pF

NOTES:
1. All typical values are at V_{CC} = 5V, T_{amb} = +25°C.
2. All voltage values are with respect to network ground terminal.
3. Test one at a time.
4. Measured with inputs V_{IL} applied to I_{11}. Pins 1–5 = 0V, Pins 6–10 = 4.5V, Pin 11 = 0V and Pin 13 = 10V.
5. Same conditions as Note 4 except Pin 11 = +10V.
6. Duration of short circuit should not exceed 1 second.
7. I_{CC} is measured with I_0 and I_1 = 0V, and $I_2 – I_{11}$ and $B_0 – B_9$ = 4.5V. Part in Virgin State.
8. Leakage values are a combination of input and output leakage.
9. I_{IL} and I_{IH} limits are for dedicated inputs only ($I_0 – I_{11}$).

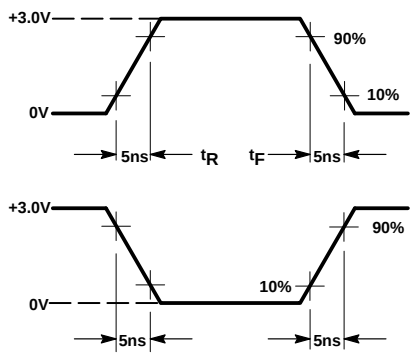
AC ELECTRICAL CHARACTERISTICS

$0°C \le T_{amb} \le +75°C$, $4.75 \le V_{CC} \le 5.25V$, $R_1 = 470\Omega$, $R_2 = 1k\Omega$

SYMBOL	PARAMETER	FROM	TO	TEST CONDITION	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
t_{PD}	Propagation delay[2]	Input ±	Output ±	C_L = 30pF		20	30	ns
t_{OE}	Output enable[1]	Input ±	Output –	C_L = 30pF		20	30	ns
t_{OD}	Output disable[1]	Input ±	Output +	C_L = 5pF		20	30	ns

NOTES:
1. For 3-State output; output enable times are tested with C_L = 30pF to the 1.5V level, and S_1 is open for high-impedance to High tests and closed for high-impedance to Low tests. Output disable times are tested with C_L = 5pF. High-to-High impedance tests are made to an output voltage of $V_T = (V_{OH} – 0.5V)$ with S_1 open, and Low-to-High impedance tests are made to the $V_T = (V_{OL} + 0.5V)$ level with S_1 closed.
2. All propagation delays are measured and specified under worst case conditions.

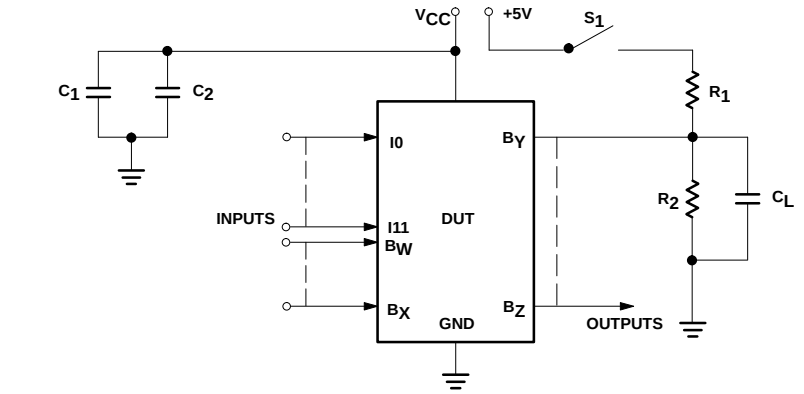
VOLTAGE WAVEFORM



MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

Input Pulses

TEST LOAD CIRCUIT

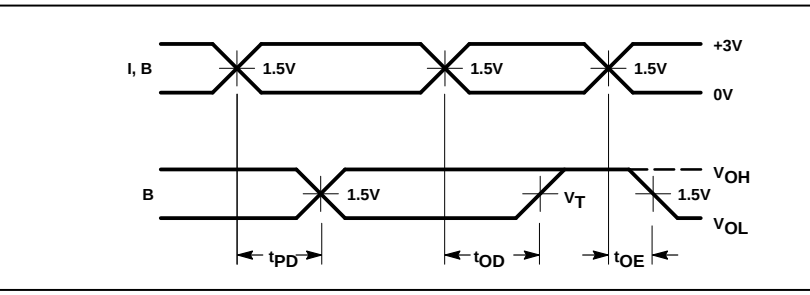


NOTE:
C_1 and C_2 are to bypass V_{CC} to GND.

TIMING DEFINITIONS

SYMBOL	PARAMETER
t_{PD}	Propagation delay between input and output.
t_{OD}	Delay between input change and when output is off (Hi-Z or High).
t_{OE}	Delay between input change and when output reflects specified output level.

TIMING DIAGRAM



Programmable logic array ($22 \times 42 \times 10$)

PLS173

LOGIC PROGRAMMING

The PLS173 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Philips Semiconductors SNAP, Data I/O Corporation's ABEL™, and Logical Devices Incorporated's CUPL™ design software packages.

All packages allow Boolean and state equation entry formats. SNAP, ABEL and CUPL also accept, as input, schematic capture format.

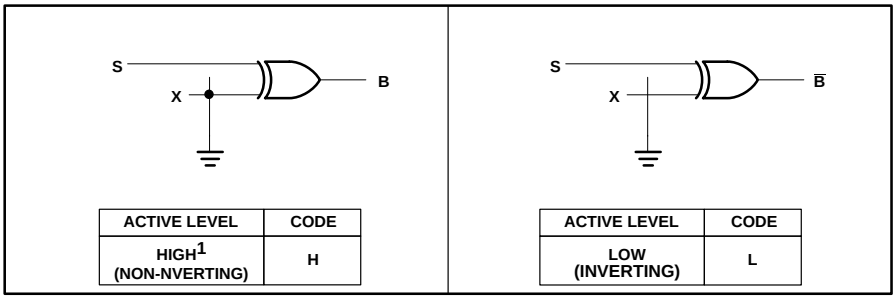
PLS173 logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Philips Semiconductors SNAP PLD design software package.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

PROGRAMMING AND SOFTWARE SUPPORT

Refer to Section 9 *(Development Software)* and Section 10 *(Third-Party Programmer/Software Support)* of this data handbook for addtional information.

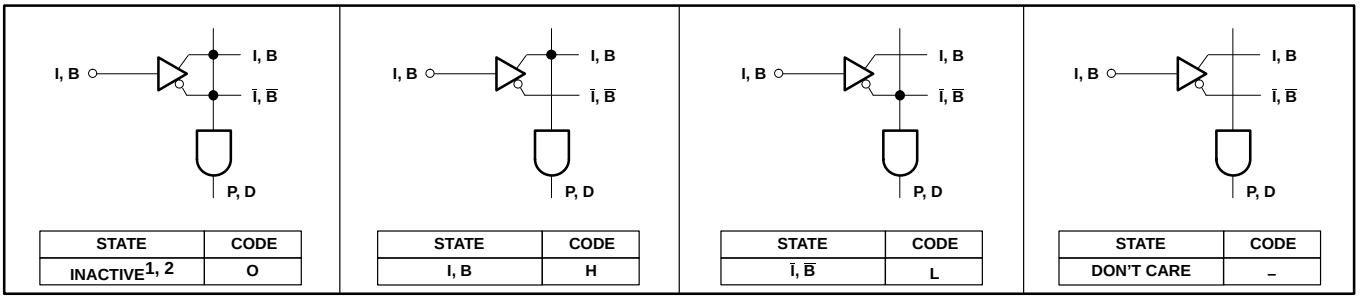
OUTPUT POLARITY – (B)



ACTIVE LEVEL	CODE
HIGH[1] (NON-NVERTING)	H

ACTIVE LEVEL	CODE
LOW (INVERTING)	L

AND ARRAY – (I, B)



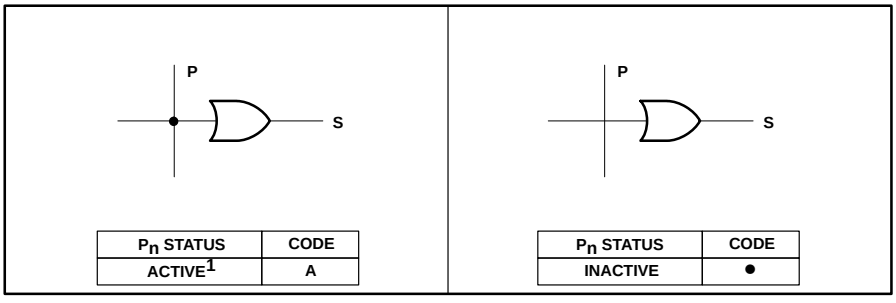
STATE	CODE
INACTIVE[1, 2]	O

STATE	CODE
I, B	H

STATE	CODE
$\overline{I}$, $\overline{B}$	L

STATE	CODE
DON'T CARE	–

OR ARRAY – (B)



P_n STATUS	CODE
ACTIVE[1]	A

P_n STATUS	CODE
INACTIVE	•

NOTES:
1. This is the initial unprogrammed state of all link pairs. It is normally associated with all unused (inactive) AND gates P_n, D_n.
2. Any gate P_n, D_n will be unconditionally inhibited if both the True and Complement of any input (I, B) are left intact.

VIRGIN STATE

A factory shipped virgin device contains all fusible links intact, such that:

1. All outputs are at "H" polarity.
2. All P_n terms are disabled.
3. All P_n terms are active on all outputs.

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CUPL is a trademark of Logical Devices, Inc.

Programmable logic array ($22 \times 42 \times 10$)

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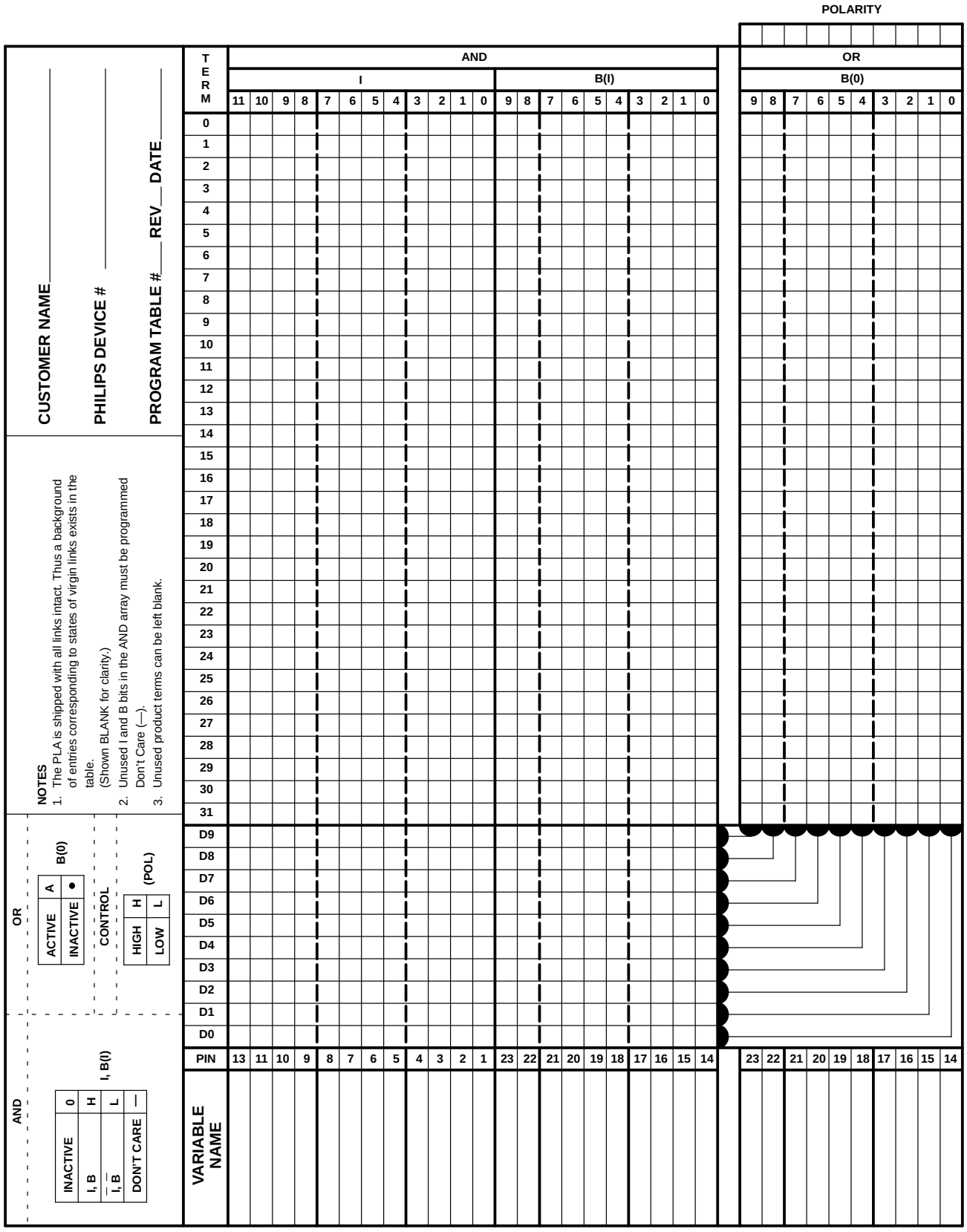
PROGRAM TABLE



Programmable logic array ($22 \times 42 \times 10$)

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SNAP RESOURCE SUMMARY DESIGNATIONS