Octal T1 Framer

FEATURES

- Monolithic single-chip device that integrates eight datacom T1 framers and transmitters for terminating duplex DS1 signals.
- Supports DS1 signals in SF, ESF, or unframed modes.
- Provides ESF bit-oriented code detection/generation, and an HDLC interface for terminating/generating the ESF datalink.
- Supports transfer of PCM data to/from 1.544 Mbit/s or 2.048 Mbit/s backplane buses. Supports fractional T1 backplane interface with asymmetric transmit/receive $n \times$ DS0 rates.
- Supports robbed-bit signaling extraction and insertion on a per-DS0 basis.
- Provides programmable idle code substitution and data inversion on a per-channel basis.
- Provides per-DS0 line loopback and per-link diagnostic and line loopbacks.
- Provides trunk conditioning which forces programmable trouble code substitution on all/selected channels.
- Supports a Pseudo Random Binary Sequence (PRBS) generator and detector which may be configured for insertion/detection on a $n \times$ DS0 basis.
- Supports a 1-second polling interval for access to T1 performance monitoring and HDLC datalinks.
- Pin-compatible to the PM6388 EOCTL Octal E1 Framer.
- Software-compatible with the PM4341A T1XC Single T1 Transceiver, the PM4344 TQUAD Quad T1 Framer, the PM6388 EOCTL Octal E1 Framer and the PM4351 COMET Single T1/E1 Transceiver.
- Seamless interface to the PM7364 FREEDM-32 HDLC controller, the PM7366 FREEDM-8 HDLC controller, the PM8313 D3MX single-chip M13 multiplexer, and the PM4314 QDSX quad line interface unit.
- Provides an 8-bit microprocessor bus interface for configuration, control, and status monitoring.
- Low power 3.3V CMOS technology with 5 V tolerant inputs.
- Supports standard 5-signal P1149.1 JTAG boundary scan.
- Available in a rectangular 128-pin PQFP 14 by 20 mm package.

RECEIVE SECTION

- Accepts gapped data streams to support higher rate demultiplexing.
- Provides red, yellow, and Alarm Indication Signal (AIS) alarm detection.
- Supports Line and Path performance monitoring according to AT&T and ANSI specifications. Accumulators are provided for counting ESF CRC-6 errors, Framing bit errors and Loss Of Frame (LOF) or change of frame alignment events.
- Extracts the ESF datalink, provides 128 bytes of FIFO buffering per datalink.
- Provides a 2-frame buffer for jitter and wander attenuation.

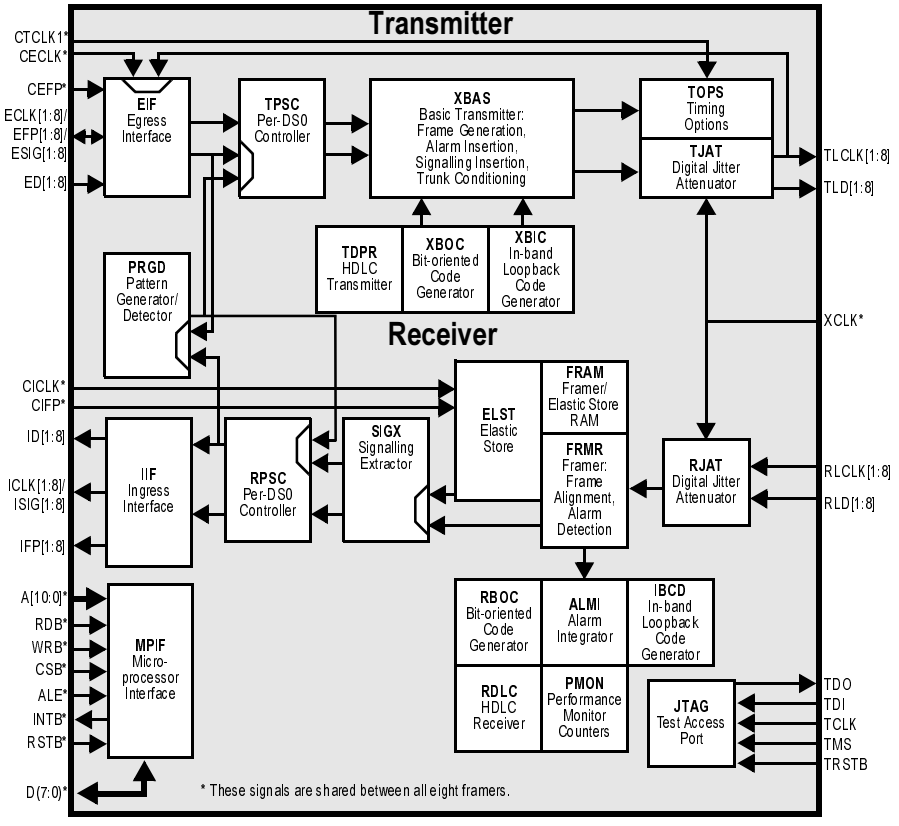
TRANSMIT SECTION

- Provides per-channel minimum ones density through Bell (bit 7), GTE, DDS, or “jammed bit 8" (56 Kbit/s) zero code suppression.
- Allows insertion of framed or unframed in-band line loopback and per-channel loopback code sequences.
- Allows insertion of a datalink in ESF mode via the microprocessor port. Provides 128 bytes of datalink message storage per datalink.
- Supports transmission of the AIS or the yellow alarm signal in both SF and ESF formats.
- Provides a digital PLL for generation of a low jitter transmit clock.
- Provides a FIFO buffer for jitter attenuation and transmit rate conversion. FIFO full or empty indication allows for bit-stuffing in higher rate multiplexing applications.

APPLICATIONS

- High-Density Internet T1 Interfaces for Multiplexers, Switches, Routers, and Digital Modems
- Frame Relay Switches and Access Devices (FRADS)
- T1 Performance Monitoring
- SONET/SDH Add/Drop Multiplexers (ADMs)

BLOCK DIAGRAM



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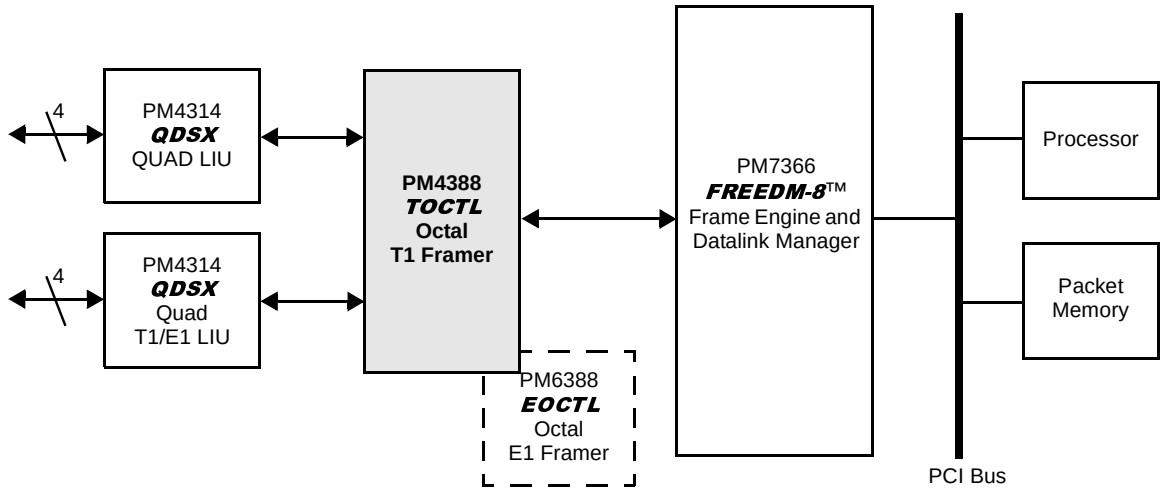
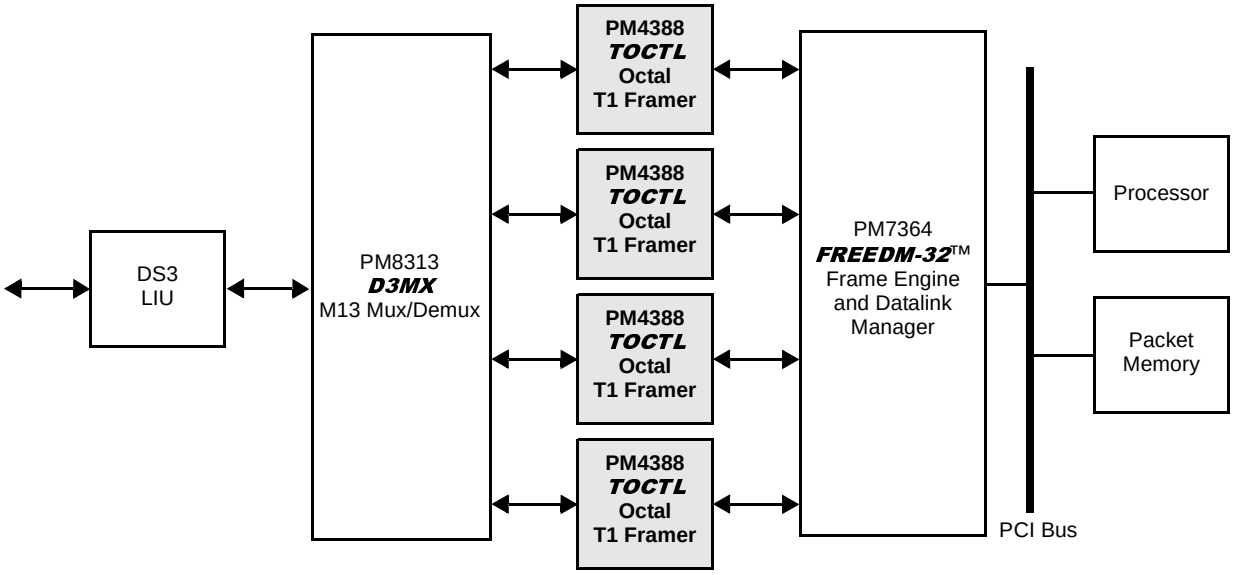
TYPICAL APPLICATIONS

EIGHT-CHANNEL T1/E1 PORT CARD ADAPTER USING PIN-COMPATIBLE TOCTL AND EOCTL



CHANNELIZED DS3 INTERFACE



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