622 MBPS ATM Traffic Management Device

FEATURES

QUEUING ALGORITHMS

Receive

- Maintains 64 weighted, bandwidth-controlled Service Classes (SCs) with per-VC queues.
- Provides round-robin servicing of queues within each SC
- Provides per-channel (VP or VC), per-SC, and per-direction congested and maximum queue depth limits
- Provides up to 64K cell buffers

Transmit

- Provides 31 VOs
- Maintains 16 SCs for each virtual output (VO) with per-VC accounting
- Provides per-channel (VP or VC), per-SC Queue (SCQ), per-SC, per-VO, and per-direction congested and maximum queue depth limits
- Provides up to 64K cell buffers

CONGESTION MANAGEMENT ALGORITHMS

- Supports EPD and Partial Packet Discard (PPD) for UBR traffic, and as a backup for ABR traffic
- Supports CLP-based cell discard and Explicit Forward Congestion Indicator (EFCI) cell marking
- Supports three congestion limits (as well as EPD, CLP, and EFCI, and/or backpressure) for logical multicast on the transmit side

SWITCHING

- Supports VC and VP switching.
- Supports up to 16K VCs

ADDRESS MAPPING

- Supports all 12 VP and 16 VC bits through use of a double, indirect lookup table
- Performs header translation at both the input (receive) and output (transmit) directions. Input header translation is used to pass the output queue channel number through the switch

MULTICAST

Supports logical multicast with a superior queue-clearing algorithm

DIAGNOSTIC/ROBUSTNESS FEATURES

- Checks the header parity
- Counts tagged cells
- Runs error checks continually on all fabric lines
- Checks liveness of control signal lines at both switch fabric and UTOPIA interfaces, working around partial fabric failures
- Checks Static Random Access Memory (SRAM) and Dynamic Random Access Memory (DRAM) parity

STATISTICS FEATURES

- In the receive direction, counts cells transmitted and dropped.
- In the transmit direction, counts cells transmitted and dropped on a per-VC basis

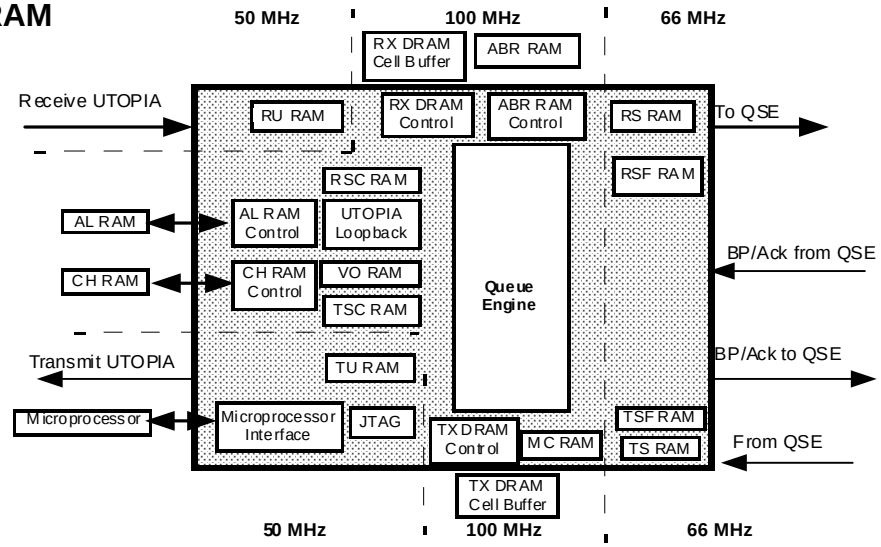
I/O FEATURES

- Provides four switch element interfaces with phase aligners. The phase aligners allow for external serialization of the data stream enabling systems to be built that support device separation of up to 10 meters.
- Provides a UTOPIA Level 2 Multi-PHY (MPHY) 16-bit, 50 MHz interface
- Provides a 2-level priority servicing algorithm for high and low bandwidth UTOPIA PHY layer devices
- Provides a multiplexed address/data CPU interface
- Provides two 100 MHz, 32-bit, synchronous DRAM cell buffer interfaces
- Provides three 100 MHz, synchronous SRAM control interfaces
- Provides a JTAG boundary scan interface

COMPATIBILITY FEATURES

- Compatible with the ATM Forum 3.0, 3.1, and 4.0 specifications
- Compatible with the ATM Forum UTOPIA Level 1 and Level 2

BLOCK DIAGRAM



622 MBPS ATM Traffic Management Device

specifications
- Compatible with the PM73488 QSE

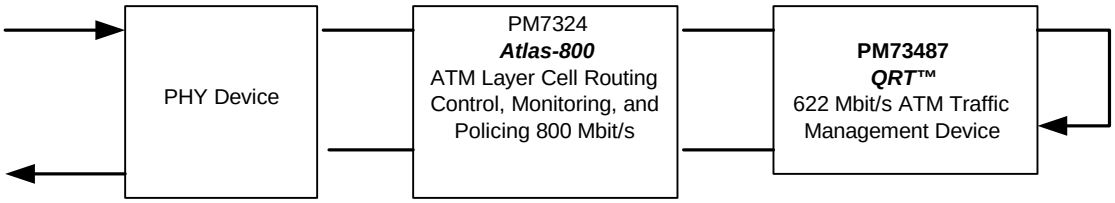
PHYSICAL CHARACTERISTICS

- 3.3 V supply voltage
- 5 V tolerant inputs on the microprocessor and UTOPIA interfaces
- Available in a 503-pin Enhanced Plastic Ball Grid Array (EPBGA) package

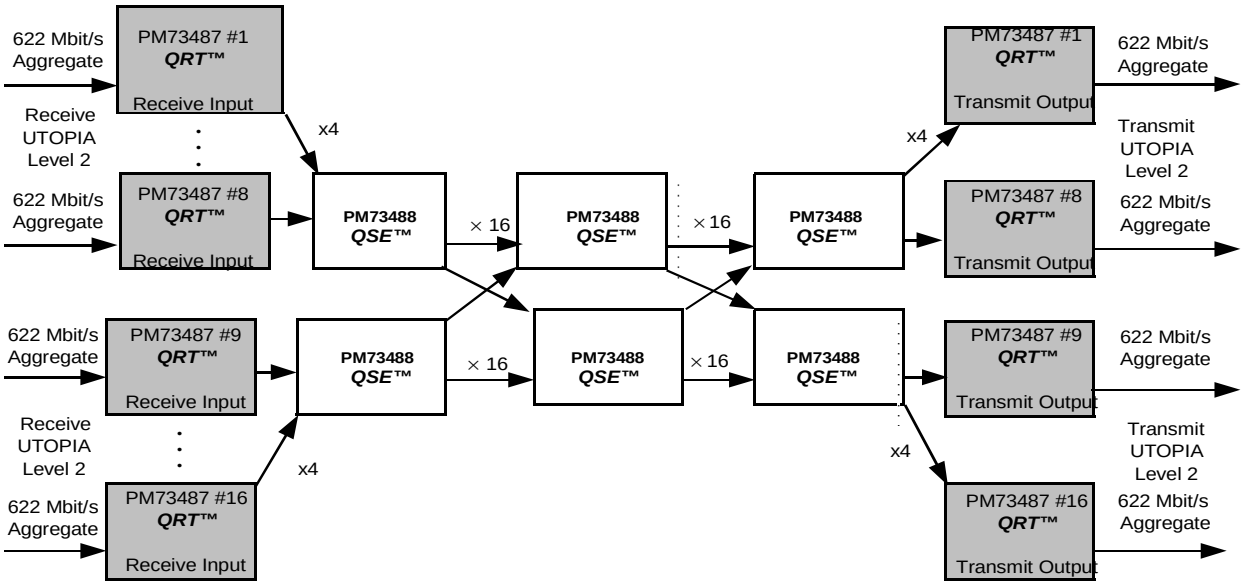
TYPICAL APPLICATIONS

- A Stand-Alone 622 Mbit/s Switch
- A 5 Gbit/s to 20 Gbit/s Scalable Switch Architecture
- A 2.4 Gbit/s to 80 Gbit/s Scalable Switch Architecture
- A 5 Gbit/s to 320 Gbit/s Scalable Switch Architecture

TYPICAL APPLICATION- QRT Used as a standalone 622 Mbps ATM switch



64X64 SWITCH APPLICATION (10GBPS)



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