SIEMENS

ICs for Communications

PMB 2240 V 1.6
GSM-Transmitter

Preliminary Data Sheet 05.97

Contents page

0 Revision History

Changes from Data sheet PMB2240 V1.5 (08.96) to Data sheet PMB2240 V1.6 (5.97)

#	Subject	Data sheet V1.5 (8.96)		Data sheet V1.6 (2.97)		Change
		Page	Item	Page	Item	
1	General Overview	4	1	4	1	Revised
2	Pinning	5	2.1	5	2.1	Pin 9 changed to VCCPR; Pin 13 changed to SLEEP; Pins 17,18,20,21 changed to GND pins
3	Functional block diagram	7	3	7	3	Prescaler with separate VCCPR-pin; Former SLEEP/PR and SLEEP/RF are merged to SLEEP; Oscillator/Buffer for RFIN removed;
4	Circuit description	8,9,10	4	8,9,10	4	Revised
5	Internal I/O Circuits	11	5	11	5	Revised
6	Asolute Maxi-mum ratings	12	6.1	12	6.1	ESD integrity revised; Item symbols revised
7	Operational range	13	6.2	13	6.2	Temperature range -30°C - 85°C
8	Prescaler	15	23	15	23	minimum H-voltage increased to 2.3V
9	Electrical Characteristics	12-18	6	12-17	6	Spec item symbols revised
10	AC/DC characteristics	14	6.3 #4	14	6.3 #4	Now referred to Test circuit 1
11	S-Parameters	27-30	9	27-31	9	Smith diagrams of simulated S-Params replaced by measured S-Param-table and I/O impedances

1 General Overview

1.1 Features

- Transmitter with I/Q modulator
- Direct I/Q modulation
- Generation of orthogonal carriers with possibility of phase adjust with external resistors at OFF1/OFF2
- 32dB minimum carrier rejection, 35dB minimum SSB rejection with 1 Vpp I/Q drive level
- 50dB rejection of third order products with 1 Vpp I/Q drive level
- -3dBm output power at 1 Vpp I/Q drive level with 200 Ohms load according testcircuit 1
- RF oscillator signal is AC-coupled to internal buffer stage (symmetrical or unsymmetrical)
- The RF oscillator-signal is buffered for off-chip use, especially for receiver chip PMB2405.
- Prescaler for the RF oscillator signal
- Possibility to build RF-PLL with integrated prescaler + PMB2306
- Possibility to use the IF oscillator signal from the IF-VCO on PMB2405
- Possibility to use external source for IF oscillator-signal
- Digital parts of fixed IF frequency PLL (fixed-PLL) for IF-VCO on PMB2405
- Supply voltage range from 2.7 V to 4.5 V
- P-TQFP-48 package
- Temperature range -30° to 85°C

1.2 Applications

- Vector modulated digital mobile cellular systems as GSM, DAMPS, PDC,WLAN etc.
- Various modulation schemes, such as PM, PSK, FSK, QAM, QPSK, GMSK etc.
- Analog systems with FM and AM modulation
- Space and power saving optimizations of existing discrete transmitter circuits

1.3 Functional Description

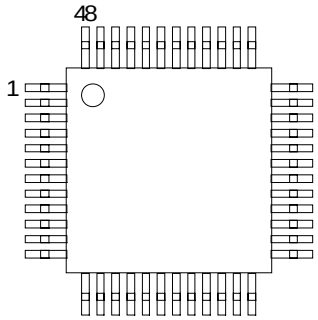
The PMB2240 is a single-chip transmitter which includes a prescaler for the main oscillator signal and a fixed frequency PLL for the IF oscillator. The transmitter is designed for use in conjunction with the single-chip receiver PMB2405 and the CMOS PLL PMB2306.
The RF oscillator signal can be supplied from an external source symmetrically as well as unsymmetrically. The oscillator signal can be buffered for off-chip use, depending on a separate power down pin.
There is a prescaler by 64/65 for the RF oscillator signal on chip, which can be used to implement a PLL together with the PMB2306.
The on-chip fixed-PLL consists of the system clock divider, the IF oscillator signal divider, the phase detector and the charge pump. The IF oscillator signal divider is driven by the oscillator on the PMB2405 or by an external discrete VCO.
The two oscillator signals are combined in the transmit mixer, and the image sideband and other mixing products are suppressed with an external interstage filter. The filtered signal reenters the chip at the modulator inputs LO/LOX. The modulator generates two orthogonal carriers which are mixed with the modulation signals I and Q in two Gilbert multipliers. The phase between the two carriers can be fine-adjusted to 90 ° (orthogonality) by two external resistors at OFF1/OFF2 for best SSB suppression. The outputs of the Gilbert cells are added and amplified by a linear output stage.
The PMB2240 is designed for digital mobile telephones according to the GSM-Standard. The chip can also be used for other digital systems and the dual mode system.
As part of the Siemens GSM/DCS chipset the derivatives PMB2245 and PMB2247 are offered for the DCS 1800 and DCS 1900 frequency range.

2 Pinning

2.1 Pin Description

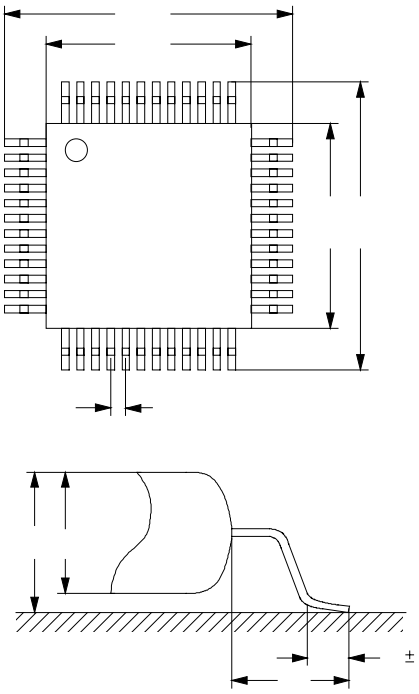
Pin No.	Symbol	Function
1, 44, 46	GND2	Ground for the PLL-parts and their bias
2	PUPLO2/FP	Power down for fixed-PLL-dividers and phase detector
3	IF	Input for external IF oscillator signal
4	IFX	Input for inverted external IF oscillator signal
5	VCC2	Supply voltage for PLL parts (IF and RF) and their biasing
6	PUPLO2/BU	Power down for IF/IFX input buffer
7	RF	RF oscillator signal to receiver
8	RFX	Inverted RF oscillator signal to receiver
9	VCCPR	Separate supply voltage for RF-PLL prescaler
10	TOUT	Output of RF-PLL prescaler
11	IREF/PLL	Output for reference current for external RF-PLL-chip
12	FMOD	Modulus control for prescaler
13	SLEEP	Power down of RF oscillator input- and output buffer and the prescaler
14,17,18,20	GND3	Ground for RF oscillator + BufRX
15	VCC3	Supply voltage for BufRX and BufRF
16	RFB1	RF oscillator input buffer (inverting input)
19	RFB2	RF oscillator input buffer (non-inverting input)
21,24	GND4	Ground for internal shielding
22	LO	Modulator LO frequency input
23	LOX	Inverted Modulator LO frequency input
25,33	GND1	Ground for modulator and mixer parts + Bias1
26	MO	Mixer output, open collector
27	MOX	Inverted mixer output, open collector
28	GND5	Ground for substrate contacts in the modulator
29	QX	Quadratur modulating inverting input, open base
30	Q	Quadratur modulating input, open base
31	I	In phase modulating input, open base
32	IX	In phase inverted modulating input, open base
34	E	Non-inverting output of modulator, open collector; ESD disconnected
35	EX	Inverting output of modulator, open collector; ESD disconnected
36	VCC1	Supply voltage for modulator and mixer parts + Bias1
37	TREF	Temperature compensated DC reference voltage output for modulator I/Q -inputs via GMSK baseband circuit
38	TXON1	Power down for modulator and mixer parts + Bias1
39	OFF1	Phase error adjustment of orthogonal carriers with constant R
40	OFF2	Phase error adjustment of orthogonal carriers with constant R
41	T3	Test pin 3
42	PDBUFRX	Power down for "BufRX"
43	n.c.	not bonded
45	CHP	Phase-detector output for external loop filter (charge pump)
47	RREF/PLL	To be connected to GND via resistor to determine IREF for RF-PLL
48	FREF	Input of system reference clock

2.2 Pin Configuration (top view)

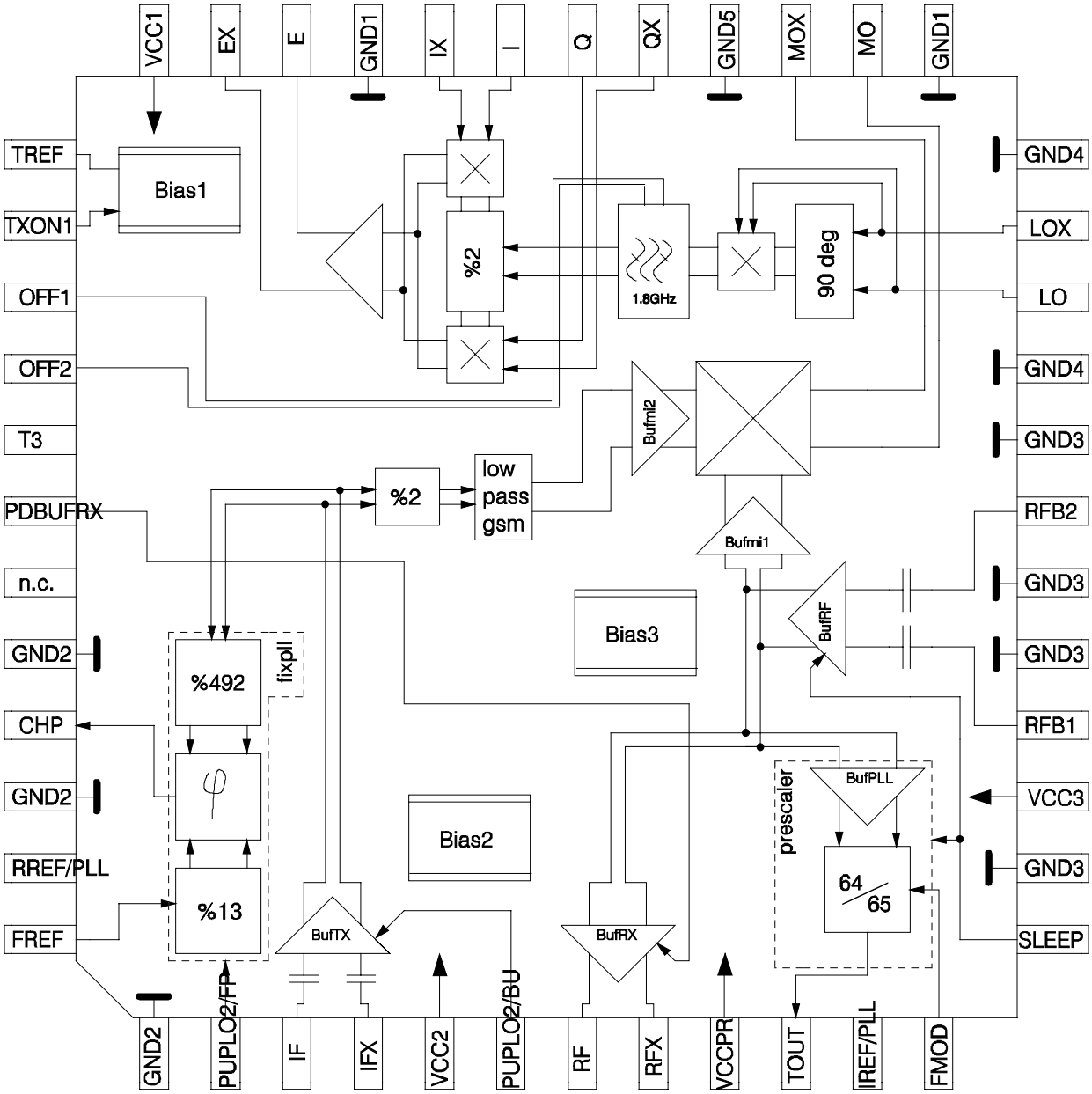


2.3 Package Outline

Quad Flat package
P-TQFP-48



3 Functional Block Diagram



4 Circuit Description

4.1 Block Level description

The GSM transmitter PMB2240 contains a number of functions that have been realised with multiple chips earlier:

- Oscillator signal input balanced or unbalanced
- RF-PLL prescaler
- IF-PLL dividers and phase detection
- TX - mixer
- I/Q modulator

The PMB2240 V1.6 is designed to be used with an external RF oscillator module. On chip this signal is AC-coupled to an internal buffer stage. Therefore the RF input is suitable for symmetrical or single ended use. There is no need for an external DC-bias of the RF input. The active parts of the IF oscillator are located on the receive chip PMB2405.

A buffer BufRX, which can be powered down by pin PDBUFRX, is used to transmit the RF oscillator signal to the receiver chip to drive the RF receive mixer. A special input buffer BufTX receives the IF oscillator signal from the receive chip or an external source.

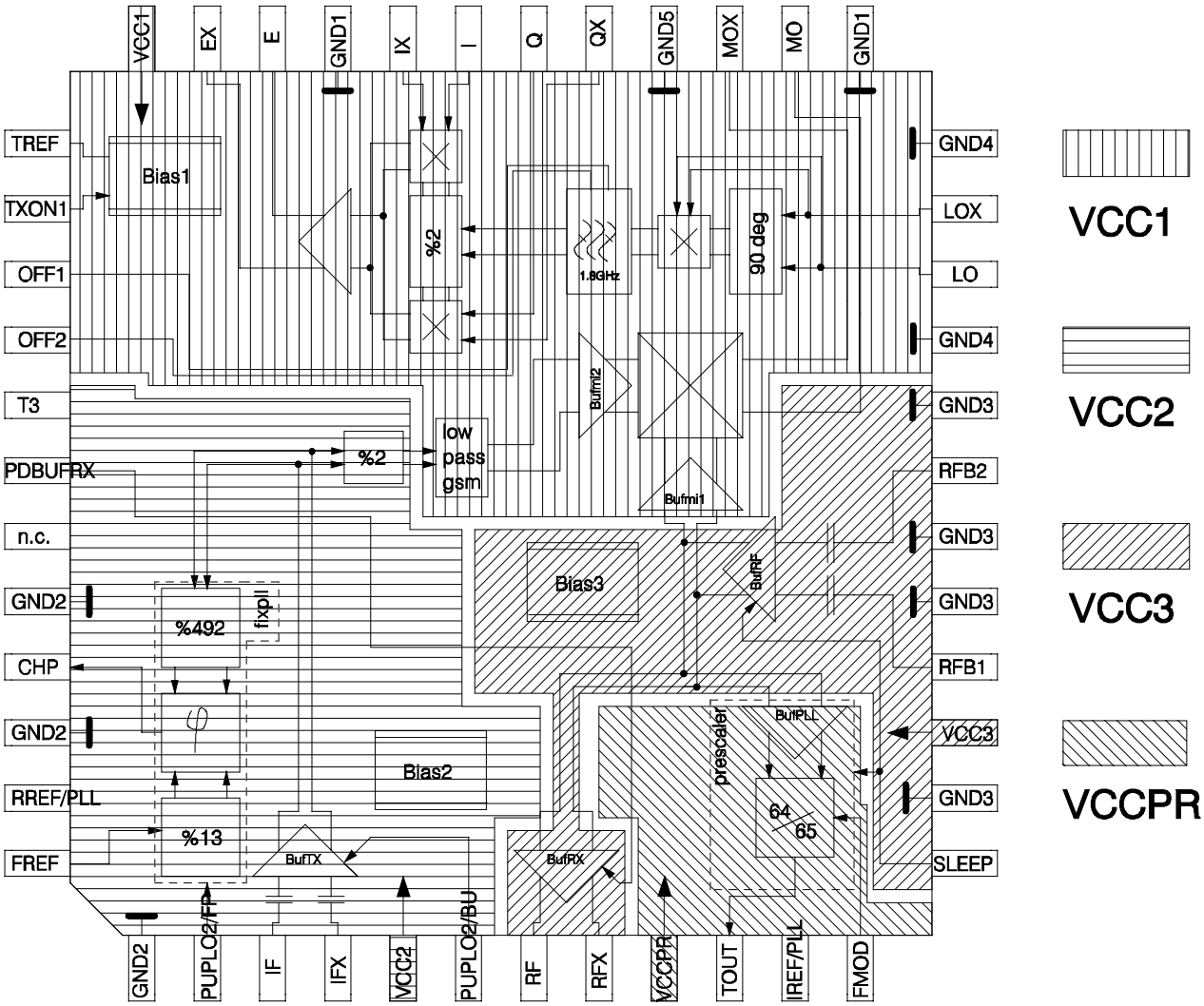
The RF oscillator signal is divided by the integrated 64/65 prescaler which can be connected to the CMOS PLL circuit PMB2306 for the RF oscillator PLL. The supply pin VCCPR is a separate prescaler supply, which openes the possilility to run the prescaler and the rest of the RF synthesizer on a supply voltage that is different from the supplies of the rest of the chip.

For the IF-PLL the active oscillator structures on the PMB2405 or an external VCO module can be used. The PMB2240 V1.6 contains the digital parts tor the IF oscillator PLL (fixed-PLL): the IF-frequency and system clock dividers and a phase detector plus charge pump are integrated to lock the IF oscillator to the external system clock. The oscillator signal drives the divider by 2 in front of the transmit mixer. The phase locked IF- and RF- signals are converted into the transmit band (e.g. 880 - 915 MHz for GSM) by the TX- mixer. The mixer output signal leaves the chip at MO/MOX and passes an external interstage filter to provide suppression of unwanted products. This signal reenters the chip at the modulator input LO/LOX.

The LO signal is divided into two orthogonal carriers at the transmit frequency. The phase between the two carriers can be fine-adjusted to 90 ° (orthogonality) by two external resistors at OFF1/OFF2 for maximum SSB suppression. The modulator consists of two Gilbert multipliers, where the modulating signals I(t) and Q(t) are multiplied with the RF-carriers. The outputs of both Gilbert cells are added and amplified by a linear output stage. The modulated transmit signal is available at E/EX and is fed into a transmitter power amplifier.

4.2 Supply concept

There are four independent supply voltages (VCC1-3,VCCPR) and ground rails (GND1-4) to decouple the modulator/mixer parts, the synthesizer parts, and the RFVCO parts.
The supply pin VCCPR is a separate prescaler supply, which openes the possilility to run the prescaler together with the rest of the RF synthesizer on a supply voltage that is different from the supplies of the rest of the chip
GND4 is a special shielding ground to decrease crosstalk between the separately supplied blocks.
GND5 collects the substrate contacts in the modulator and mixer.
It is recommended to connect all GND pins to a common GND on the board.
In the following figure the chip schematic is partitioned according to its supply rails.

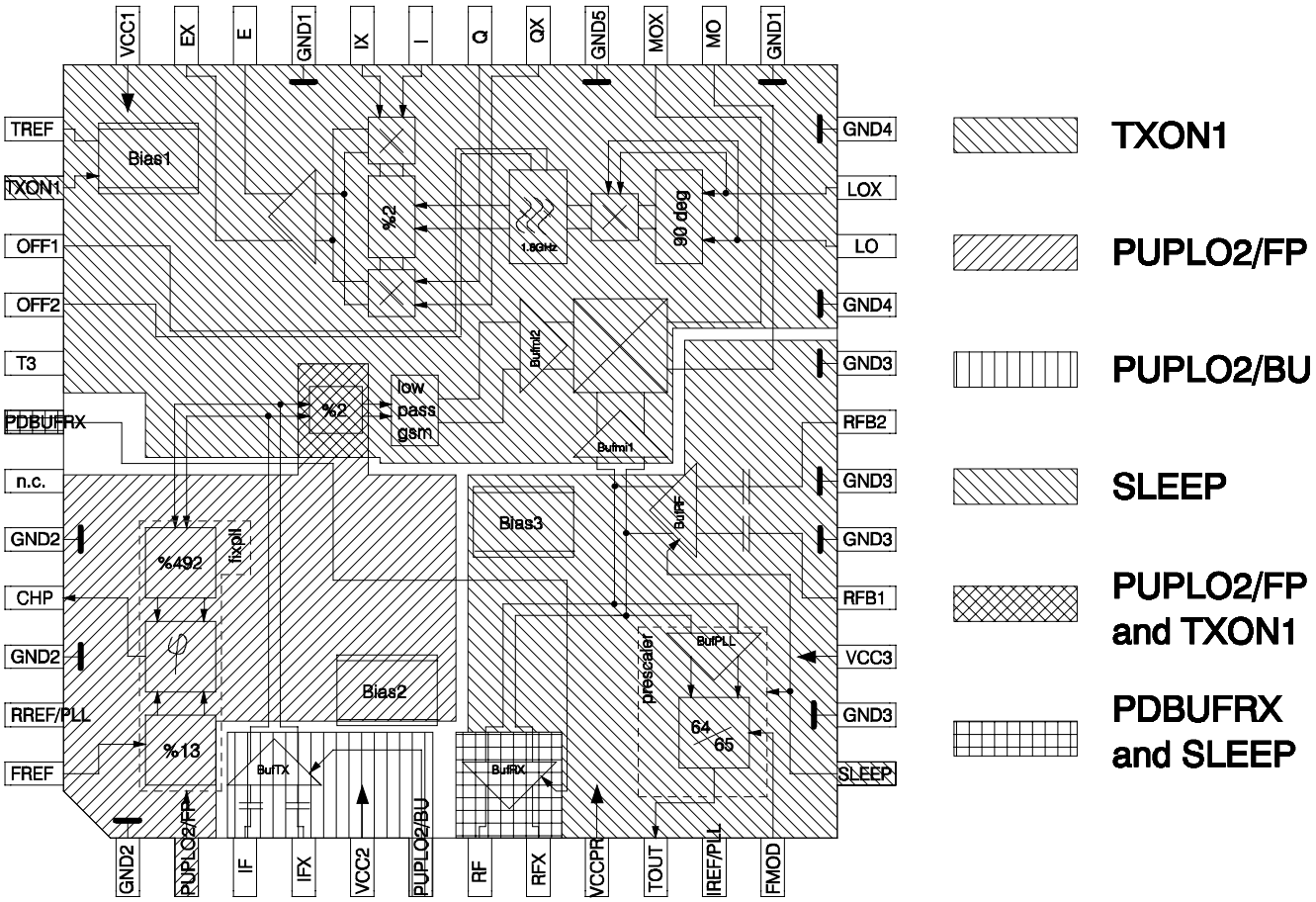


4.3 Power down conditions

The PMB 2240 has five Power down inputs.
PD = Low means that the respective part of the chip is in power down mode.

TXON1:	Modulator, mixer, Bufmi1, Bufmi2
TXON1 /\ PUPLO2/FP	%2 divider
SLEEP:	BufRF, prescaler with its input buffer BufPLL
PUPLO2/BU:	Input buffer BufTX for external IF oscillator-signal
PUPLO2/FP:	fixed-PLL, (%492; %13; phase detector, charge pump)
PDBUFRX /\ SLEEP	BufRX

For normal operation only three modes are used: sleep mode, TX-mode, RX-mode. Depending on the application some power down-pins can be combined, and others can be fixed to supply rails.

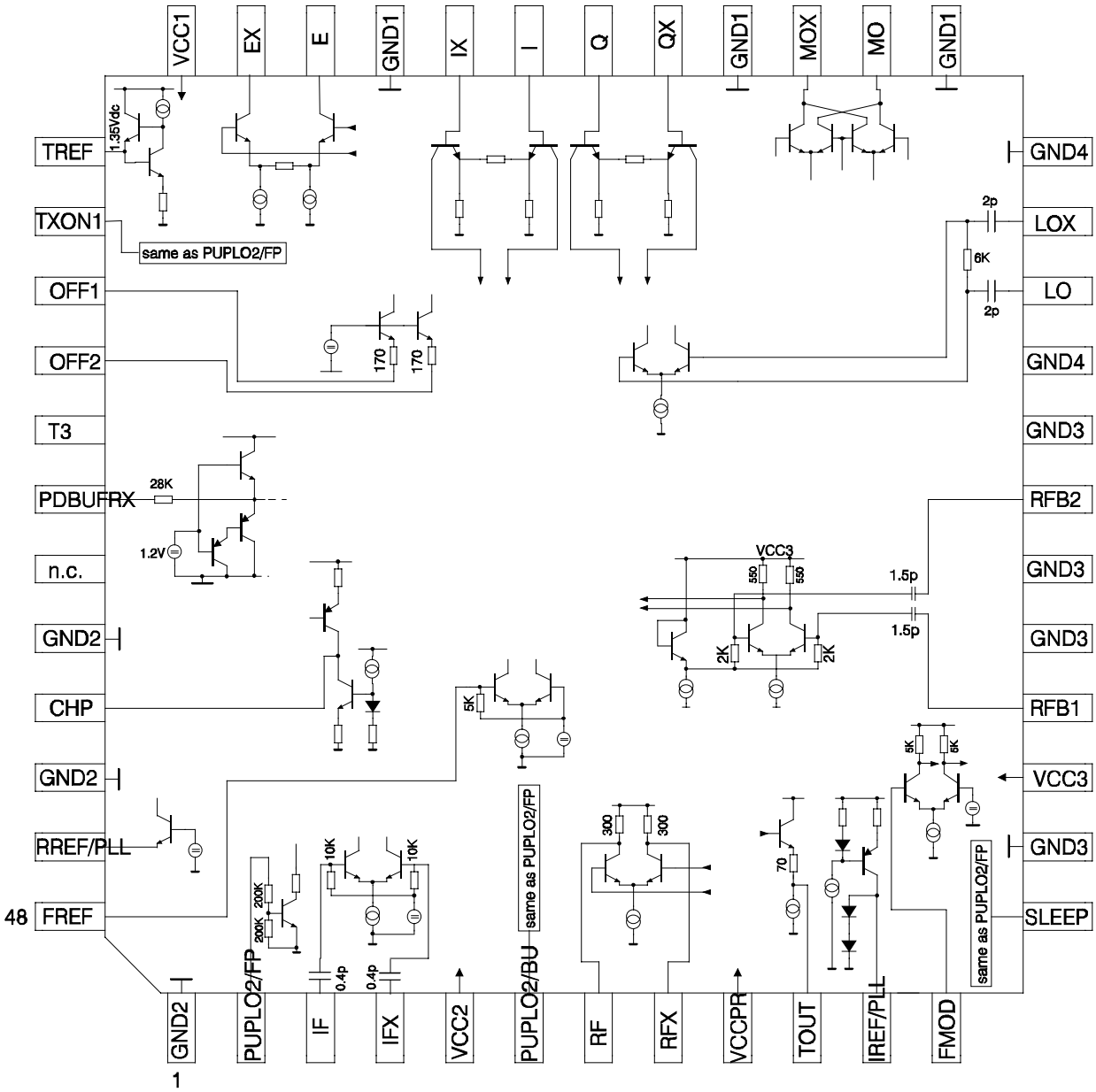


4.4 Matching with Timing Signals of GOLD-uC

In application with PMB2405 and GOLD-uC the power down pins of PMB2240 must be connected to the timing signals of GOLD-uC as follows:

PMB 2240		GOLD-uC
TXON1	connected to	TXON1
PUPLO2/BU, PUPLO2/FP	connected to	PUPLO2
SLEEP, PDBUFRX	connected to	general purpose port pin

5 Internal Input/Output Circuits



6 Electrical Characteristics

6.1 Absolute Maximum Ratings

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC will result.

#	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
1	Supply Voltage	V_{CC}	-0.3	5.0	V	
2	Input/Output Voltage	V_{IO}	-0.3	5.0	V	
3	Open Collector Output Voltage at E/EX	V_{OCE}	V_{CC} - 1.5	V_{CC} + 1.0	V	
4	Open Collector Output Voltage at MO/MOX	V_{OCM}	-0.3	5.0	V	
5	Differential Input Voltage (any differential Input)	V_{ID}		2	V	
6	Junction Temperature	T_J	-40	125	°C	
7	Storage Temperature	T_S	-55	125	°C	
8	Thermal Resistance (junction to ambient)	R_{thJA}		165	K/W	
9	ESD integrity *	V_{ESD}	-1000	+1000	V	according MIL-Std. 883D, method 3015.7

* exception: Pin 47 to GND and a negative Pulse to pin 11
=> 800V ESD-integrity

6.2 Operational Range

Within the operational range the IC operates as described in the circuit description. The AC/DC characteristics limits are not guaranteed.

V_{CC} = 2.7V to 4.5V; TA = -30 to 85°C;

#	Parameter	Symbol	Limit Values		Unit	Remarks
			min.	max.		
1	RFB1/RFB2 Input Level	P_{RFIN}	-10	0	dBm	
2	RFB1/RFB2 Input Frequency	f_{RFIN}	900	1300	MHz	
3	IF/IFX Input Level	P_{IFIN}	-15	0	dBm	
4	IF/IFX Input Frequency	f_{IFIN}	400	600	MHz	
5	LO/LOX Input Level	P_{LO}	-15	0	dBm	
6	LO/LOX Input Frequency	f_{LO}	800	1000	MHz	
7	Mixer output Frequency Range	f_{MO}	800	1000	MHz	wanted sideband
8	PD-Signals Voltage-L	V_{PDL}	0	0.8	V	
9	PD-Signals Voltage-H	V_{PDH}	2.0	V_{CC}	V	

Note:
Power levels are referred to impedance of 50 Ohms

6.3 AC/DC Characteristics

AC/DC characteristics involve the spread of values guaranteed within the specified supply voltage and ambient temperature range. Typical characteristics are the median of the production.

V_{CC} = 2.7V/4.5V; TA = 25°C;

#	Parameter	Sym-bol	Limit Values			Unit	Test Condition	Test-circuit
			min.	typ.	max.			
1	Supply Current all powered up	I_{vcc1} I_e+I_{ex} $I_{mo}+$ I_{mox} I_{vcc2} I_{vcc3} I_{vccpr}	16 9 7 5 9.3 2.5	22 13 10 6.3 11 3.3	29 18 13 7.5 13.2 4	mA mA mA mA mA mA	TXON1 & PUPLO2/FP & PUPLO2/BU & SLEEP & PDBUFRX = HIGH	1
2	Supply Current all powered down	I_{vcc1} I_e,I_{ex} I_{mo}, I_{mox} I_{vcc2} I_{vcc3} I_{vccpr}			2 2 2 2 2 2	uA uA uA uA uA uA	TXON1 & PUPLO2/FP & PUPLO2/BU & SLEEP & PDBUFRX = LOW	1
Transmit Mixer Output MO/MOX								
3	Output impedance (open collector diff. output)	see S-parameter 9.1						
4	Output level	P_{MO}	-18	-15	-12	dBm	900 MHz	1
5	Carrier suppression	a_{Cmix}	25	30		dB		1
6	Output Frequency	f_{MO}	800		1000	MHz	wanted sideband	1
IF input at IF/IFX								
7	Input Level	P_{IFIN}	-15 110		0 600	dBm mVpp *		1
8	Input Frequency	f_{IFIN}	400		600	MHz		1

* referred to 50 Ohm

#	Parameter	Symbl	Limit Values			Unit	Test Condition	Test Circuit
			min.	typ.	max.			
Fixed PLL								
9	lock in time	t_l		250		usec	Application hint	
10	Power on delay	t_{po}		0.3		usec	Application hint	
11	Input level at FREF	V_{FREFI}	0.4	1	2	Vpp	high input levels may cause spurious problems	1
12	Output current at CHP	I_{CHP}	+-450	+-600	+-750	uA		1
Output to receiver RF/RFX								
13	Internal DC bias	V_{RFDC}		V_{CC} - 0.6		V		1
14	Output impedance	see S-parameter 9.4						
15	Output level	P_{RFOUT}	-11	-8	-5	dBm	f = 1200 MHz	1
RF input at RFB1/RFB2								
16	Input Level	P_{RFIN}	-10		0	dBm		1
17	Input Frequency	f_{RFIN}	900		1300	MHz		1
LO input at LO/LOX								
18	Input impedance	see S-parameter 9.6						
19	Input Level	P_{LO}	-15		0	dBm	into 50 Ohm	1
20	Input Frequency	f_{LO}	800		1000	MHz		1
21	suppression of image in mixer output signal	a_{IM}	14			dB	Application hint	
Prescaler								
22	Input at FMOD voltage-L	V_{FMOD}	0		0.8	V		1
23	Input at FMOD voltage-H	V_{FMOD}	2.3		V_{CC}	V		1
24	Output DC level at TOUT	V_{TOUTDC}	V_{CC}-1		V_{CC}-0.7	V		1
25	Output AC amplitude at TOUT	V_{TOUTAC}	160		300	mVpp	f = 13.5MHz to 20.5MHz	1

#	Parameter	Symbl	Limit Values			Unit	Test Condition	Test Circuit
			min.	typ.	max.			
Reference current for external PLL								
26	External voltage of current sink fed to IREF/PLL	$V_{IREF/PLL}$			1.2	V		1
27	Current sourced at IREF/PLL	$I_{IREF/PLL}$		100**	360	uA	dependent of resistor value at RREF/PLL ***	1
28	Temperature dependency of current sourced at IREF/PLL *	$I_{IREF/PLL}$		+-2		%	temperature range: -30 to 85 °C nominal current: 300uA	
Modulator inputs I/IX and Q/QX								
29	I-IX and Q-QX differential input level	V_{I-IX}, V_{Q-QX}		500	1000	mVpp		
30	Recommended range for ext DC voltage to compen-sate internal offset at I-IX and Q/QX *	V_{DCext}			15	mV		
31	Reference voltage for I,Q modulating inputs	V_{TREF}	1.25	1.35	1.45	V	Reference to external GMSK basebandcircuit to bias I and Q of PMB2240 (temperature compensated)	1
32	Resistive load at TREF *	R_{TREF}	3			kOhm		
33	Input base current	I_{I/Q_DC}	1	6	12	uA		
34	Differential input resistance *	R_{I-IX}	50			kOhm	at 200 kHz	
35	Differential input capacitance *	C_{I-IX}		1		pF		
36	Input frequency *	f_{I-IX} f_{Q-QX}			10	MHz		

* Design hint

** required by PMB2306 R19 = 6.8kΩ

*** R19 at pin RREF/PLL gives constant PLL reference current at pin IREF/PLL:

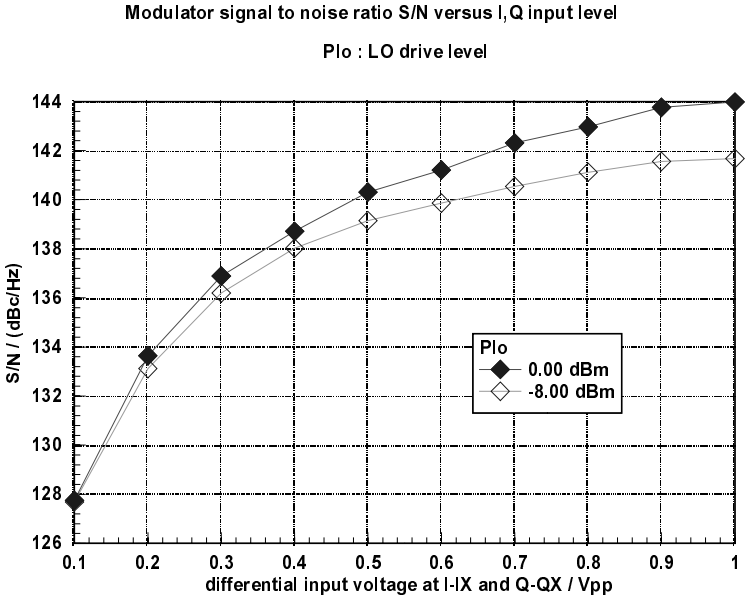
($R19_{max}$ = open -> $I_{IREF/PLL}min$ = 0,
$R19_{min}$ = 2 KOhm -> $I_{IREF/PLL}max$ =360uA)

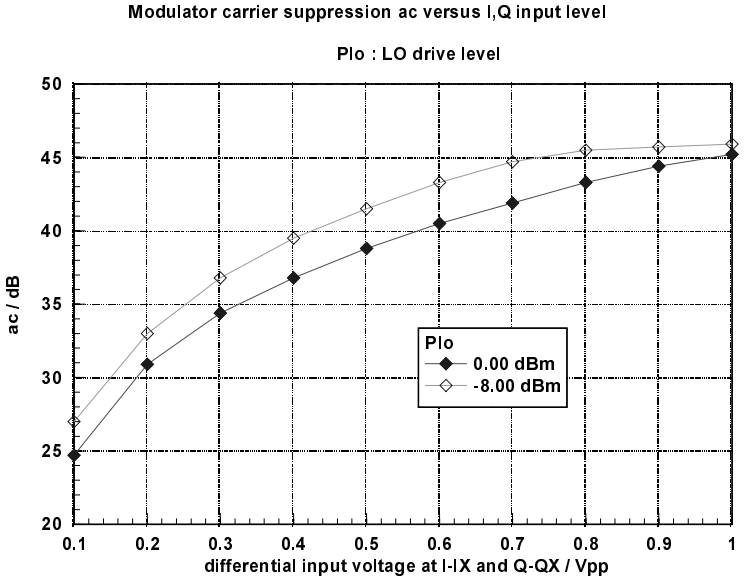
#	Parameter	Symbl	Limit Values			Unit	Test Condition	Test Circuit
			min.	typ.	max.			
Modulator output E/EX		f_{LO} = 900 MHz; $f_{I-IX} = f_{Q-QX}$ =10MHz;						
37	Output impedance (open collector diff. output)	see S-parameter 9.5						
38 ,	Output power	P_{E_b}	-12	-9	-6	dBm	cond1 **	1
			-6	-3	0	dBm	cond2 ***	1
39	Carrier suppression	a_{Cmod}	26	32		dB	cond1 **	1
			32	38		dB	cond2 ***	1
40	Single sideband suppression	a_{SSB}	35			dB	with 90° phase shift between I and Q; ROFF1,ROFF2 tuned to maximum SSB suppression (appl. hint: fig.1,sec. 8.3)	1
41	Suppression of third order distortion products	a_{IM3}		62		dB	cond1 **	1
				50		dB	cond2 ***	1
42	Signal to noise ratio *	S/N		-139		dBc/Hz	cond1 ** P_{LO} = -8 dBm f_{offset} = 20MHz	1
				-142		dBc/Hz	cond2 *** P_{LO} = -8 dBm f_{offset} = 20MHz	1

* Design hint
** cond1 means $V_{I-IX} = V_{Q-QX}$ = 500 mV_{pp}
*** cond2 means $V_{I-IX} = V_{Q-QX}$ = 1 V_{pp}

6.4 Typical modulator measurement results

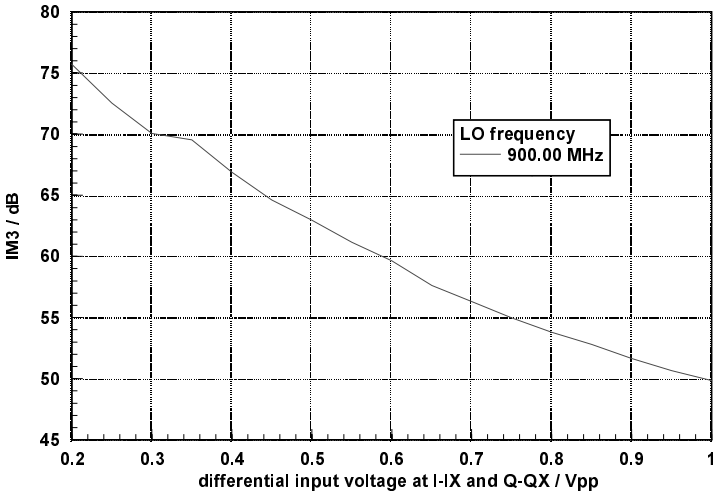
The following measurements refer to Testcircuit 1 (item **7.1**, page 21)





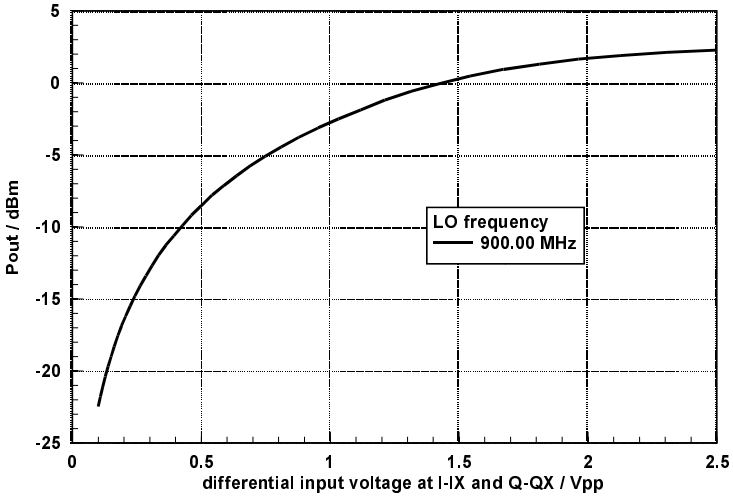
Modulator third order intermodulation product IM3 versus I,Q input level

LO drive level : Plo = -8 dBm



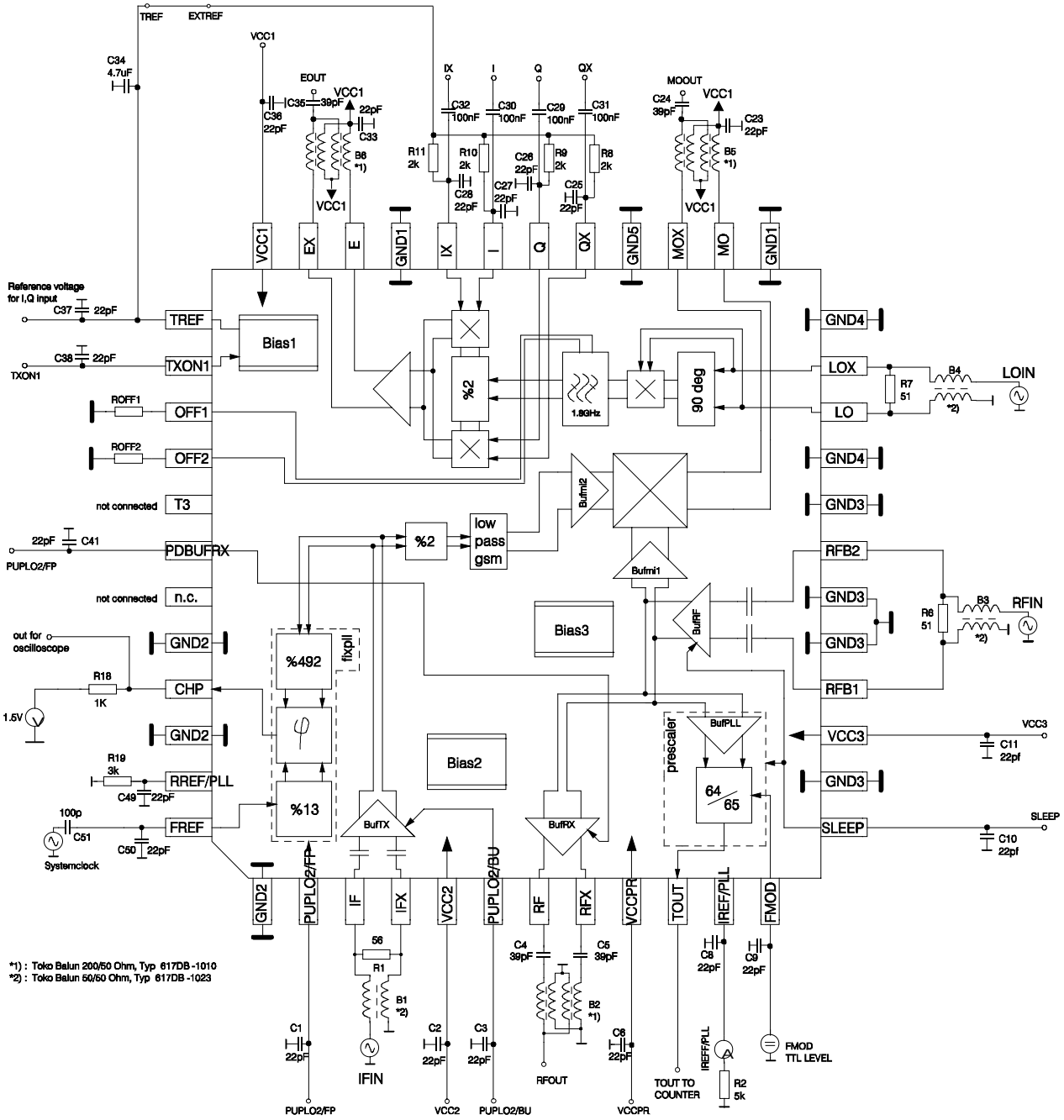
Modulator output power Pout versus I,Q input level

LO drive level: Plo = -8 dBm



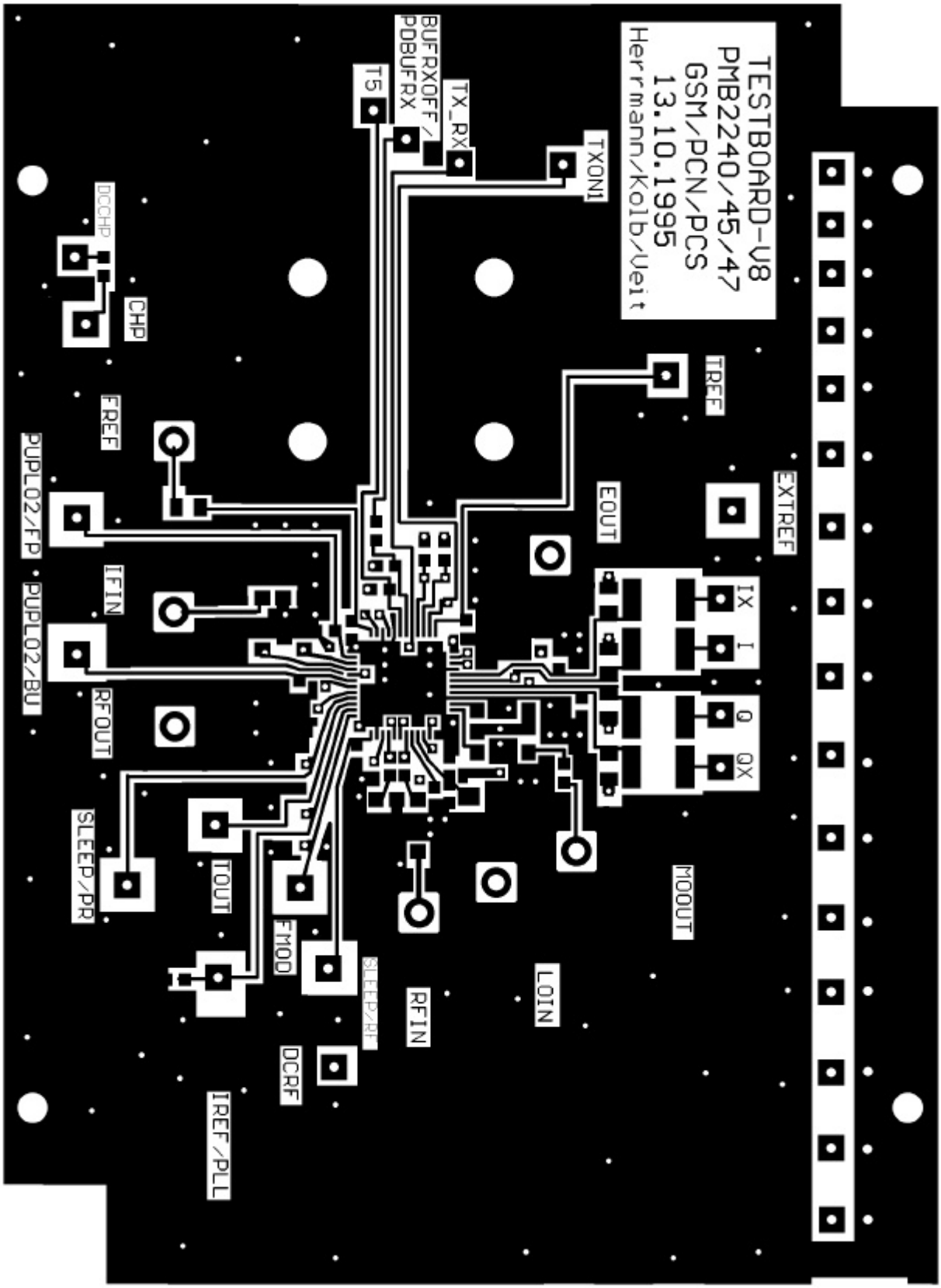
7 Test Circuits

7.1 Test Circuit 1

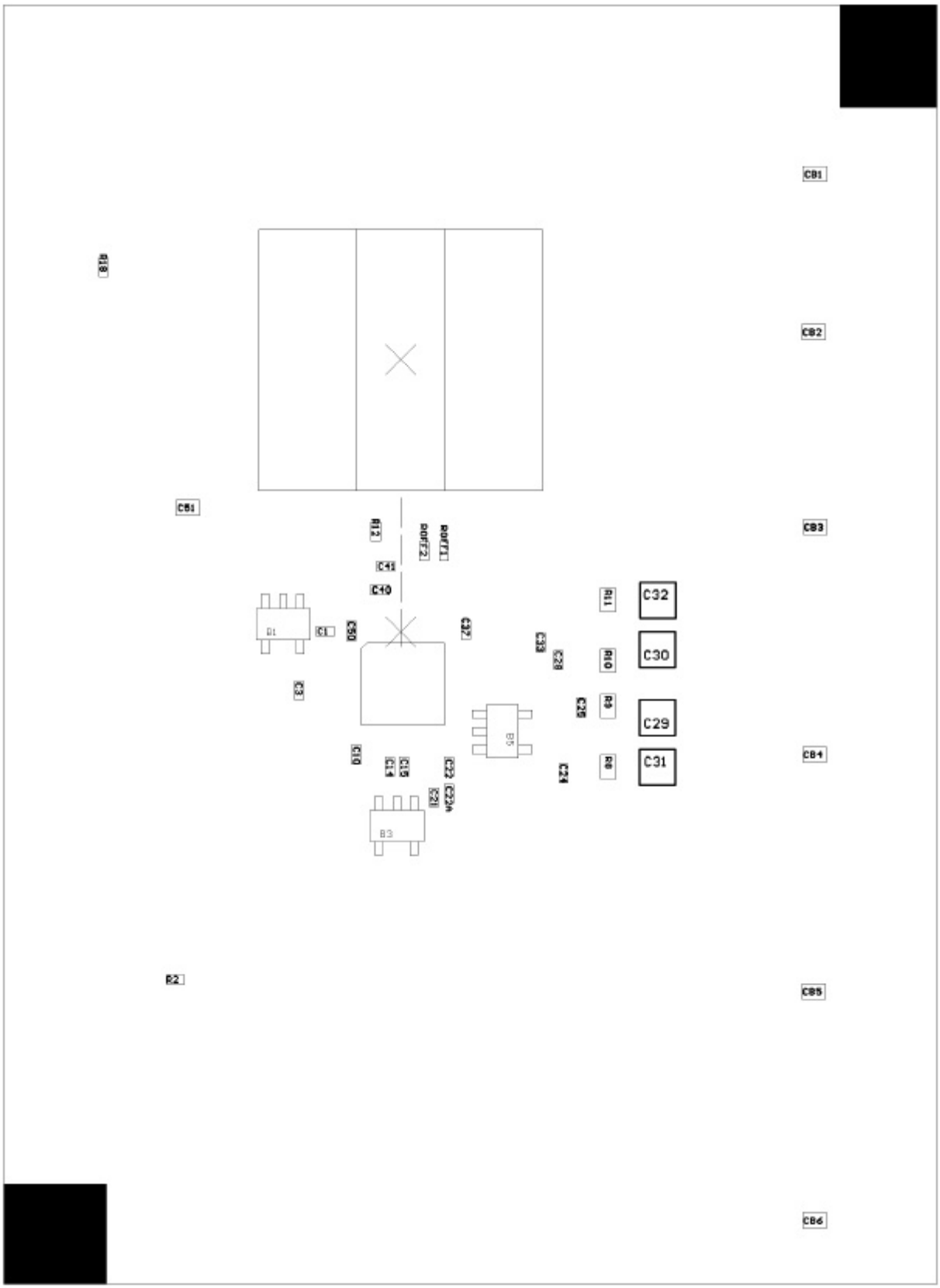


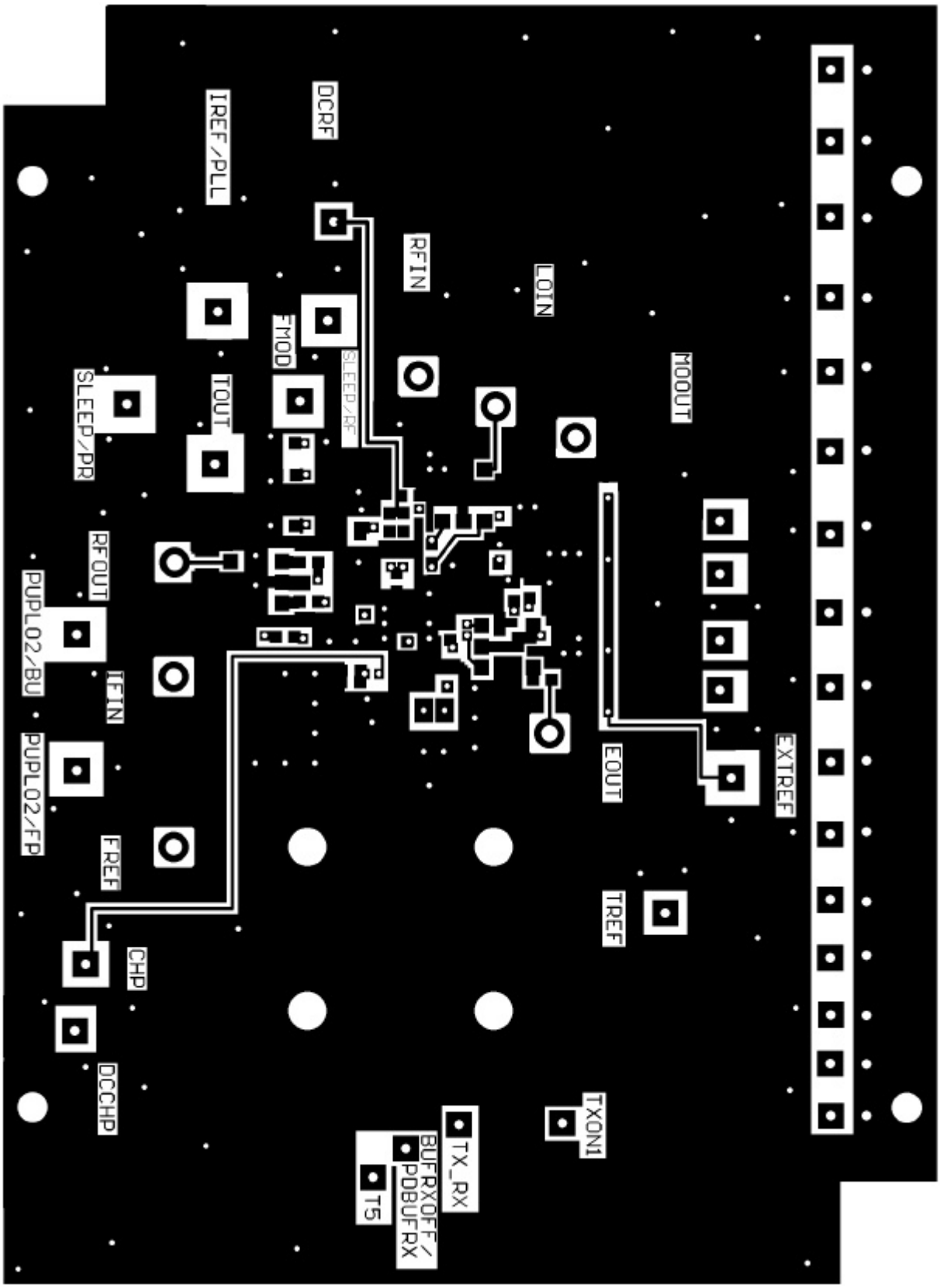
ROFF1/ROFF2 = 0 ... 600 Ohm; see application hint on page 26

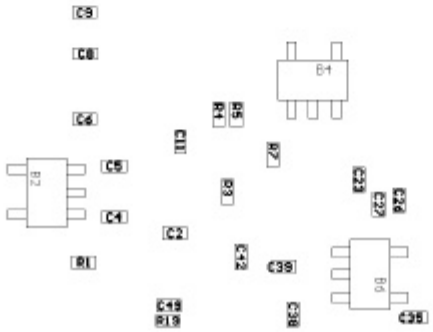
7.2 Test board Layout top, (M 2:1)



7.3 Test board Top place



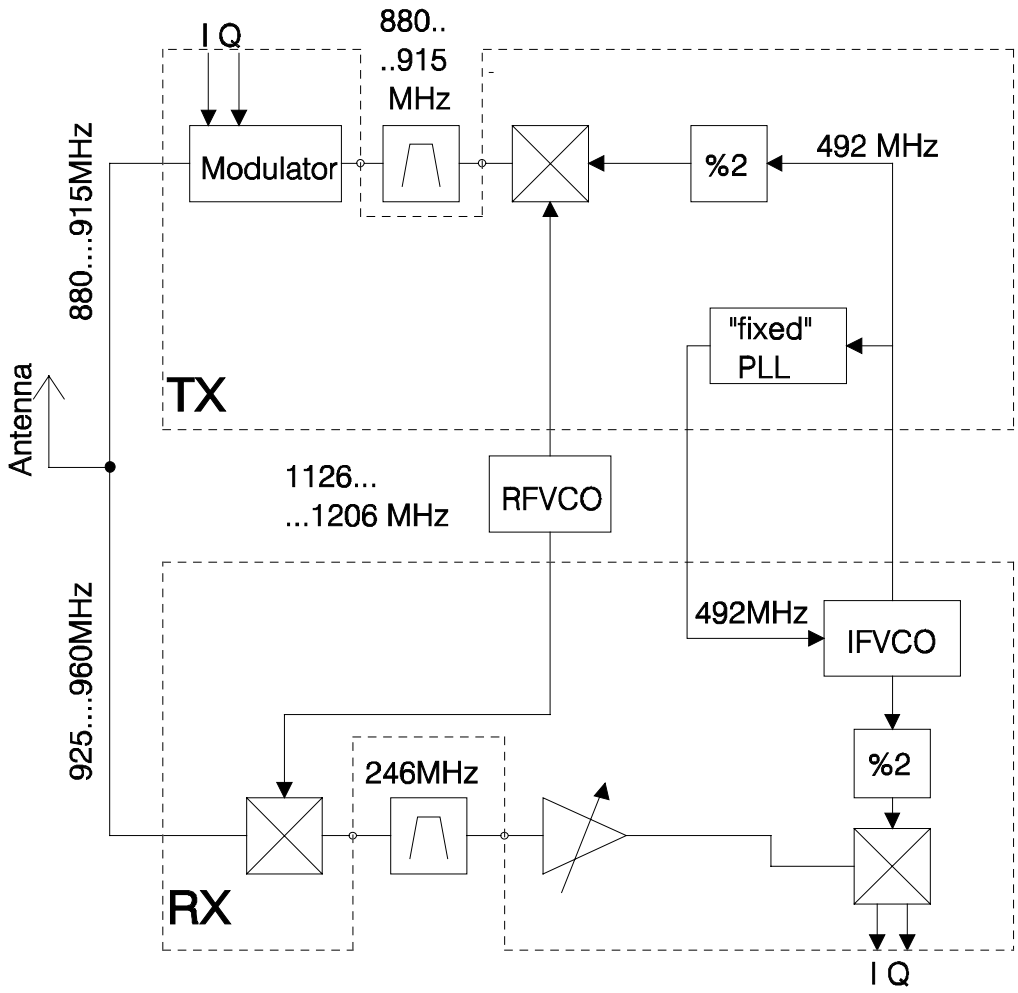




8 Application

8.1 Frequency plan for GSM application

In the application the IF oscillator on the receive chip is locked at a frequency of 492 MHz by the fixed-PLL circuit. The RF oscillator module is tuned from 1126 MHz to 1206 MHz.



8.2 Application hint for phase adjust

The LO level for maximum SSB suppression can be tuned to every value within its operational range (-15 dBm to 0 dBm) by appropriate choice of ROFF1/ROFF2.
At pins OFF1 and OFF2 always a resistor or a short cicuit to ground is required. The recommended range of values is:

0 > ROFF1,ROFF2 < 600 Ohm.

In fig. 1 the maximum single sideband suppression (a_{ssb}) is tuned to -7dBm LO input power accordinng test circuit 1. ROFF1=0 and ROFF2=200 Ohms.
The LO level can vary +/- 4dB around its optimum value with assb $\leq$ -35dB.

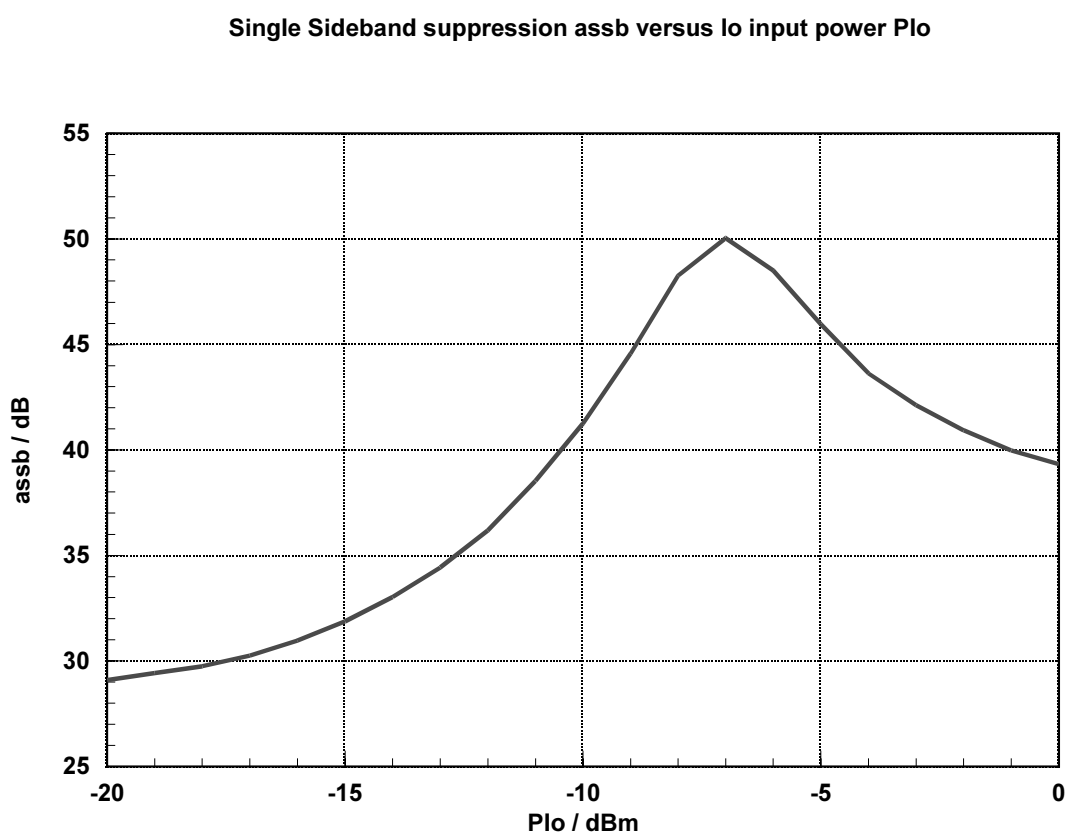
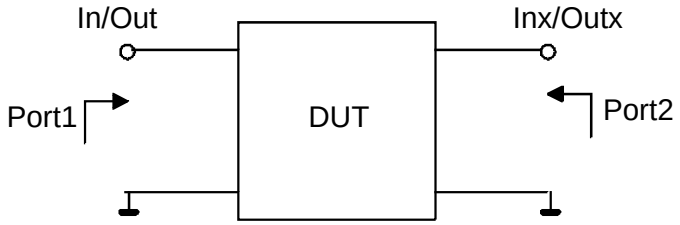


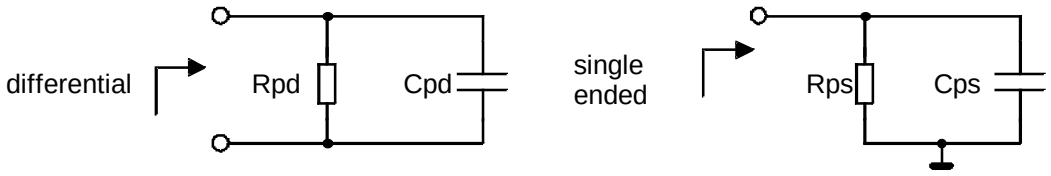
fig. 1: Phase adjust with ROFF1=short, ROFF2=200 Ohms

9 S-Parameters and Input/Output Impedances

The S-parameters provided in this section are based on measurements.
Measurement setup for differential in-/outputs:



The input/output impedances are calculated from these parameters.
The impedances are given as equivalent circuit with lumped elements for differential and single ended in-/outputs.
The high frequency in-/outputs in this section are base inputs or collector outputs.
As equivalent circuit for these in-/outputs a resistor Rp in parallel to a capacitance Cp is derived:



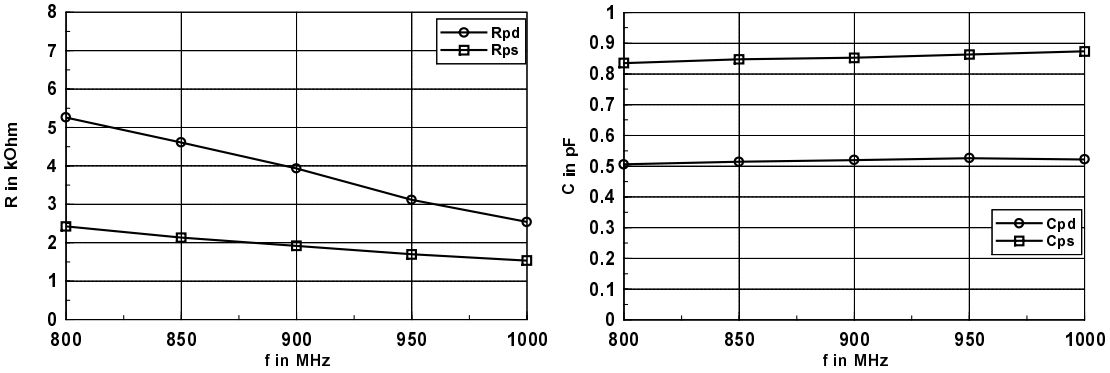
The S-parameters are available on disk.

9.1 Transmit Mixer Output MO/MOX

S-parameters:

f	S11		S21		S12		S22	
GHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
0.80	0.957	-23.7	0.093	70.4	0.092	71.7	0.952	-22.4
0.85	0.951	-25.5	0.098	69.3	0.097	70.7	0.944	-24.3
0.90	0.946	-27.1	0.103	68.2	0.102	69.4	0.932	-26.2
0.95	0.940	-28.9	0.107	67.2	0.106	68.4	0.913	-28.0
1.00	0.935	-30.7	0.111	66.8	0.109	68.0	0.892	-28.5

Output impedance at MO/MOX:

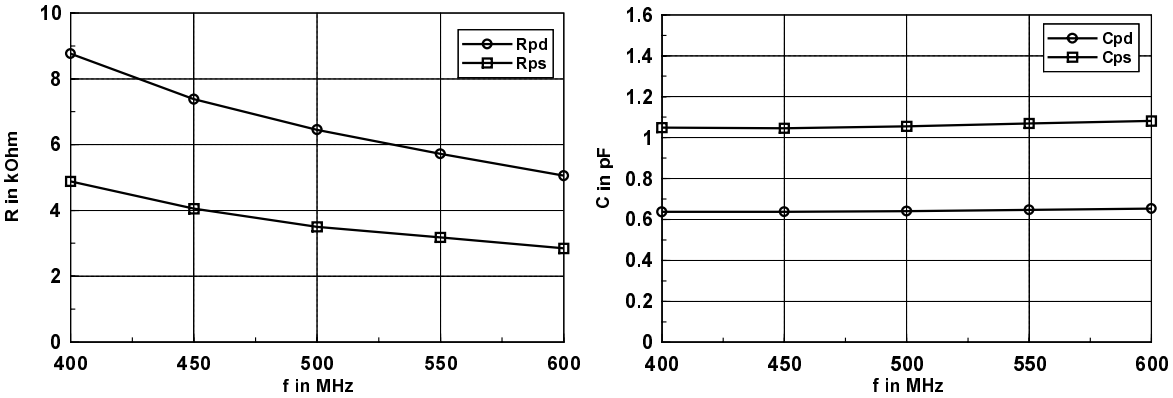


9.2 IF Input IF/IFX

S-parameters:

f	S11		S21		S12		S22	
GHZ	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
0.40	0.978	-15.0	0.057	74.0	0.057	73.7	0.977	-14.7
0.45	0.974	-16.8	0.063	72.5	0.064	72.0	0.972	-16.6
0.50	0.970	-18.8	0.070	70.8	0.070	70.2	0.968	-18.5
0.55	0.967	-20.9	0.076	69.2	0.076	68.4	0.963	-20.5
0.60	0.963	-23.0	0.082	67.5	0.082	66.7	0.957	-22.5

Input impedance at IF/IFX:

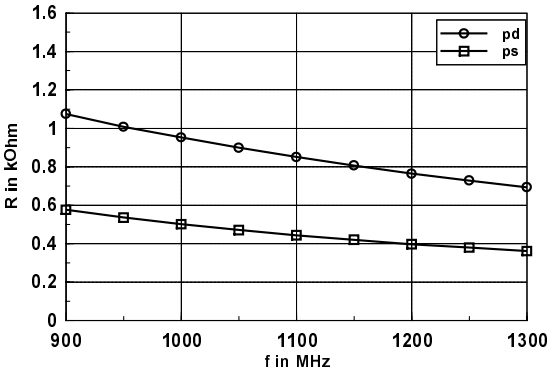


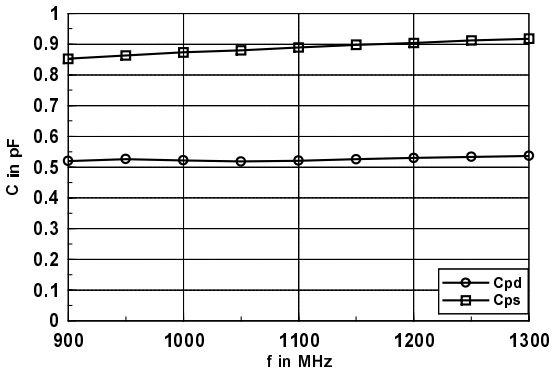
9.3 RF Input RFB1/RFB2

S-parameters:

f	S11		S21		S12		S22	
GHZ	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
0.90	0.850	-29.7	0.020	43.1	0.021	47.5	0.843	-31.8
0.95	0.840	-31.5	0.020	41.8	0.022	46.1	0.836	-33.6
1.00	0.832	-33.2	0.021	41.0	0.024	45.4	0.830	-35.4
1.05	0.823	-34.8	0.022	40.3	0.025	43.9	0.823	-37.2
1.10	0.815	-36.5	0.022	39.1	0.026	41.5	0.817	-39.0
1.15	0.807	-38.1	0.022	37.8	0.027	38.8	0.810	-40.8
1.20	0.799	-39.7	0.023	37.7	0.028	36.6	0.803	-42.6
1.25	0.792	-41.3	0.023	35.8	0.028	33.1	0.797	-44.3
1.300	0.785	-42.8	0.023	36.0	0.028	31.1	0.790	-46.0

Input impedance:



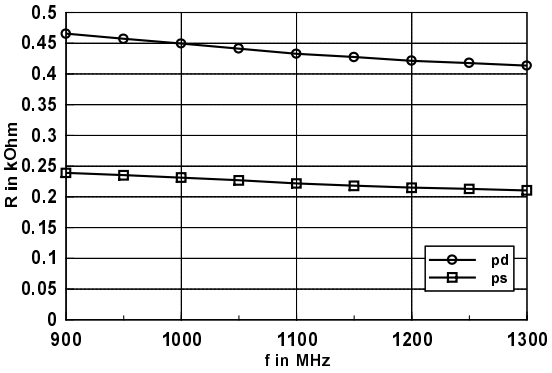


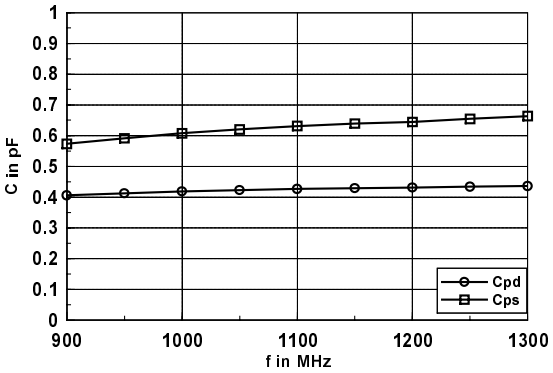
9.4 Output to Receiver RF/RFX

S-parameters:

f	S11		S21		S12		S22	
GHZ	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
0.90	0.556	-19.6	0.164	21.2	0.149	122.2	0.789	-20.8
0.95	0.543	-19.5	0.165	14.7	0.168	117.8	0.795	-23.4
1.00	0.532	-19.2	0.164	7.5	0.187	113.2	0.800	-26.3
1.05	0.524	-18.3	0.161	-0.6	0.207	108.3	0.805	-29.4
1.10	0.520	-17.2	0.155	-9.8	0.228	103.1	0.806	-32.8
1.15	0.524	-16.0	0.144	-19.6	0.248	97.3	0.803	-36.3
1.20	0.534	-14.8	0.132	-31.1	0.267	91.5	0.796	-40.0
1.25	0.551	-14.2	0.116	-43.9	0.283	85.2	0.783	-43.6
1.30	0.572	-14.1	0.101	-59.6	0.297	78.7	0.765	-47.2

Output impedance at RF/RFX:



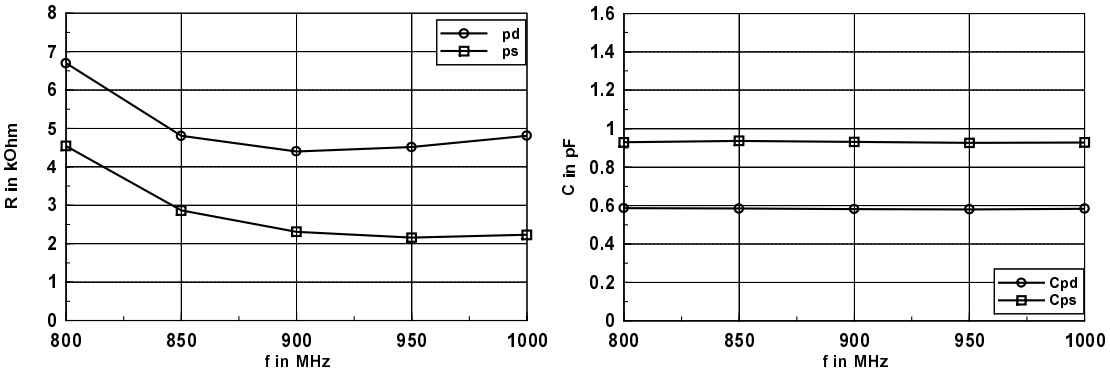


9.5 Modulator Output E/EX

S-parameters:

f	S11		S21		S12		S22	
GHz	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
0.80	0.972	-26.2	0.116	65.2	0.126	64.7	0.957	-25.2
0.85	0.960	-28.0	0.120	64.1	0.131	63.2	0.947	-26.4
0.90	0.951	-29.4	0.125	63.3	0.136	61.9	0.946	-27.8
0.95	0.948	-30.8	0.131	62.4	0.142	60.7	0.948	-29.3
1.00	0.949	-32.4	0.137	60.9	0.148	58.9	0.950	-31.2

Output impedance at E/EX:



9.6 Modulator Input LO/LOX

S-parameters:

f	S11		S21		S12		S22	
GHZ	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
0.80	0.896	-29.6	0.125	62.4	0.126	62.4	0.887	-32.1
0.85	0.888	-31.7	0.130	61.2	0.131	61.2	0.871	-34.1
0.90	0.879	-33.9	0.136	59.9	0.136	59.6	0.863	-35.9
0.95	0.871	-36.1	0.140	58.7	0.141	58.4	0.854	-37.9
1.00	0.861	-38.4	0.145	57.1	0.145	56.8	0.850	-40.0

Input impedance at LO/LOX: